32,768 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55257PL-85, TC55257P-10/PL-10
TC55257P-12/PL-12

DESCRIPTION

The TC55257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz(Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257P has two control inputs. Chip enable ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257P is offered in a dual-in-line 28 pin standard plastic package.

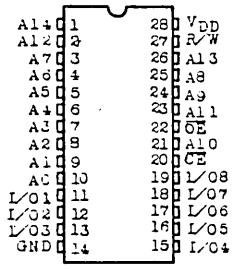
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  100uA(Max.): TC55257PL-85/PL-10/PL-12
  1mA(Max.): TC55257P-10/P-12
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Access Time

	TC55257PL-85	TC55257P-10 TC55257PL-10	TC55257P-12 TC55257PL-12
Access Time (Max.)	85ns	100ns	120ns
CE Access Time (Max.)	85ns	100ns	120ns
Output Enable Time(Max.)	40ns	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Standard 28 pin DIP

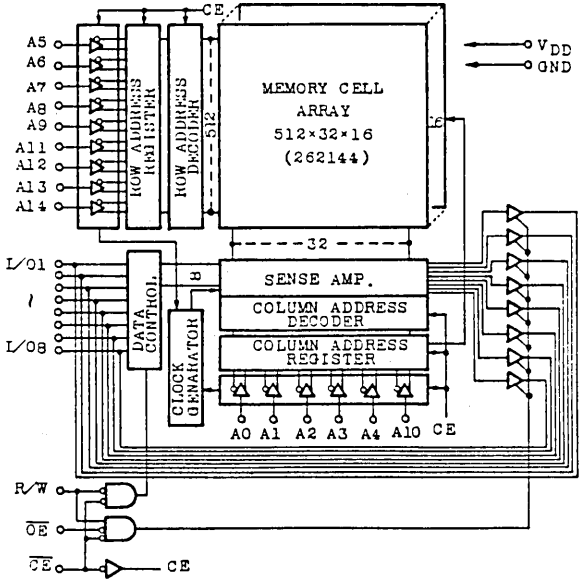
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3*~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 • 10	°C•sec
T_{strg}	Storage Temperature	-55 ~ 150	°C
T_{opr}	Operating Temperature	0 ~ 70	°C

* ..... -3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $R/W=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	$V_{DD}=5.5V$ $\overline{CE}=V_{IL}$, $R/W=V_{IH}$ Other Input $=V_{IH}/V_{IL}$ $I_{OUT}=0mA$	t_{cycle}=1μs	-	-	10	mA
			t_{cycle}= Min. cycle	-	-	70	
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE}=0.2V$, $R/W=V_{DD}-0.2V$ Other Input $=V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	t_{cycle}=1μs	-	-	5	mA
			t_{cycle}= Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE}=V_{DD}-0.2V$ $V_{DD}=2.0 \sim 5.5V$	TC55257PL	-	2	100	μA
			TC55257P	-	-	1.0	mA

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

CAPACITANCE ($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN}=2.4V/0.6V V_{IH}=2.2V V_{IL}=0.8V t_r, t_f≦5ns V_{OH}=2.2V V_{OL}=0.8V Output Load: C_L(100pF) and 1 TTL Gate	85	-	100	-	120	-	ns
t_{ACC}	Address Access Time		-	85	-	100	-	120	
t_{CO}	$\overline{CE}$ Access Time		-	85	-	100	-	120	
t_{OE}	Output Enable to Output in Valid		-	40	-	50	-	60	
t_{COE}	Chip Enable($\overline{CE}$)to Output in Low-Z		10	-	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z		5	-	5	-	5	-	
t_{OD}	Chip Enable($\overline{CE}$)to Output in High-Z		-	30	-	50	-	60	
t_{ODO}	Output Enable to Output in High-Z		-	30	-	40	-	50	
t_{OH}	Output Data Hold Time		5	-	10	-	10	-	

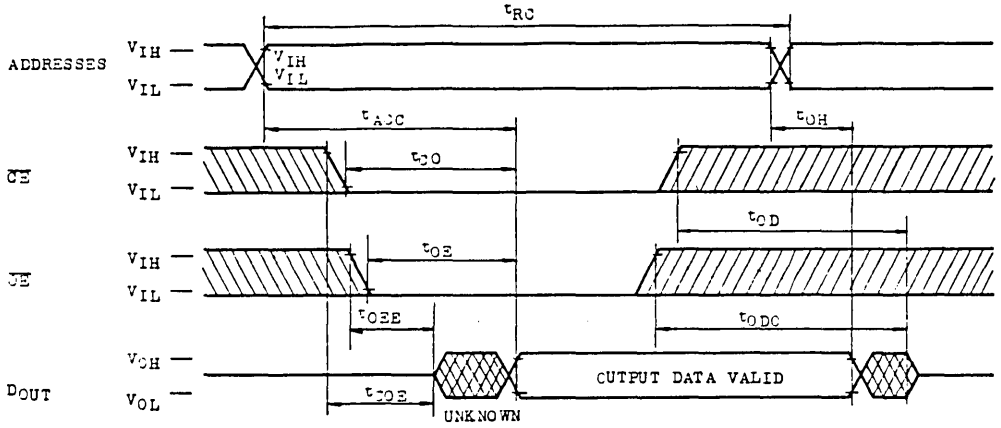
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN}=2.4V/0.6V V_{IH}=2.2V V_{IL}=0.8V t_r, t_f≦5ns	85	-	100	-	120	-	ns
t_{WP}	Write Pulse Width		60	-	70	-	80	-	
t_{CW}	Chip Selection to End of Write		65	-	90	-	100	-	
t_{AS}	Address Set up Time		0	-	0	-	0	-	
t_{WR}	Write Recovery Time		10	-	10	-	10	-	
t_{ODW}	R/W to Output High-Z		-	30	-	50	-	60	
t_{OEW}	R/W to Output Low-Z		10	-	10	-	10	-	
t_{DS}	Data Set up Time		40	-	40	-	50	-	
t_{DH}	Data Hold Time		0	-	0	-	0	-	

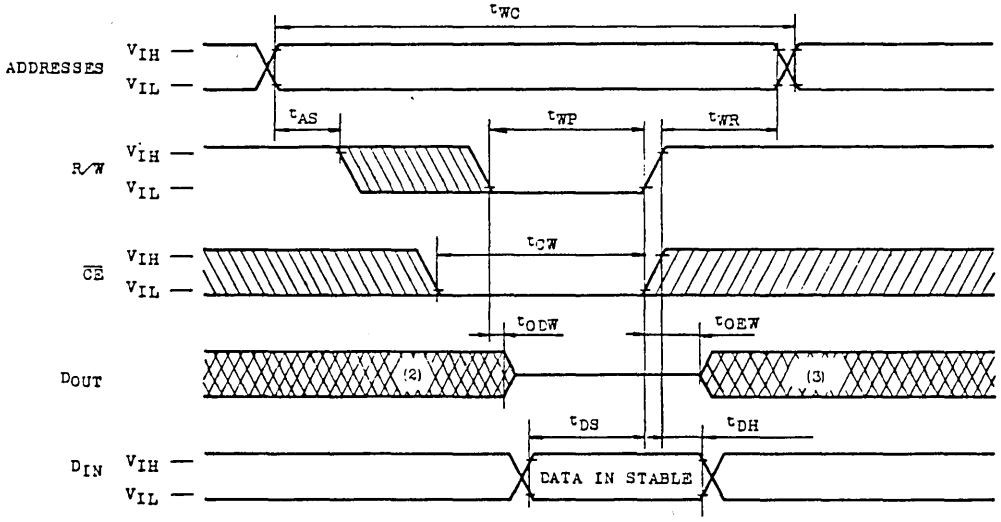
Note: Input pulse levels=V_{IN}
Timing Measurement Reference levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

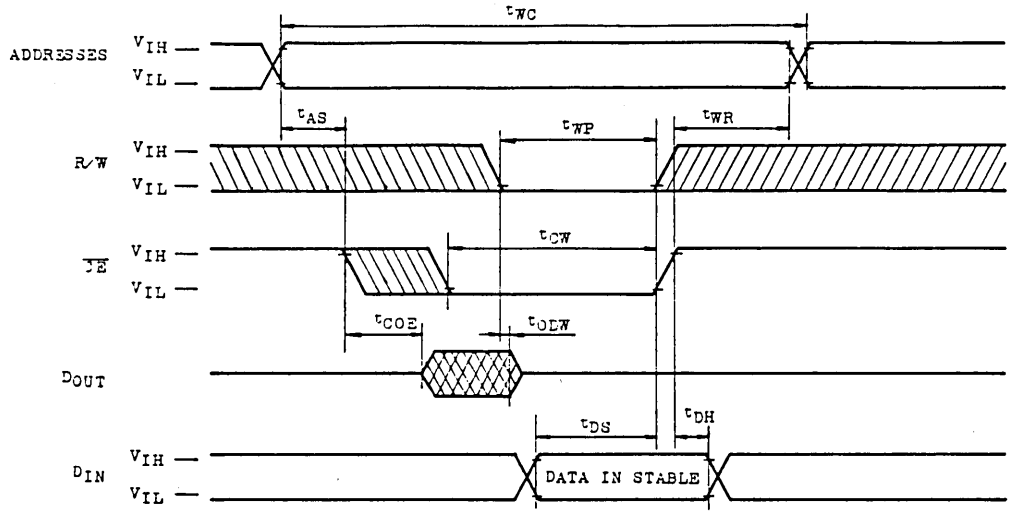
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

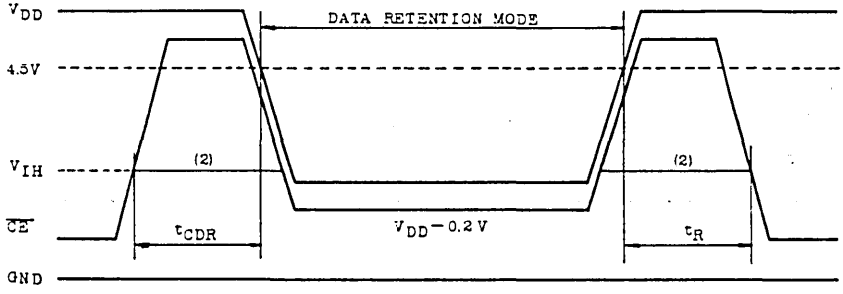
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	TC55257PL	V_{DD}=3.0V	-	-	50	μA
			V_{DD}=5.5V	-	-	100	
		TC55257P		-	-	1.0	mA
t_{CDR}	Chip Deselection to Data Retention Mode			0	-	-	μs
t_R	Recovery Time			t_{RC}(1)	-	-	

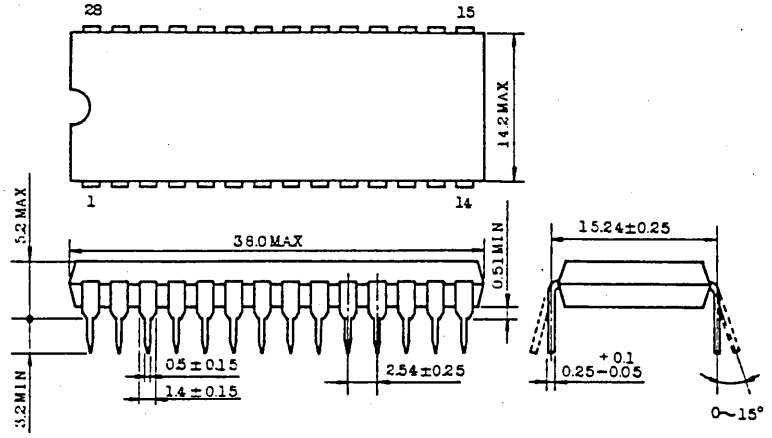
Note (1): Read cycle time

$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

DIP 28 PIN OUTLINE DRAWING (6D28A-P) Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.