SILICON GATE CMOS

32,768 WORD x 9 BIT CMOS STATIC RAM

Description

The TC55329AP/AJ is a 294,912 bit high speed CMOS static random access memory organized as 32,768 words by 9 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55329AP/AJ features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, CE2) and has an output enable input ($\overline{OE}$) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

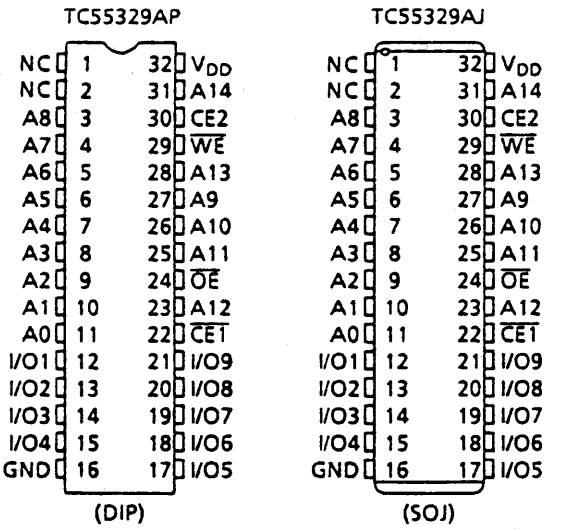
The TC55329AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55329AP/AJ is available in a 300mil width, 32-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
  - TC55329AP/AJ-15 15ns (max.)
  - TC55329AP/AJ-20 20ns (max.)
  - TC55329AP/AJ-25 25ns (max.)
  - TC55329AP/AJ-35 35ns (max.)
- Low power dissipation
  - Operation:
  - TC55329AP/AJ-15 140mA (max.)
  - TC55329AP/AJ-20 140mA (max.)
  - TC55329AP/AJ-25 140mA (max.)
  - TC55329AP/AJ-35 120mA (max.)
  - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Package:
  - TC55329AP: DIP32-P-300
  - TC55329AJ: SOJ32-P-300

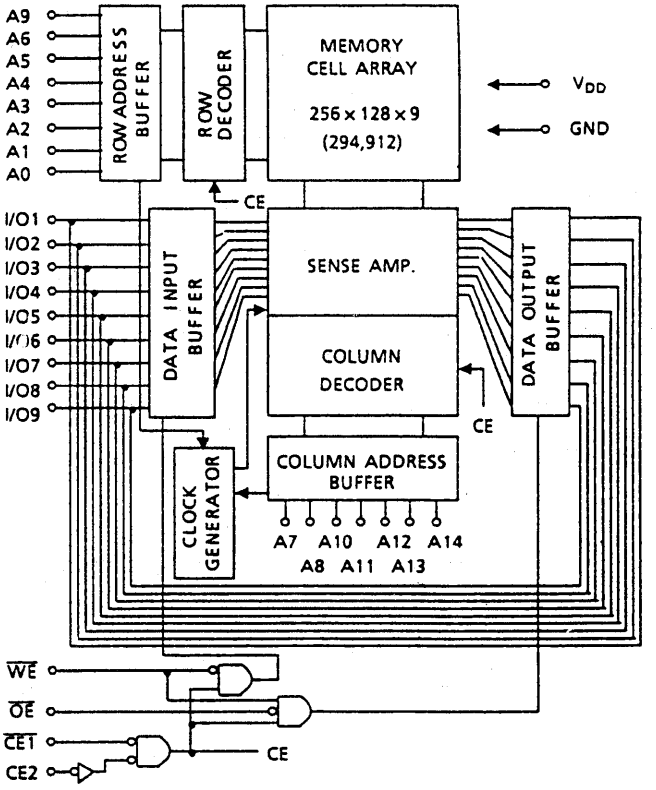
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O1 ~ I/O9	POWER
Read	L	H	L	H	Output	I_{DDO}
Write	L	H	*	L	Input	I_{DDO}
Output Disable	L	H	H	H	High Impedance	I_{DDO}
Standby	H	*	*	*	High Impedance	I_{DDS}
	*	L	*	*	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0 ~ V_{DD}		–	–	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	t_{cycle} = Min cycle $\overline{CE1}$ = V_{IL} or CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL}	-15	–	–	140	mA
			-20	–	–	140	
			-25	–	–	140	
			-35	–	–	120	
I_{DDS1}	Standby Current	t_{cycle} = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}	-15	–	–	20	mA
			-20				
			-25				
			-35				
I_{DDS2}		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55329AP/AJ-15		TC55329AP/AJ-20		TC55329AP/AJ-25		TC55329AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO1}	$\overline{CE1}$ Access Time	–	15	–	20	–	25	–	35	
t_{CO2}	CE2 Access Time	–	15	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	–	12	–	15	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	8	–	8	–	10	–	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	10	–	15	

Write Cycle

SYMBOL	PARAMETER	TC55329AP/AJ-15		TC55329AP/AJ-20		TC55329AP/AJ-25		TC55329AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	10	–	11	–	13	–	18	–	
t_{AW}	Address Valid to End of Write	12	–	13	–	15	–	20	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	20	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	12	–	15	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	10	–	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

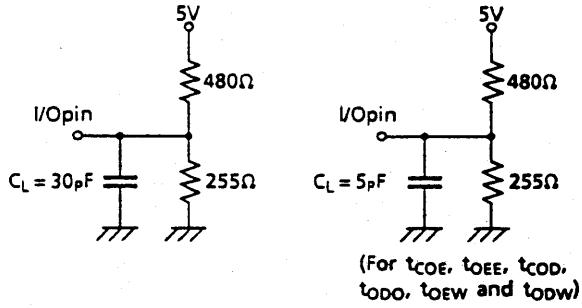
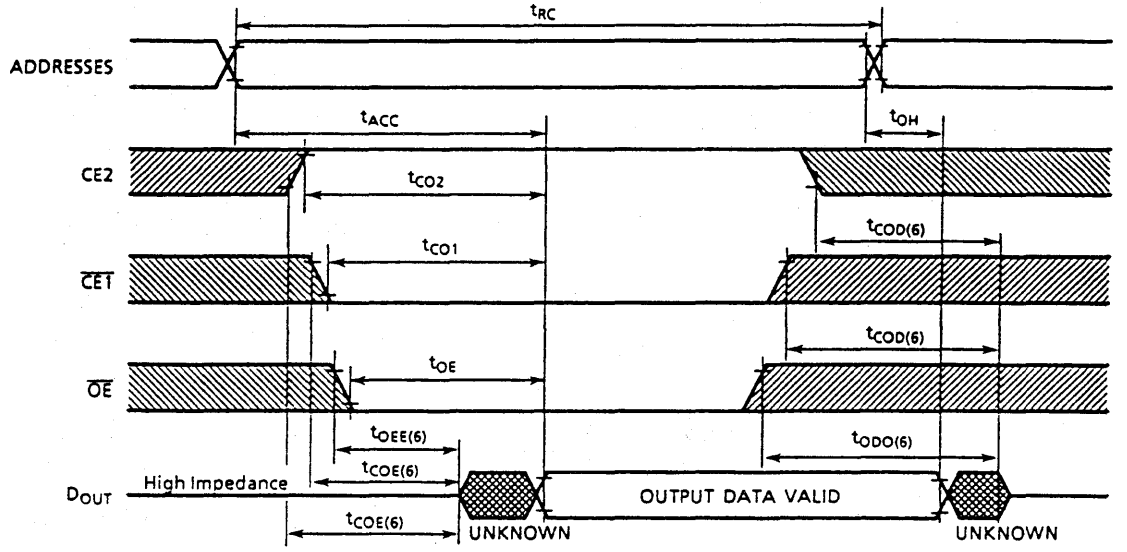


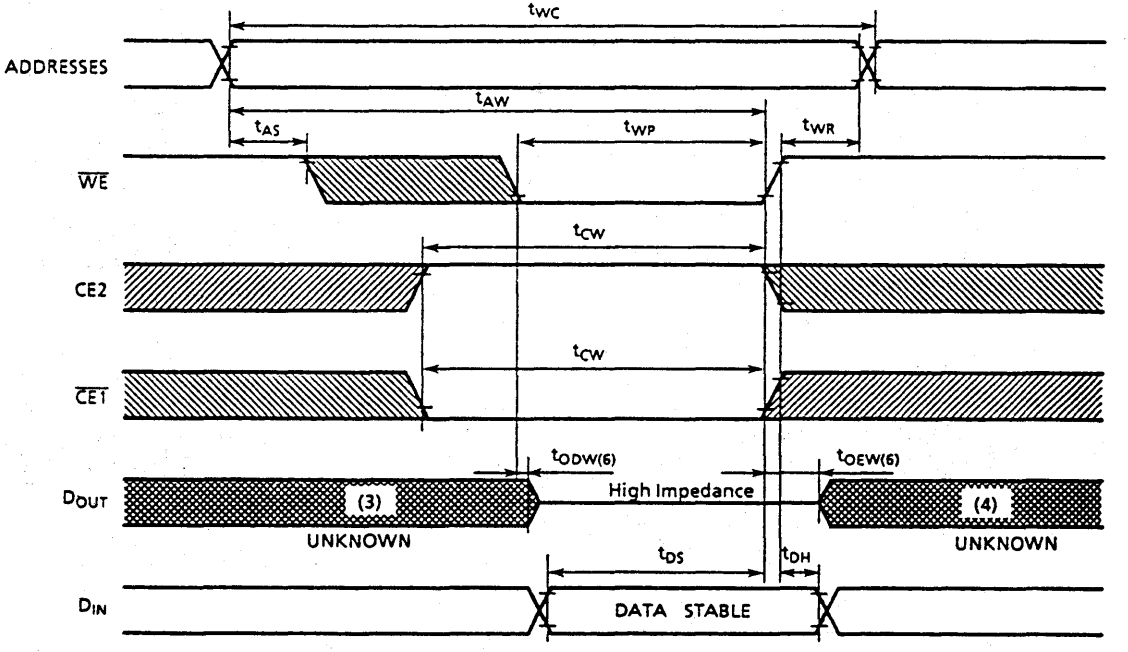
Figure 1.

Timing Waveforms

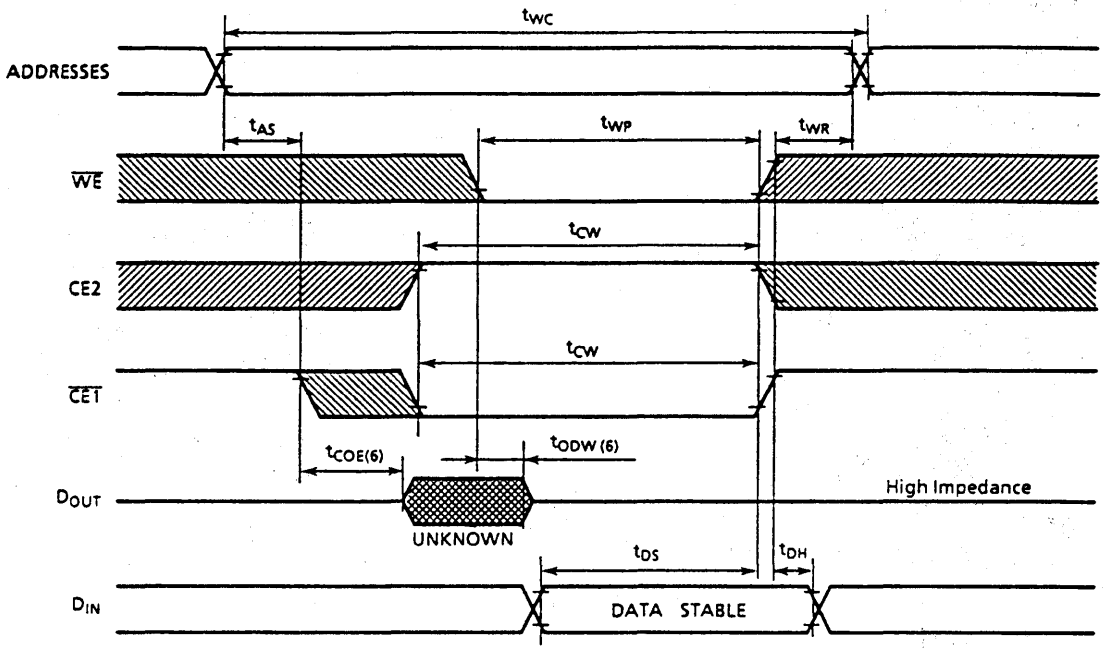
Read Cycle [2]



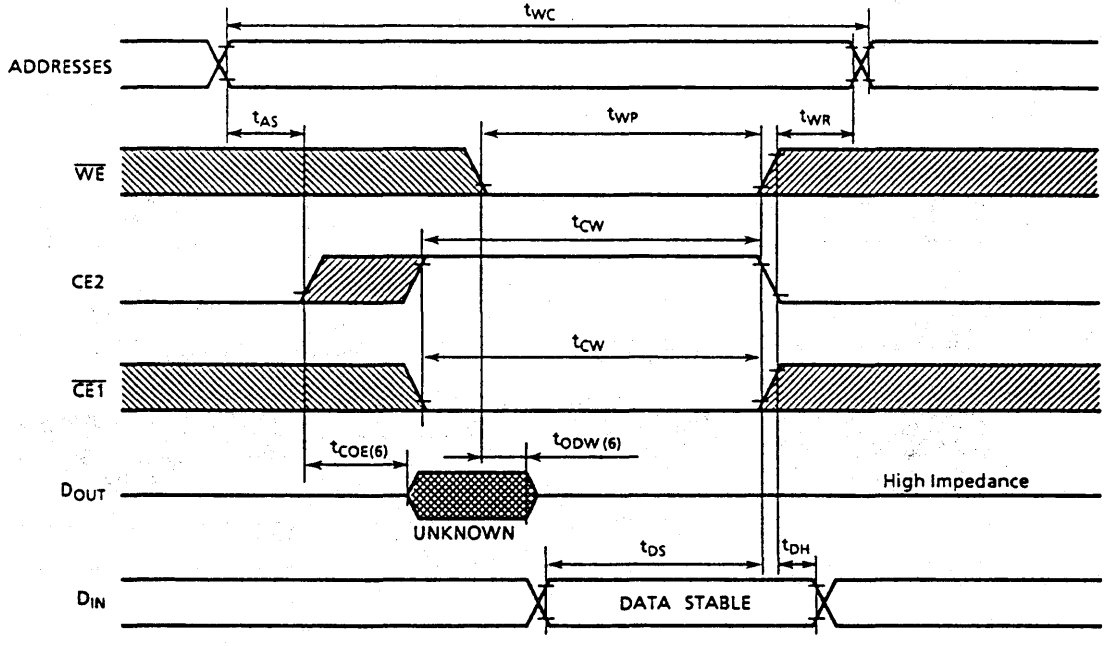
Write Cycle 1 [5] (WE Controlled Write)



Write Cycle 2 [5] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [5] (CE2 Controlled Write)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is high for read cycles.

3. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

4. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the $\overline{WE}$ high transition, outputs remain in a high impedance state.

5. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time