TC554101J-20/25/30

PRELIMINARY

SILICON GATE CMOS

1,048,576 WORD x 4 BIT SEPARATE I/O CMOS STATIC RAM

Description

The TC554101J is a 4,194,304 bit high speed CMOS static random access memory organized as 1,048,576 words by 4 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC554101J features low power dissipation when the device is deselected using chip enable ($\overline{CE}$), and has an output enable input ($\overline{OE}$) for fast memory access.

The TC554101J is suitable for use in applications where high speed is required such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC554101J is available in a 400mil width, 36-pin SOJ suitable for high density surface assembly.

Features

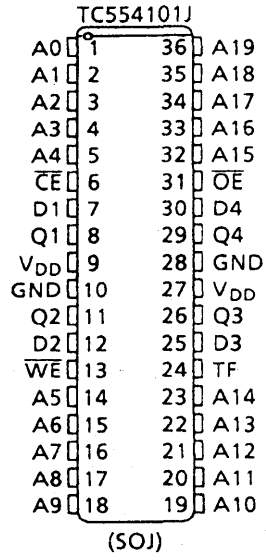
- Fast access time
  - TC554101J -20 20ns (max.)
  - TC554101J -25 25ns (max.)
  - TC554101J -30 30ns (max.)
- Low power dissipation
  - TC554101J -20 160mA (max.)
  - TC554101J -25 160mA (max.)
  - TC554101J -30 150mA (max.)
  - Standby: 10mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Separate inputs and outputs
- Output buffer control: $\overline{OE}$
- Package:
  - TC554101J: SOJ36-P-400

Pin Names

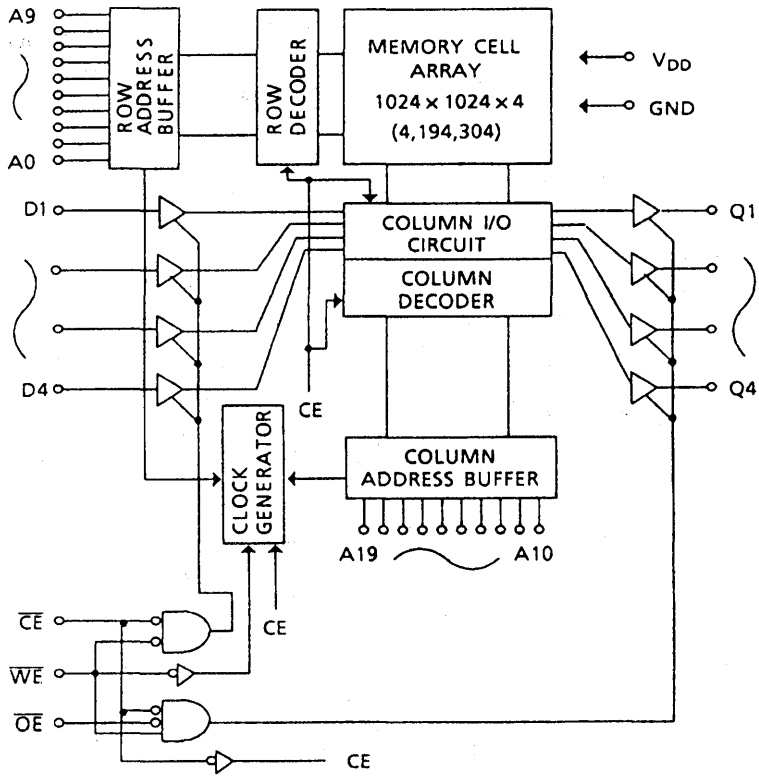
A0 ~ A19	Address Inputs
D1 ~ D4	Data Inputs
Q1 ~ Q4	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
TF*	Test Function

* The TF pin is low for normal operation.

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Disable	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{OUT}	Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

*-3V with a pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	-20	–	–	160	mA
			-25	–	–	160	
			-30	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	10	

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554101J -20		TC554101J -25		TC554101J -30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	ns
t_{ACC}	Address Access Time	–	20	–	25	–	30	
t_{CO}	Chip Enable Access Time	–	20	–	25	–	30	
t_{OE}	Output Enable Access Time	–	10	–	12	–	14	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	10	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	20	–	25	–	30	

Write Cycle

SYMBOL	PARAMETER	TC554101J -20		TC554101J -25		TC554101J -30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	–	25	–	30	–	ns
t_{WP}	Write Pulse Width	11	–	13	–	15	–	
t_{AW}	Address Valid to End of Write	17	–	20	–	23	–	
t_{CW}	Chip Enable to End of Write	17	–	20	–	23	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	10	–	12	
t_{DS}	Data Setup Time	10	–	12	–	14	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

Test Mode

SYMBOL	PARAMETER	TC554101J -20		TC554101J -25		TC554101J -30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SWE}	$\overline{WE}$ Setup Time to TF	20	–	25	–	30	–	ns
t_{HWE}	$\overline{WE}$ Hold Time from TF	20	–	25	–	30	–	
t_{SCE}	$\overline{CE}$ Setup Time to TF	20	–	25	–	30	–	
t_{HCE}	$\overline{CE}$ Hold Time from TF	20	–	25	–	30	–	
t_{SADD}	Address Setup Time to TF	20	–	25	–	30	–	
t_{HADD}	Address Hold Time to TF	20	–	25	–	30	–	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

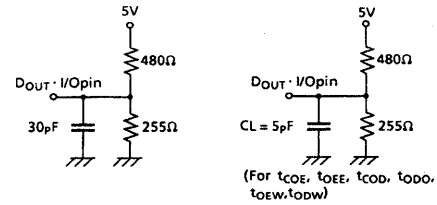
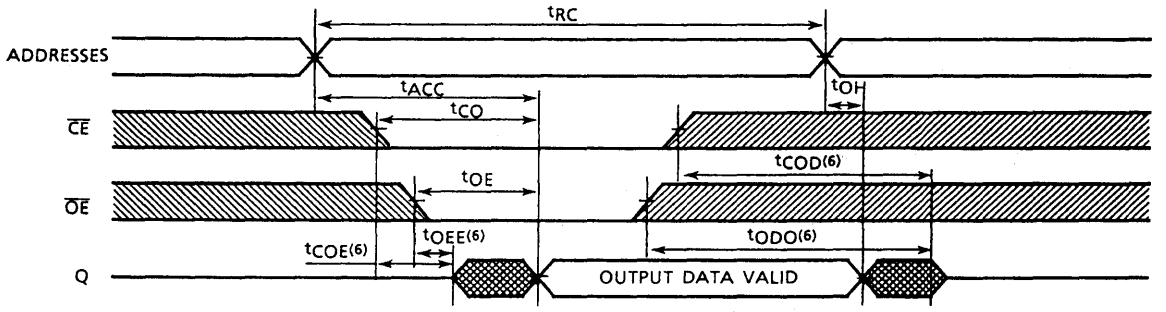


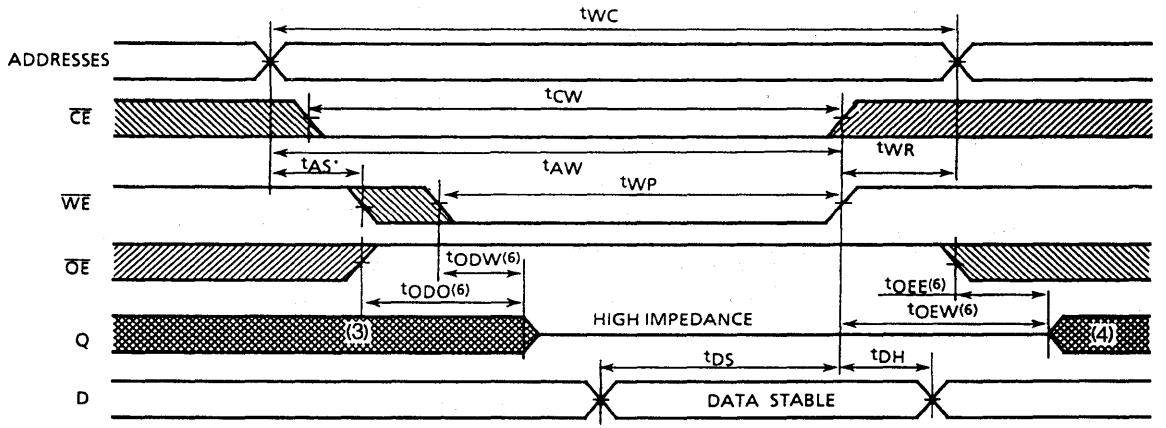
Figure 1.

Timing Waveforms

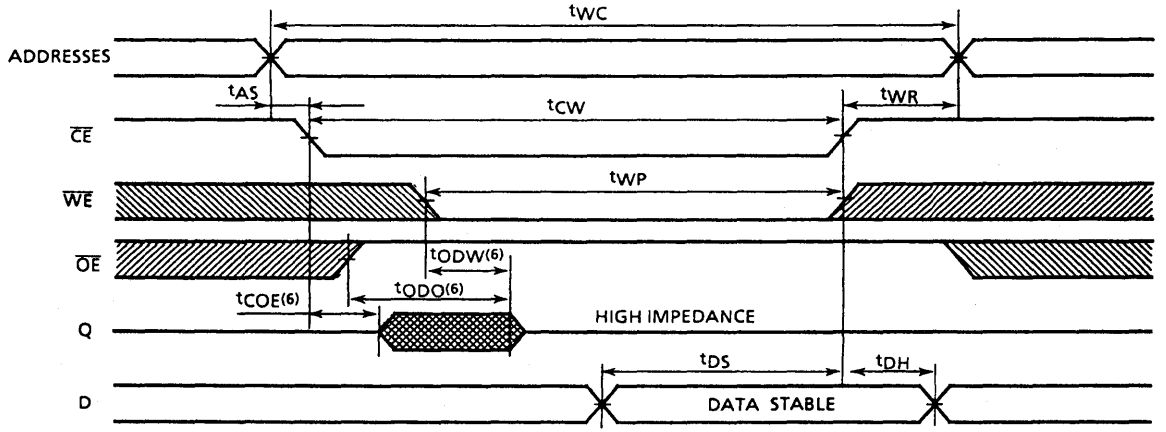
Read Cycle (2)



Write Cycle 1 (5) (WE Controlled Write)



Write Cycle 2 (5) (CE Controlled Write)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

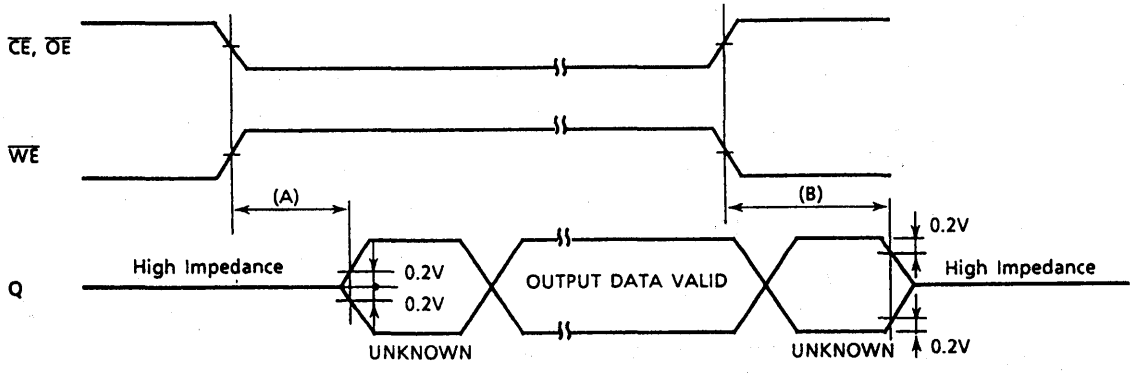
2. $\overline{WE}$ is high for read cycles.

3. If the $\overline{CE}$ low transition occurs coincident with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

4. If the $\overline{CE}$ high transition occurs coincident with or prior to the $\overline{WE}$ high transition, outputs remain in a high impedance state.

5. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Test Mode

Although the TC554101J appears to be organized as 1,048,576 words by 4 bits, it is internally organized as 524,288 words by 8 bits.

In the "Test Mode", data is written into the 8-512K blocks in parallel and then retrieved. Address line A19 is not used. Upon reading, if the two bits associated with the I/O pin are equal (all "1"s or "0"s), the output pin indicates a "1". If they are not equal, the output pin would indicate a "0". Fig. 3 show the block diagram of the TC554101J. The "Test Mode" enables the 1M word memory to be tested as if it were only a 512K word memory. The "Test Mode" function can be performed in any timing cycle when the "TF" pin is held at V_{IH} (see Figure 2). Normal functioning requires that the "TF" pin be connected to V_{IL}.

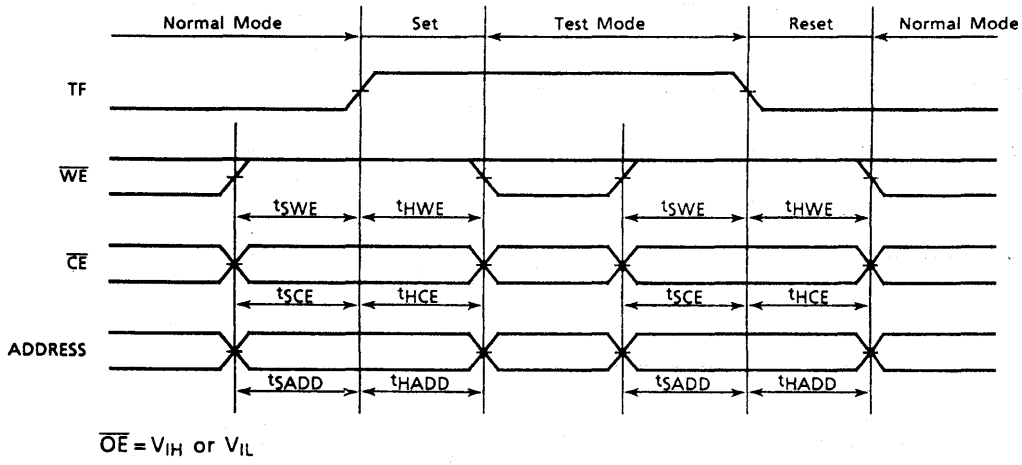


Figure 2. Test Mode Cycle

Block Diagram in Test Mode

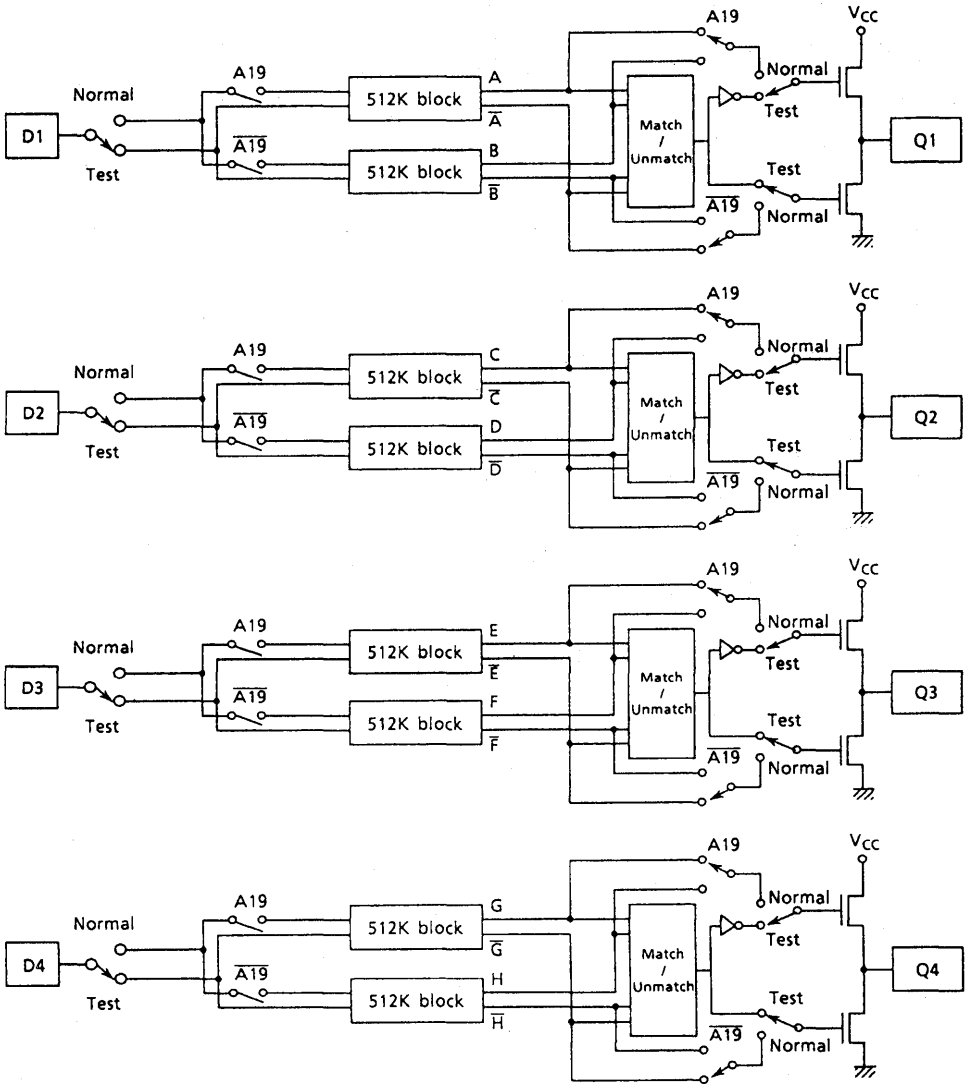


Figure 3. Block Diagram in Test Mode