

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT STATIC RAM

DESCRIPTION

The TC554161AFTI is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2 μA standby current (typ) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. Data byte control pin (\overline{LB} , \overline{UB}) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of -40° to 85°C, the TC554161AFTI can be used in environments exhibiting extreme temperature conditions. The TC554161AFTI is available in a plastic 54-pin thin -small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 55 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10%
- Power down features using \overline{CE} .
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum):

	TC554161AFTI	
	-70,-85,-10	-70L,-85L,-10L
5.5 V	200 μA	100 μA
3.0 V	100 μA	50 μA

- Access Times (maximum):

	TC554161AFTI		
	-70,-70L	-85,-85L	-10,-10L
Access Time	70 ns	85 ns	100 ns
\overline{CE} Access Time	70 ns	85 ns	100 ns
\overline{OE} Access Time	35 ns	45 ns	50 ns

- Package:

TSOP II54-P-400-0.80 (AFTI) (Weight: 0.57 g typ)

PIN ASSIGNMENT (TOP VIEW)

NC	1	54	A4
A3	2	53	A5
A2	3	52	A6
A1	4	51	A7
A0	5	50	NC
I/O16	6	49	I/O1
I/O15	7	48	I/O2
V _{DD}	8	47	V _{DD}
GND	9	46	GND
I/O14	10	45	I/O3
I/O13	11	44	I/O4
\overline{UB}	12	43	\overline{LB}
\overline{CE}	13	42	\overline{OE}
OP	14	41	OP
R/W	15	40	NC
I/O12	16	39	I/O5
I/O11	17	38	I/O6
GND	18	37	GND
V _{DD}	19	36	V _{DD}
I/O10	20	35	I/O7
I/O9	21	34	I/O8
NC	22	33	A8
A17	23	32	A9
A16	24	31	A10
A15	25	30	A11
A14	26	29	A12
A13	27	28	NC

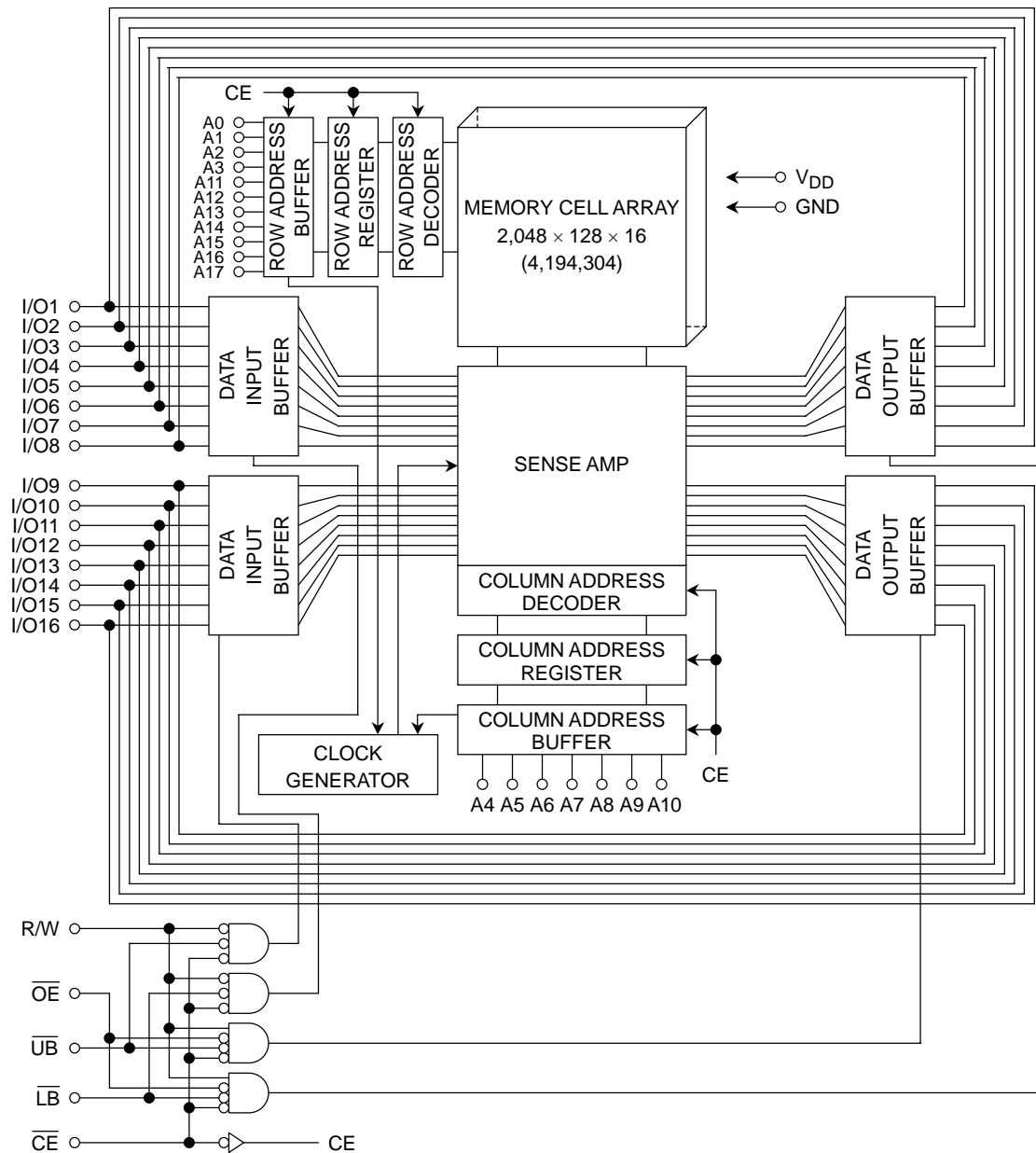
(Normal pinout)

PIN NAMES

A0~A17	Address Inputs
I/O1~I/O16	Data Inputs/Outputs
\overline{CE}	Chip Enable
R/W	Read/Write Control
\overline{OE}	Output Enable
\overline{LB} , \overline{UB}	Data Byte Control
V _{DD}	Power (+5 V)
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3*~7.0	V
V _{I/O}	Input/Output Voltage	-0.5~V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{stg}	Storage Temperature	-55~150	°C
T _{opr}	Operating Temperature	-40~85	°C

*: -3.0V when measured at a pulse width of 30ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	—	0.6	V
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

*: -3.0V when measured at a pulse width of 30 ns

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V~V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 V~V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4 V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V			2.1	—	—	mA
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} , I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}		t _{cycle} = 70 ns	—	—	110	mA
				t _{cycle} = 85 ns, 100 ns	—	—	100	
				t _{cycle} = 1 μs	—	15	—	
I _{DDO2}	Operating Current	$\overline{CE} = 0.2$ V and R/W = V _{DD} - 0.2 V, I _{OUT} = 0 mA, Other Input = V _{DD} - 0.2 V/0.2 V		t _{cycle} = 70 ns	—	—	100	mA
				t _{cycle} = 85 ns, 100 ns	—	—	90	
				t _{cycle} = 1 μs	—	10	—	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		—	—	3	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V, V _{DD} = 2.0 V~5.5 V	-70,-85,-10	Ta = 25°C	—	2		—
				Ta = -40~85°C	—	—		200
			-70L,-85L,-10L	Ta = 25°C	—	2		5
	Ta = -40~85°C			—	—	100		

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	R/W	\overline{LB}	\overline{UB}	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I _{DDO}
				H	L	High-Z	Output	I _{DDO}
				L	H	Output	High-Z	I _{DDO}
Write	L	*	L	L	L	Input	Input	I _{DDO}
				H	L	High-Z	Input	I _{DDO}
				L	H	Input	High-Z	I _{DDO}
Output Deselect	L	H	H	*	*	High-Z	High-Z	I _{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High-Z	High-Z	I _{DDS}

* = don't care

H = logic high

L = logic low

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -40° to 85°C, VDD = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554161AFTI						UNIT
		-70,-70L		-85,-85L		-10,-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	Chip Enable Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable Access Time	—	35	—	45	—	50	
t _{BA}	Data Byte Control Access Time	—	35	—	45	—	50	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	5	—	
t _{OEE}	Output Enable Low to Output Active	0	—	0	—	0	—	
t _{BE}	Data Byte Control Low to Output Active	0	—	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	30	—	35	—	40	
t _{ODO}	Output Enable High to Output High-Z	—	30	—	35	—	40	
t _{BD}	Data Byte Control High to Output High-Z	—	30	—	35	—	40	

WRITE CYCLE

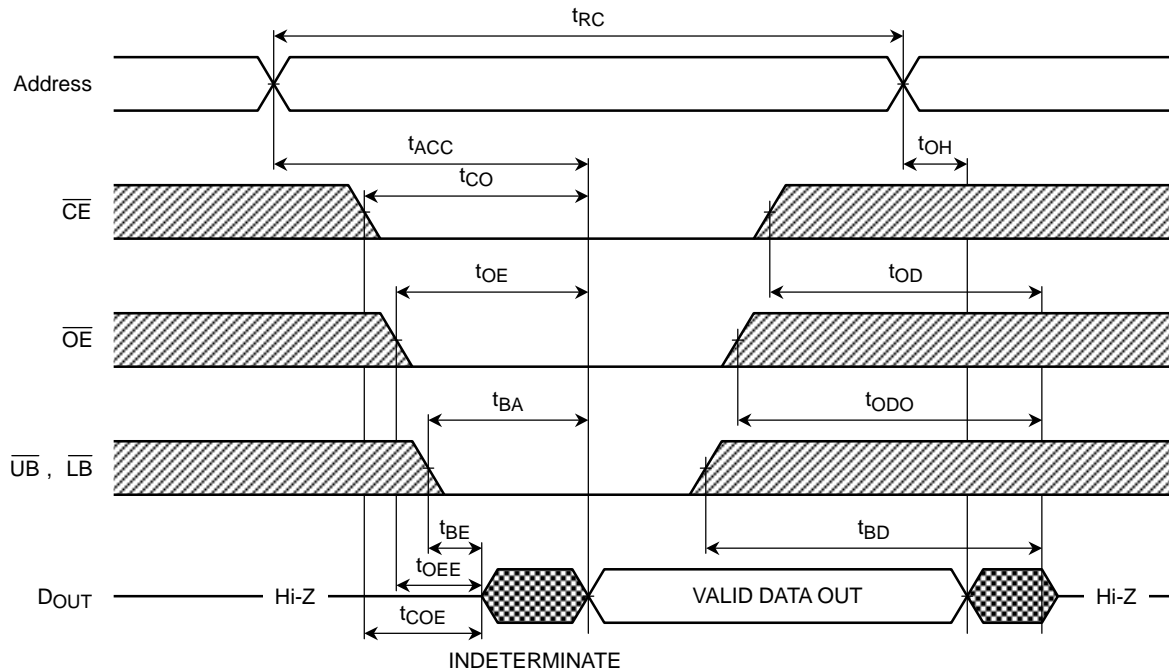
SYMBOL	PARAMETER	TC554161AFTI						UNIT
		-70,-70L		-85,-85L		-10,-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	55	—	60	—	
t _{CW}	Chip Enable to End of Write	60	—	70	—	80	—	
t _{BW}	Data Byte Control to End of Write	50	—	55	—	60	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OEW}	R/W High to Output Active	0	—	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	30	—	35	—	40	

AC TEST CONDITIONS

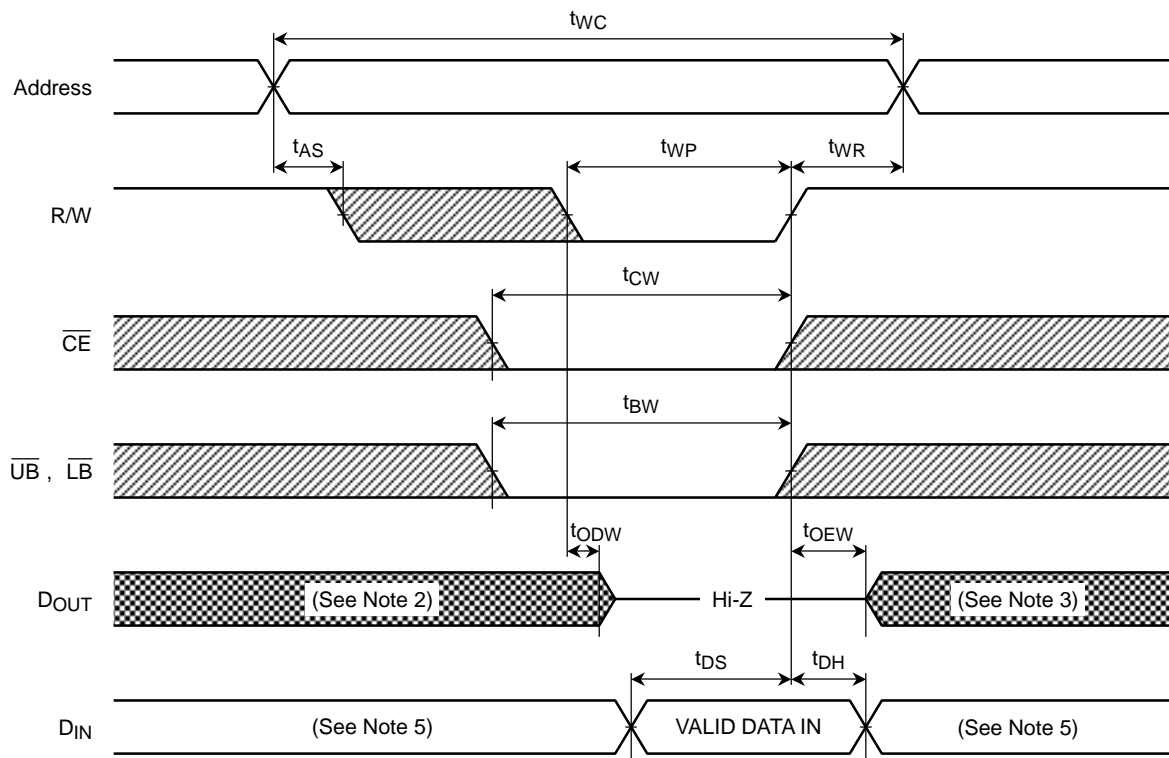
PARAMETER	TEST CONDITION
Output load	100 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.6 V
Timing measurements	1.5 V
Reference level	1.5 V
t _R , t _F	5 ns

TIMING DIAGRAMS

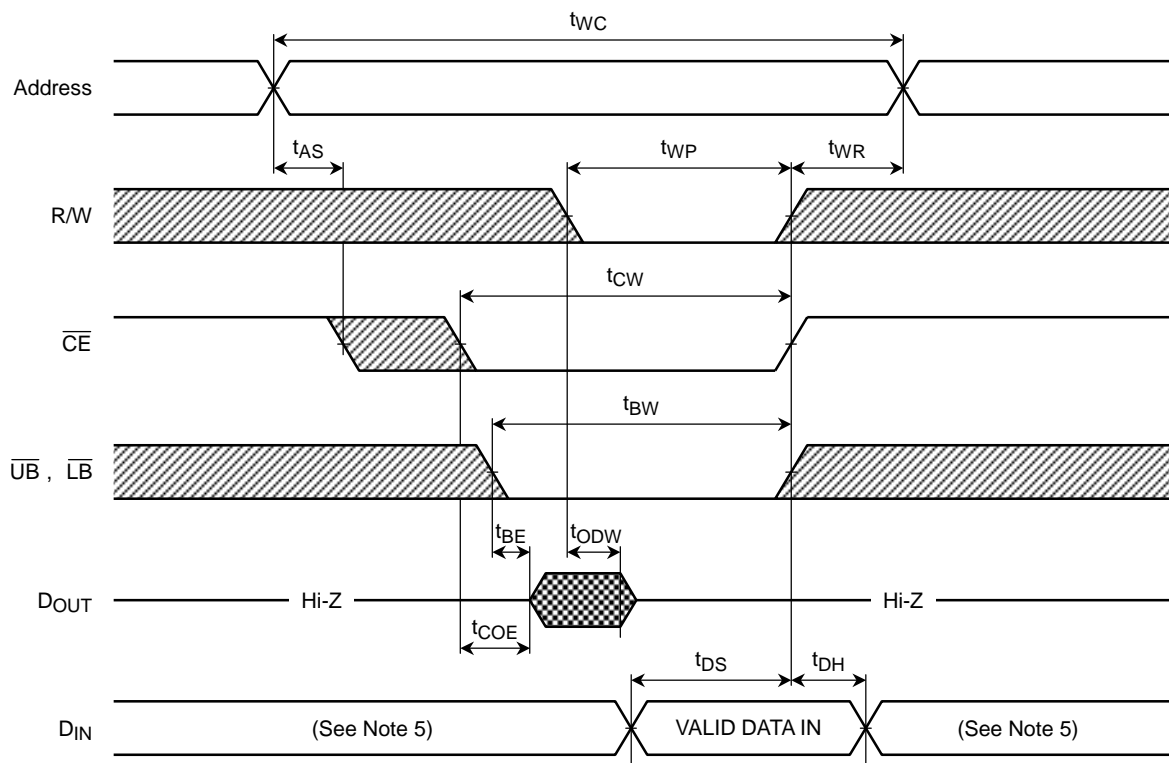
READ CYCLE (See Note 1)



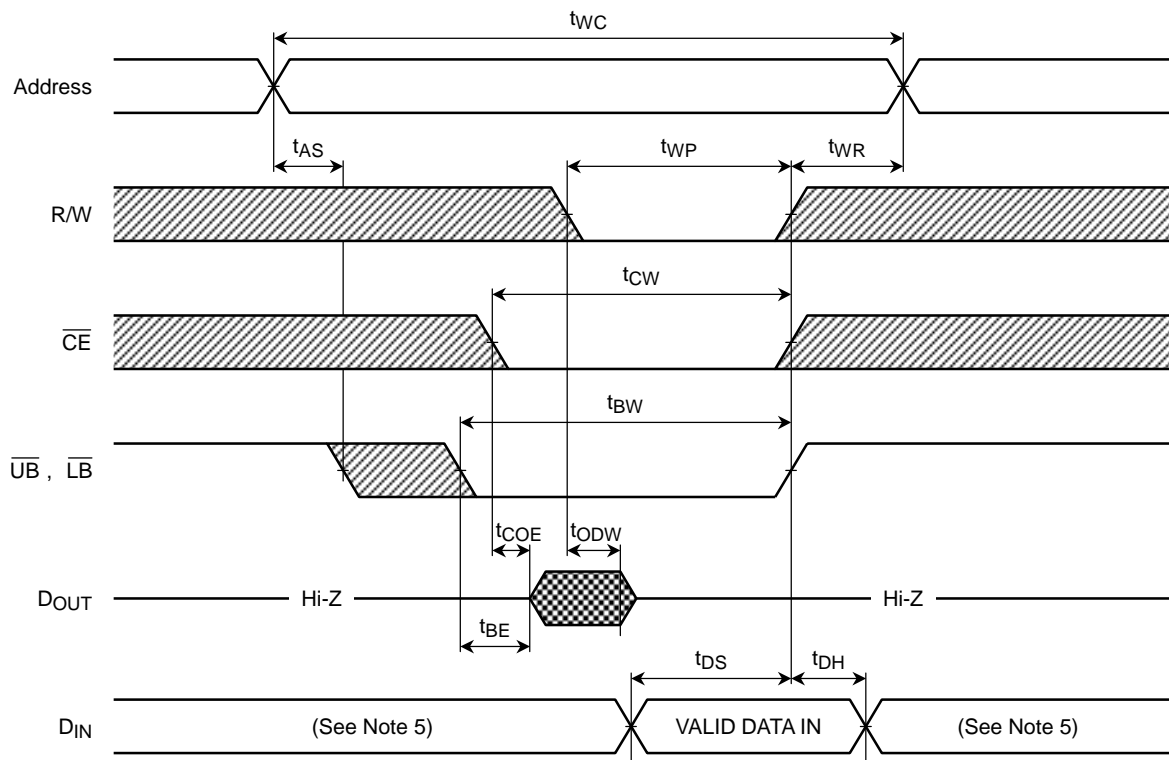
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



WRITE CYCLE 3 (\overline{UB} , \overline{LB} CONTROLLED) (See Note 4)



Note:

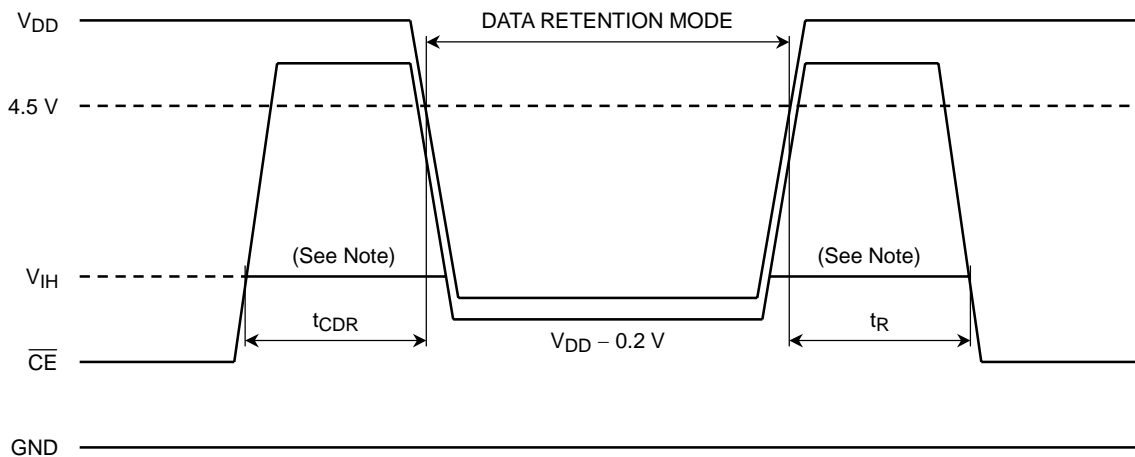
- (1) R/W remains HIGH for the read cycle.
- (2) If \overline{CE} goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V	
I _{DDS2}	Standby Current	-70,-85,-10	V _{DH} = 3.0 V	—	—	100	μA
			V _{DH} = 5.5 V	—	—	200	
		-70L,-85L,-10L	V _{DH} = 3.0 V	—	—	50*	
			V _{DH} = 5.5 V	—	—	100	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns	
t _R	Recovery Time		5	—	—	ms	

*: 5 μA (max) at Ta = -40° to 40°C

CE CONTROLLED DATA RETENTION MODE

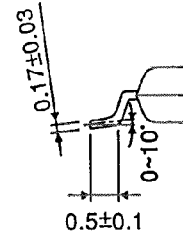
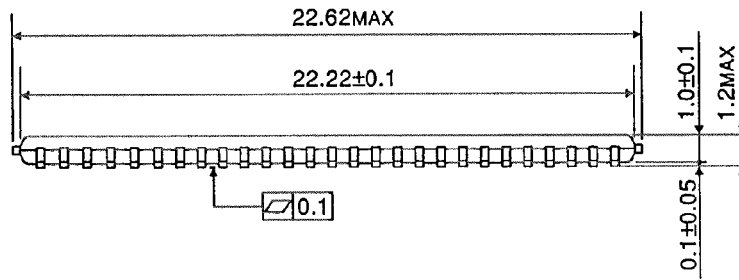
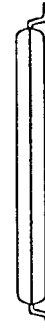
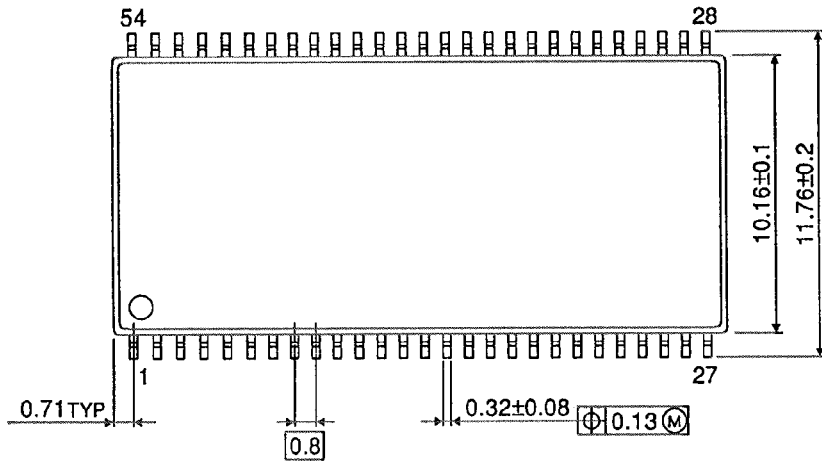


Note: When \overline{CE} is operating at the V_{IH} level (2.4V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6V.

PACKAGE DIMENSIONS

TSOPII54-P-400-0.80

Unit: mm



Weight: 0.57 g (typ)

RESTRICTIONS ON PRODUCT USE

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