

### SILICON GATE CMOS

### 65,536 WORD x 4 BIT CMOS STATIC RAM

#### Description

The TC55465AP/AJ is a 262,144 bit high speed CMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55465AP/AJ features low power dissipation when the device is deselected using chip enable ( $\overline{CE}$ ) and has an output enable input ( $\overline{OE}$ ) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

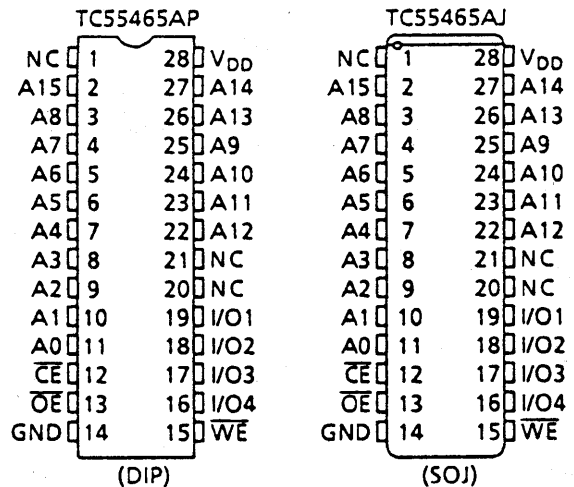
The TC55465AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55465AP/AJ is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

#### Features

- Fast access time
  - TC55465AP/AJ-15 15ns (max.)
  - TC55465AP/AJ-20 20ns (max.)
  - TC55465AP/AJ-25 25ns (max.)
  - TC55465AP/AJ-35 35ns (max.)
- Low power dissipation
  - Operation:
    - TC55465AP/AJ-15 120mA (max.)
    - TC55465AP/AJ-20 120mA (max.)
    - TC55465AP/AJ-25 120mA (max.)
    - TC55465AP/AJ-35 100mA (max.)
  - Standby: 1mA (max.)
- Single 5V power supply:  $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control:  $\overline{OE}$
- Package:
  - TC55465AP: DIP28-P-300B
  - TC55465AJ: SOJ28-P-300A

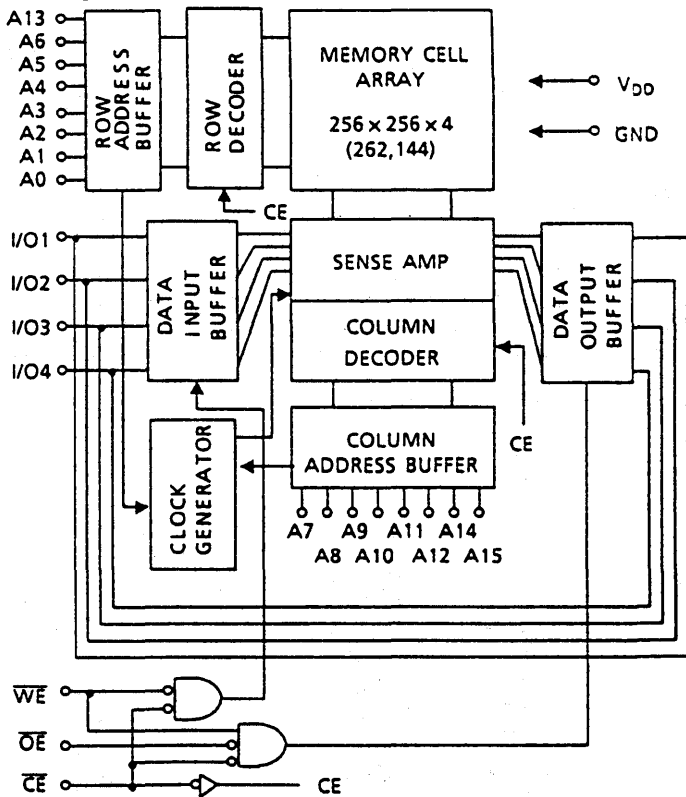
#### Pin Connection (Top View)



#### Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
WE	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 ~ I/O4	POWER
Read	L	L	H	Output	$I_{DDO}$
Write	L	*	L	Input	$I_{DDO}$
Output Disable	L	H	H	High Impedance	$I_{DDO}$
Standby	H	*	*	High Impedance	$I_{DDS}$

\*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
$V_{DD}$	Power Supply Voltage	-0.5 ~ 7.0	V
$V_{IN}$	Input Voltage	-2.0 ~ 7.0	V
$V_{IO}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
$P_D$	Power Dissipation	1.0	W
$T_{SOLDER}$	Soldering Temperature • Time	260 • 10	°C • sec
$T_{STRG}$	Storage Temperature	-65 ~ 150	°C
$T_{OPR}$	Operating Temperature	-10 ~ 85	°C

\*-3V with a pulse width of 10ns

## DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
$V_{IH}$	Input High Voltage	2.2	-	$V_{DD} + 0.5$	V
$V_{IL}$	Input Low Voltage	-0.5*	-	0.8	V

\* -3V with a pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
$I_{LI}$	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	±1	μA	
$I_{LO}$	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{OUT} = 0 \sim V_{DD}$	-	-	±1	μA	
$I_{OH}$	Output High Current	$V_{OH} = 2.4V$	-4	-	-	mA	
$I_{OL}$	Output Low Current	$V_{OL} = 0.4V$	8	-	-	mA	
$I_{DDO}$	Operating Current	$t_{cycle} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = $V_{IH}/V_{IL}$	-15	-	-	120	mA
			-20	-	-	120	
			-25	-	-	120	
			-35	-	-	100	
$I_{DDS1}$	Standby Current	$t_{cycle} = \text{Min cycle}$ $\overline{CE} = V_{IH}$ Other Inputs = $V_{IH}/V_{IL}$	-15	-	-	20	mA
			-20	-	-		
			-25	-	-		
			-35	-	-		
$I_{DDS2}$		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	-	-	1		

## Capacitance\* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

\*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C<sup>(1)</sup>, V<sub>DD</sub> = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55465AP/AJ-15		TC55465AP/AJ-20		TC55465AP/AJ-25		TC55465AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t <sub>ACC</sub>	Address Access Time	—	15	—	20	—	25	—	35	
t <sub>CO</sub>	$\overline{CE}$ Access Time	—	15	—	20	—	25	—	35	
t <sub>OE</sub>	$\overline{OE}$ Access Time	—	8	—	10	—	12	—	15	
t <sub>OH</sub>	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	
t <sub>COE</sub>	Output Enable Time from $\overline{CE}$	5	—	5	—	5	—	5	—	
t <sub>COD</sub>	Output Disable Time from $\overline{CE}$	—	8	—	8	—	10	—	15	
t <sub>OEE</sub>	Output Enable Time from $\overline{OE}$	1	—	1	—	1	—	1	—	
t <sub>ODO</sub>	Output Disable Time from $\overline{OE}$	—	8	—	8	—	10	—	15	

Write Cycle

SYMBOL	PARAMETER	TC55465AP/AJ-15		TC55465AP/AJ-20		TC55465AP/AJ-25		TC55465AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t <sub>WP</sub>	Write Pulse Width	10	—	11	—	13	—	18	—	
t <sub>AW</sub>	Address Valid to End of Write	12	—	13	—	15	—	20	—	
t <sub>CW</sub>	Chip Enable to End of Write	12	—	13	—	15	—	20	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	8	—	10	—	12	—	15	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	
t <sub>OE<sub>W</sub></sub>	Output Enable Time from $\overline{WE}$	1	—	1	—	1	—	1	—	
t <sub>OD<sub>W</sub></sub>	Output Disable Time from $\overline{WE}$	—	8	—	8	—	10	—	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

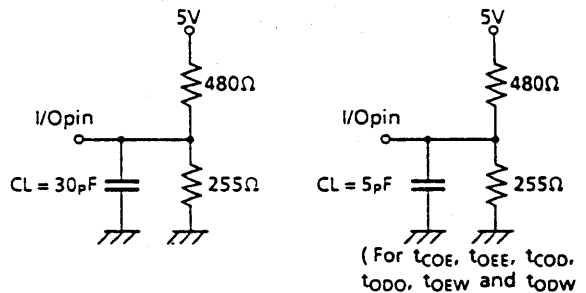
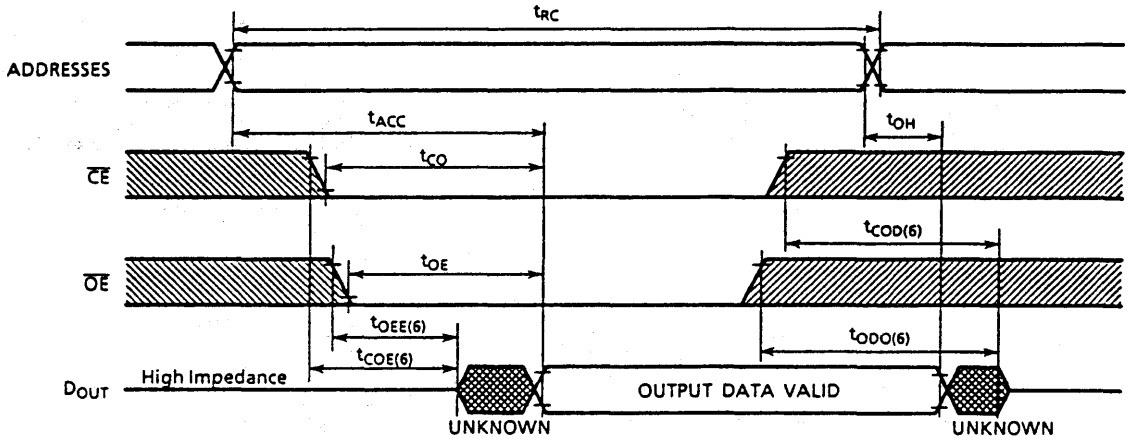


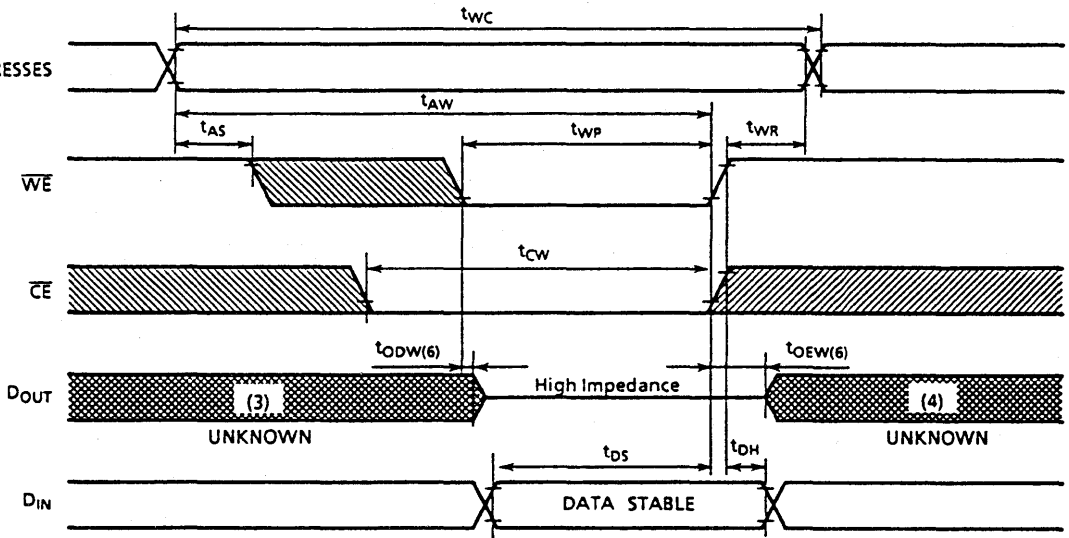
Figure 1.

Timing Waveforms

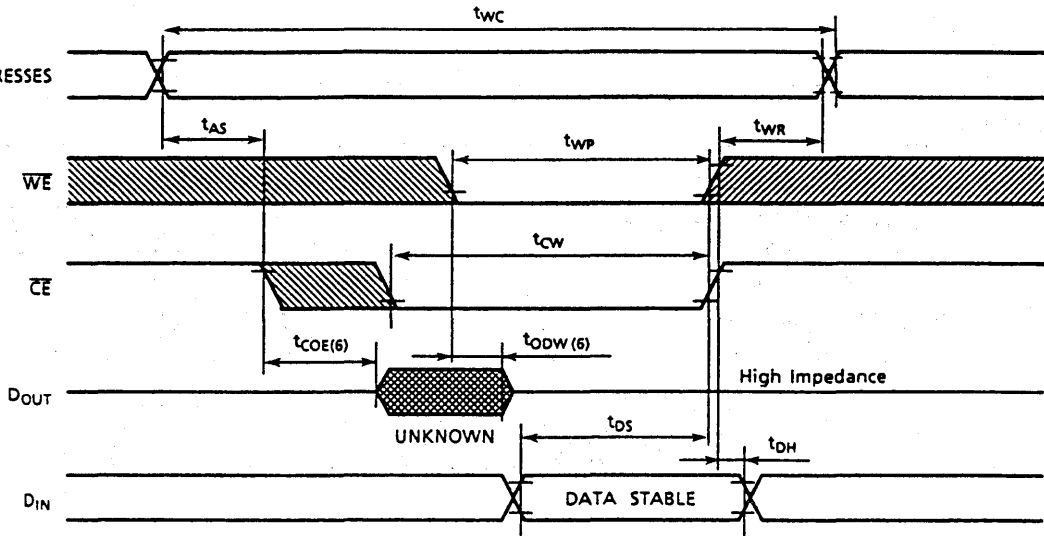
Read Cycle <sup>(2)</sup>



Write Cycle 1 <sup>(5)</sup> ( $\overline{WE}$  Controlled Write)



Write Cycle 2 <sup>(5)</sup> ( $\overline{CE}$  Controlled Write)



Notes:

1. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2.  $\overline{WE}$  is high for read cycles.
3. If the  $\overline{CE}$  low transition occurs coincident with or after the  $\overline{WE}$  low transition, outputs remain in a high impedance state.
4. If the  $\overline{CE}$  high transition occurs coincident with or prior to the  $\overline{WE}$  high transition, outputs remain in a high impedance state.
5. If  $\overline{OE}$  is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.  
 (A)  $t_{COE}$ ,  $t_{OEE}$ ,  $t_{OEw}$  . . . . . Output Enable Time  
 (B)  $t_{COD}$ ,  $t_{ODO}$ ,  $t_{ODw}$  . . . . . Output Disable Time

