TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P-55
TC5561P-70

DESCRIPTION

The TC5561P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 55ns/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P also features an automatic stand-by mode. When deselected by Chip Enable (CE), the operating current is reduced from 100mA to 100μA.

The TC5561P is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

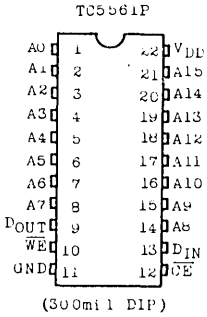
The TC5561P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

The TC5561P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

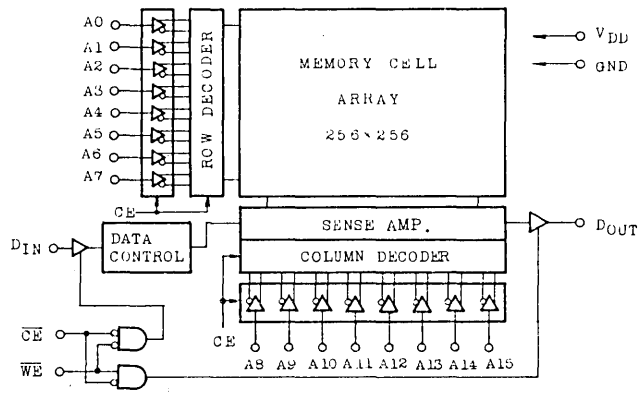
FEATURES

- Fast access time : TC5561P-55 55ns(MAX.)
  TC5561P-70 70ns(MAX.)
- Low power dissipation : Operation100mA(MAX.)
  Standby100μA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}	—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	−8	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0~V_{DD}	—	—	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V, t_{cycle}=Min cycle, $\overline{CE}$=V_{IL} Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}$=V_{IH}	—	—	2	mA
I_{DDS2}		$\overline{CE}$=V_{DD}−0.2V	—	—	100	μA

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO}	Chip Enable Access Time	—	55	—	70	
t_{COE}	Chip Enable to Output in Low-Z	5	—	5	—	
t_{COD}	Chip Disable to Output in High-Z	—	30	—	30	
t_{OH}	Output Data Hold Time	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	35	—	
t_{CW}	Chip Enable to End of Write	35	—	35	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	—	0	—	
t_{ODW}	$\overline{WE}$ to Output High-Z	—	30	—	30	
t_{DS}	Data Set up Time	35	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig.1

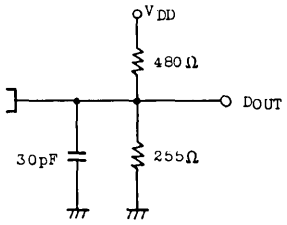
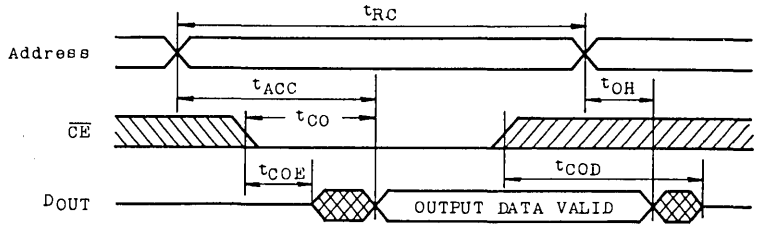


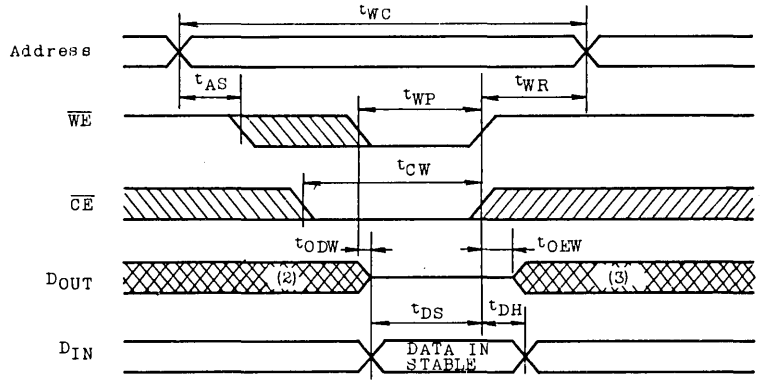
Fig.1 Output Load

TIMING WAVEFORMS

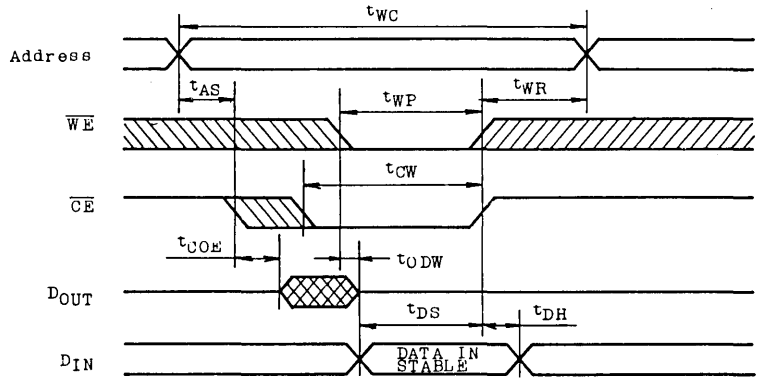
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

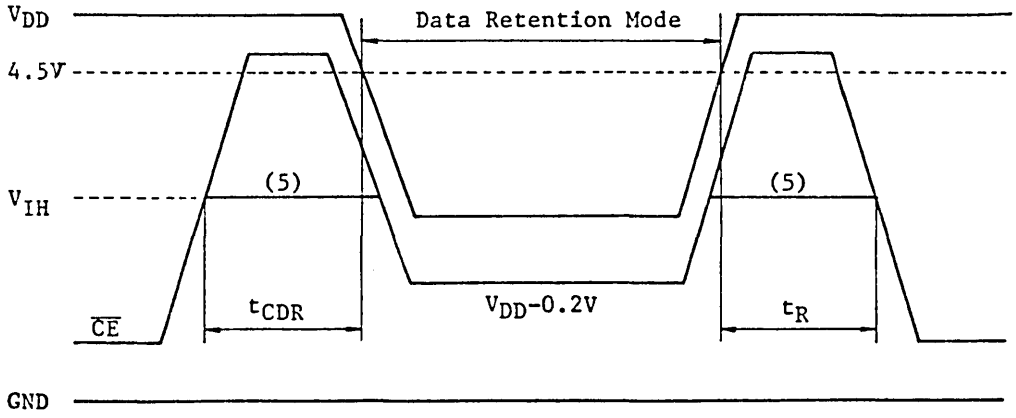


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

DATA RETENTION CHARACTERISTICS (Ta=−40~50°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	—	—	50	μA
		V_{DD}=5.5V	—	—	100	μA
t_{CDH}	Chip Deselection to Data Retntion Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs



5. If the V_{IH} of $\overline{CE}$, is 2.2V in operation, I_{DDS1} current flows the period that V_{DD} voltage is going down from 4.5V to 2.5V.

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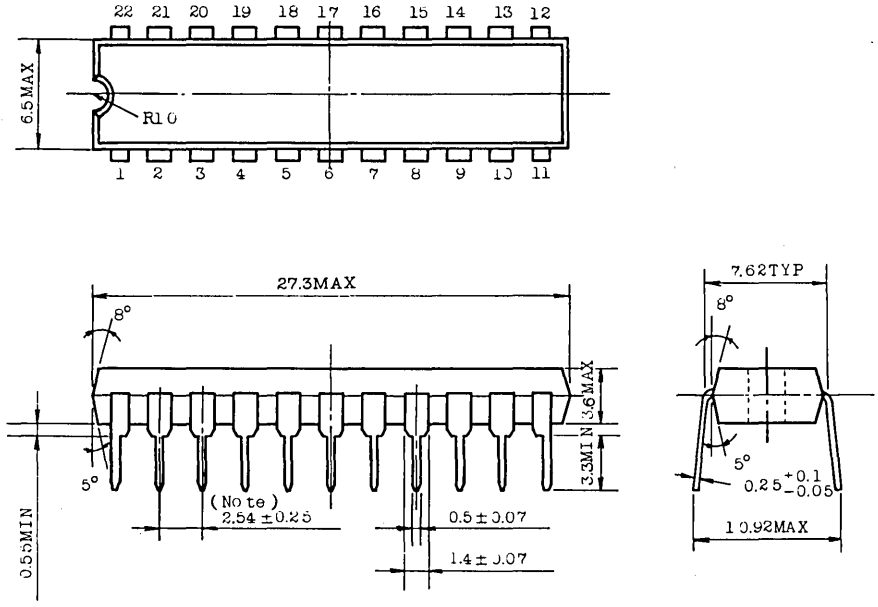
OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.