# TOSHIBA MOS MEMORY PRODUCT

**8,192 WORD × 8 BIT CMOS STATIC RAM**
**SILICON GATE CMOS**

**TC5565APL-10L, TC5565APL-12L, TC5565APL-15L**
**TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L**

## DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When $CE_2$ is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6$\mu$A typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE_1}$, $CE_2$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL/AFL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565APL/AFL is offered in a dual-in-line 28 pin standard plastic package.

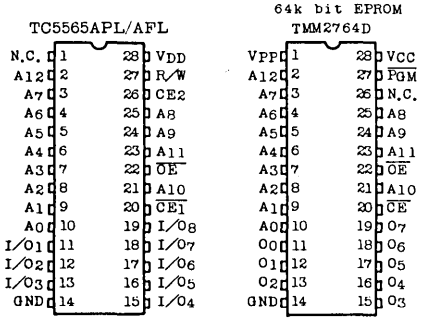
## FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 1$\mu$A (Max.) Ta=25°C
- Access Time
  TC5565APL/AFL-10L : 100ns (Max.)
  TC5565APL/AFL-12L : 120ns (Max.)
  TC5565APL/AFL-15L : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

| Package Type | Device Name |
|---|---|
| 600 mil DIP | TC5565APL |
| 300 mil DIP (Slim Package) | *TC5563APL |
| Flat Package(SOP) | TC5565AFL |

* : See TC5563APL Technical Date.

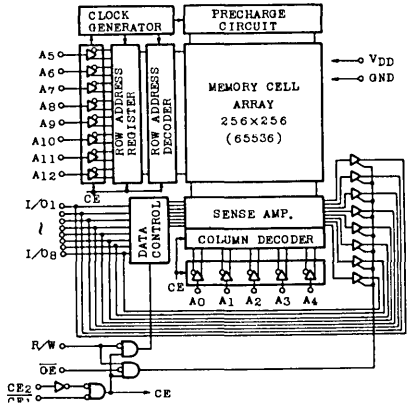
## PIN CONNECTION (TOP VIEW)




## NAMES

| | |
|---|---|
| $A_0$~$A_{12}$ | Address Inputs |
| R/W | Read/Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{CE_1}$, $CE_2$ | Chip Enable Inputs |
| $I/O_1$~$I/O_8$ | Data Input/Output |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |
| N. C. | No Connection |

## BLOCK DIAGRAM



## OPERATION MODE

| OPERATION MODE | $\overline{CE_1}$ | $CE_2$ | $\overline{OE}$ | R/W | $I/O_1 \sim I/O_8$ | POWER |
|---|---|---|---|---|---|---|
| Read | L | H | L | H | $D_{OUT}$ | $I_{DDO}$ |
| Write | L | H | * | L | $D_{IN}$ | $I_{DDO}$ |
| Output Deselect | L | H | H | H | High-Z | $I_{DDO}$ |
| Standby | H | * | * | * | High-Z | $I_{DDS}$ |
| | * | L | * | * | High-Z | $I_{DDS}$ |

* : H or L

## MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | −0.3~7.0 | V |
| $V_{IN}$ | Input Voltage | −0.3*~7.0 | V |
| $V_{I/O}$ | Input and Output Voltage | −0.5~$V_{DD}$+0.5 | V |
| $P_D$ | Power Dissipation | 1.0/0.6** | W |
| $T_{SOLDER}$ | Soldering Temperature | 260·10 | °C·Sec |
| $T_{STG}$ | Storage Temperature | −55~150 | °C |
| $T_{OPR}$ | Operating Temperature | 0~70 | °C |

* : −3.0V at Pulse width 50ns
** : Flat package

## D. C RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input Low Voltage | −0.3* | — | 0.8 | V |
| $V_{DH}$ | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

* : −3.0V at Pulse width 50ns

## D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, $V_{DD}$=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | $V_{IN}$=0~$V_{DD}$ | | — | — | ±1.0 | μA |
| $I_{OH}$ | Output High Current | $V_{OH}$=2.4V | | −1.0 | — | — | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$=0.4V | | 4.0 | — | — | mA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE_1}$=$V_{IH}$ or $CE_2$=$V_{IL}$ or R/W=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ $V_{OUT}$=0~$V_{DD}$ | | — | — | ±1.0 | μA |
| $I_{DDO1}$ | operating Current | $V_{DD}$=5.5V Iout=0mA $\overline{CE_1}$=$V_{IL}$ $CE_2$=$V_{IH}$ Other Input=$V_{IH}$/$V_{IL}$ | $t_{CYCLE}$=1μs | — | — | 10 | mA |
| | | | $t_{CYCLE}$=Min. cycle | — | — | 45 | |
| $I_{DDO2}$ | Operating Current | $V_{DD}$=5.5V $\overline{CE_1}$=0.2V $CE_2$=$V_{DD}$−0.2V Other Input Iout=0mA =$V_{DD}$−0.2V/0.2V | $t_{CYCLE}$=1μs | — | — | 5 | mA |
| | | | $t_{CYCLE}$=Min. cycle | — | — | 40 | |
| $I_{DDS1}$ | Standby Current | $\overline{CE_1}$=$V_{IH}$ or $CE_2$=$V_{IL}$ | | — | — | 3 | mA |
| *$I_{DDS2}$ | Standby Current | $\overline{CE_1}$=$V_{DD}$−0.2V or $CE_2$=0.2V | Ta=25°C | — | 0.6 | 1.0 | μA |
| | | | Ta=0~70°C | — | — | 30 | |

* : In standby mode with $\overline{CE_1}$≧$V_{DD}$−0.2V, these specification limits are guaranteed under the condition of $CE_2$≧$V_{DD}$−0.2V or $CE_2$≦0.2V.

## CAPACITANCE (Ta=25°C)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$=GND | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$=GND | 10 | pF |

Note : This parameter periodically sampled is not 100% tested.

## A. C. CHARACTERISTICS

(Ta=0~70°C, $V_{DD}$=5V±10%)

### Read Cycle

| SYMBOL | PARAMETER | TC5565APL-10L TC5565AFL-10L | | TC5565APL-12L TC5565AFL-12L | | TC5565APL-15L TC5565AFL-15L | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{RC}$ | Read Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| $t_{ACC}$ | Address Access Time | — | 100 | — | 120 | — | 150 | |
| $t_{CO1}$ | $\overline{CE1}$ Access Time | — | 100 | — | 120 | — | 150 | |
| $t_{CO2}$ | CE2 Access Time | — | 100 | — | 120 | — | 150 | |
| $t_{OE}$ | Output Enable to Output Valid | — | 50 | — | 60 | — | 70 | |
| $t_{COE}$ | Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z | 10 | — | 10 | — | 15 | — | |
| $t_{OEE}$ | Output Enable to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| $t_{OD}$ | Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z | — | 35 | — | 40 | — | 50 | |
| $t_{ODO}$ | Output Enable to Output in High-Z | — | 35 | — | 40 | — | 50 | |
| $t_{OH}$ | Output Data Hold Time | 20 | — | 20 | — | 20 | — | |

### Write Cycle

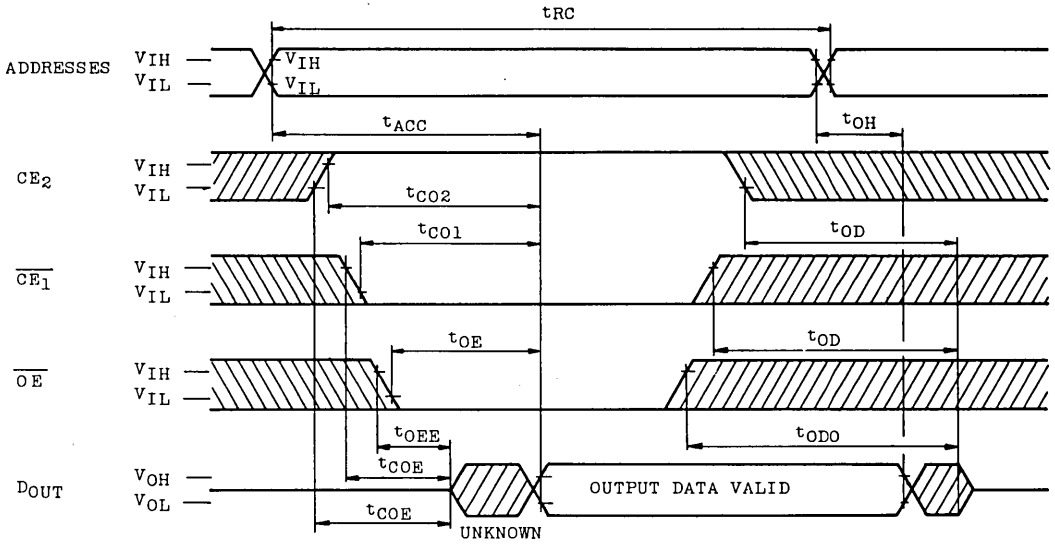
| SYMBOL | PARAMETER | TC5565APL-10L TC5565AFL-10L | | TC5565APL-12L TC5565AFL-12L | | TC5565APL-15L TC5565AFL-15L | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{WC}$ | Write Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| $t_{WP}$ | Write Pulse Width | 60 | — | 70 | — | 90 | — | |
| $t_{CW}$ | Chip Selection to End of Write | 80 | — | 85 | — | 100 | — | |
| $t_{AS}$ | Address Set up Time | 0 | — | 0 | — | 0 | — | |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| $t_{ODW}$ | R/W to Output in High-Z | — | 35 | — | 40 | — | 50 | |
| $t_{OEW}$ | R/W to Output in Low-Z | 5 | — | 5 | — | 10 | — | |
| $t_{DS}$ | Data Set Up Time | 40 | — | 50 | — | 60 | — | |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | |

## A. C. TEST CONDITIONS

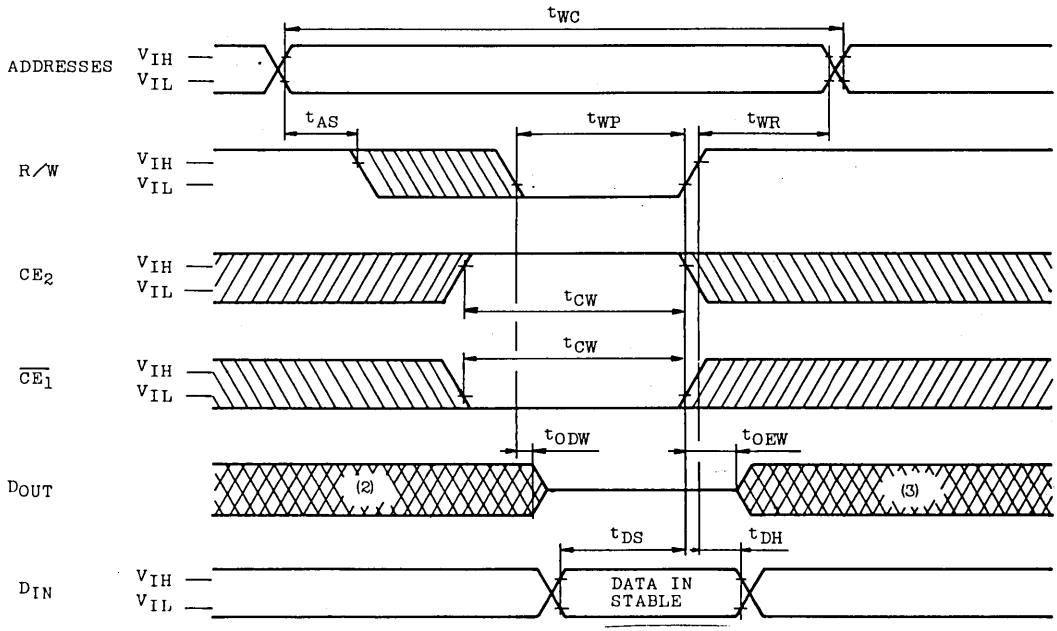
| | |
|---|---|
| Output Load | : 100pF+1 TTL Gate |
| Input Pulse Level | : 0.6V, 2.4V |
| Timing Measurement Reference Level | $V_{IN}$ : 0.8V, 2.2V<br>$V_{OUT}$ : 0.8V, 2.2V |
| $t_r$, $t_f$ | : 5ns |

## TIMING WAVEFORMS

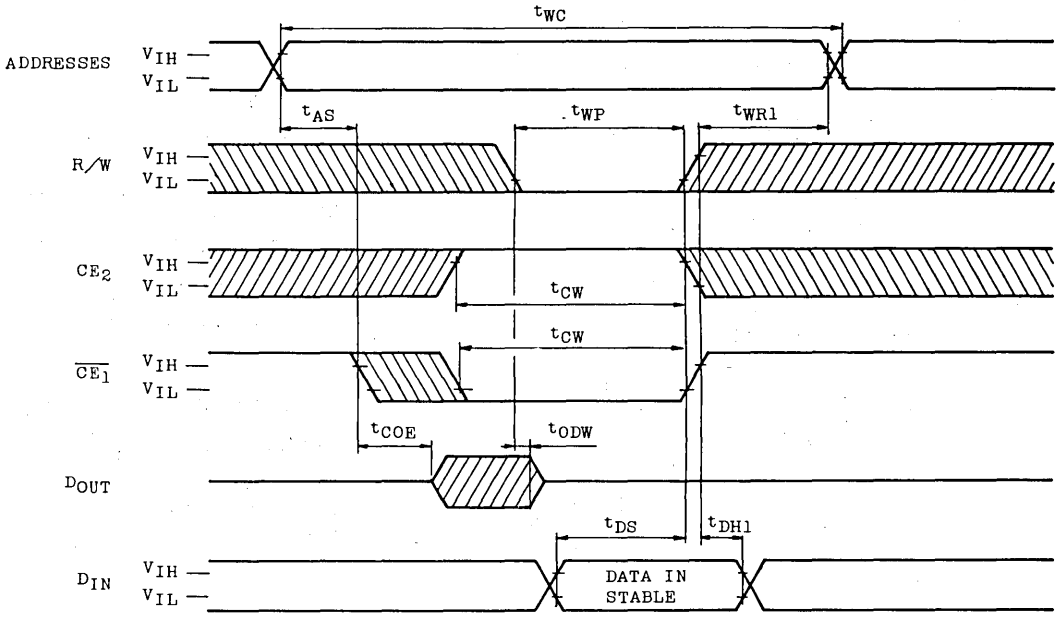
- READ CYCLE (1)



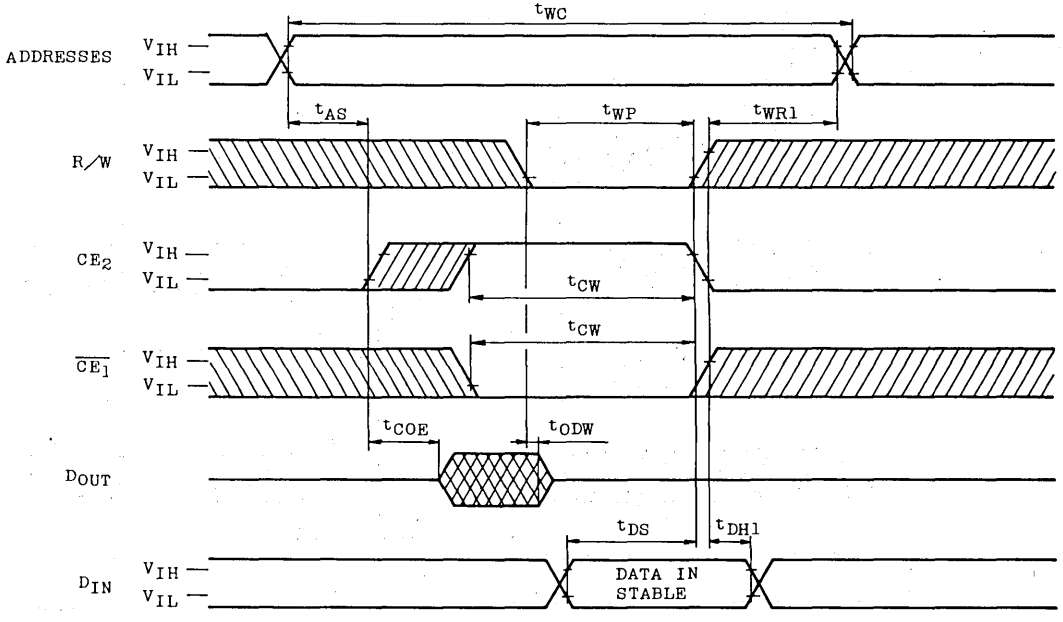

- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)




- WRITE CYCLE 3 (4) ($CE_2$ Controlled Write)



Note :

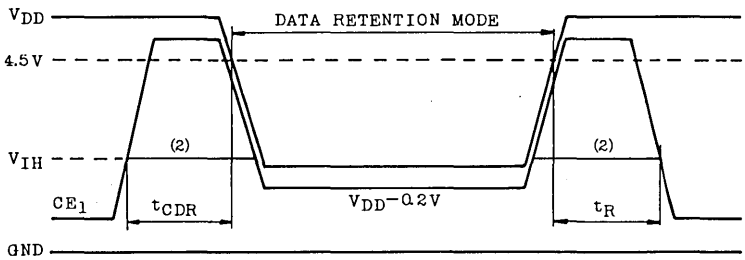
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition of $CE_2$ High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or $CE_2$ Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

## DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

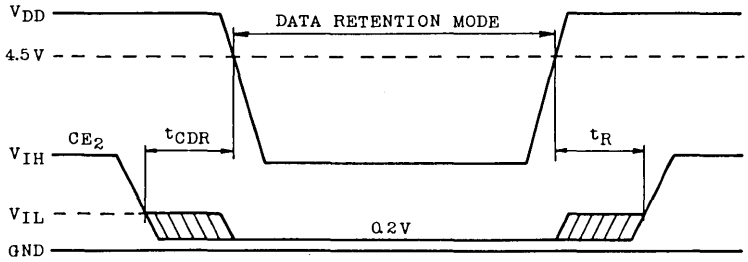
| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DH}$ | Data Retention Supply Voltage | | 2.0 | — | 5.5 | V |
| $I_{DDS2}$ | Stand by Supply Current | $V_{DD}$=3.0V | — | — | 15 | μA |
| | | $V_{DD}$=5.5V | — | — | 30 | |
| $t_{CDR}$ | Chip Deselection to Data Retention Mode | | 0 | — | — | μs |
| $t_R$ | Recovery Time | | $t_{RC}$* | — | — | ns |

* : Read cycle time.

- $\overline{CE_1}$ Controlled Data Retention Mode (1)




- $CE_2$ Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode. minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the $V_{IH}$ of $\overline{CE_1}$ is 2.2V in operation, $I_{DDS1}$ current flows during the period that the $V_{DD}$ voltage is going down from 4.5V to 2.4V.
3. In $CE_2$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

## DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on $V_{DD}$/GND lines. Thus the use of about 0.1$\mu$F decoupling capacitor for every device is recommended to eliminate such noise.

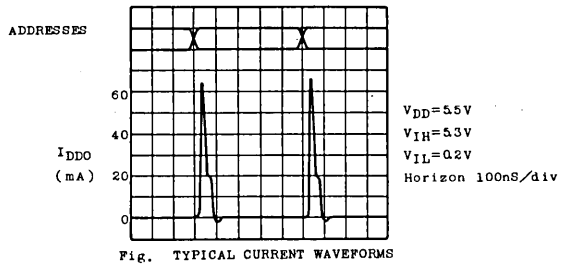
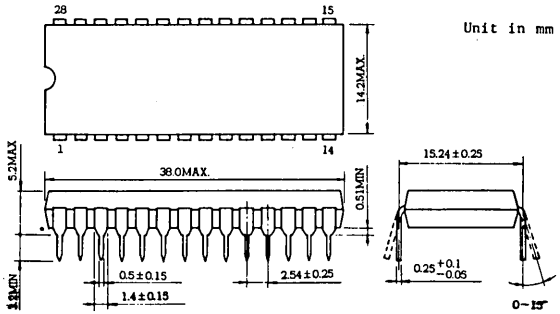


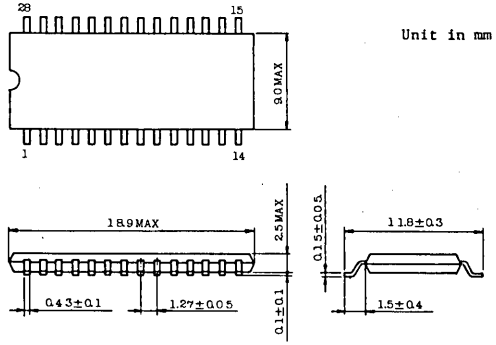

Fig. TYPICAL CURRENT WAVEFORMS

● DIP 28 PIN OUTLINE DRAWING (6D28A-P)




Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

● MFP 28 PIN OUTLINE DRAWING (F28GC-P)




Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.