## SILICON GATE CMOS

## 8,192 WORD x 9 BIT CMOS STATIC RAM

### Description

The TC5589P/J is a 73,728 bit high speed CMOS static random access memory organized as 8,192 words by 9 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC5589P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, CE2) and has an output enable input ($\overline{OE}$) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

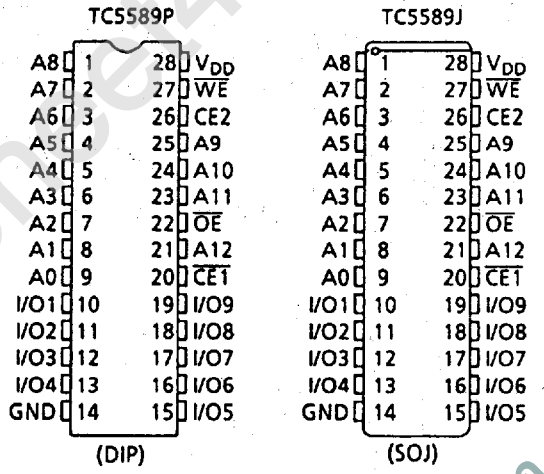
The TC5589P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC5589P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

### Features

- Fast access time
  - TC5589P/J-15 15ns (max.)
  - TC5589P/J-20 20ns (max.)
  - TC5589P/J-25 25ns (max.)
  - TC5589P/J-35 35ns (max.)
- Low power dissipation
  - Operation:
  - TC5589P/J-15 135mA (max.)
  - TC5589P/J-20 115mA (max.)
  - TC5589P/J-25 115mA (max.)
  - TC5589P/J-35 115mA (max.)
  - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Package:
  - TC5589P: DIP28-P-300B
  - TC5589J: SOJ28-P-300A

### Pin Connection (Top View)




### Pin Names

| | |
|---|---|
| A0 ~ A12 | Address Inputs |
| I/O1 ~ I/O9 | Data Inputs/Outputs |
| $\overline{CE1}$, CE2 | Chip Enable Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |

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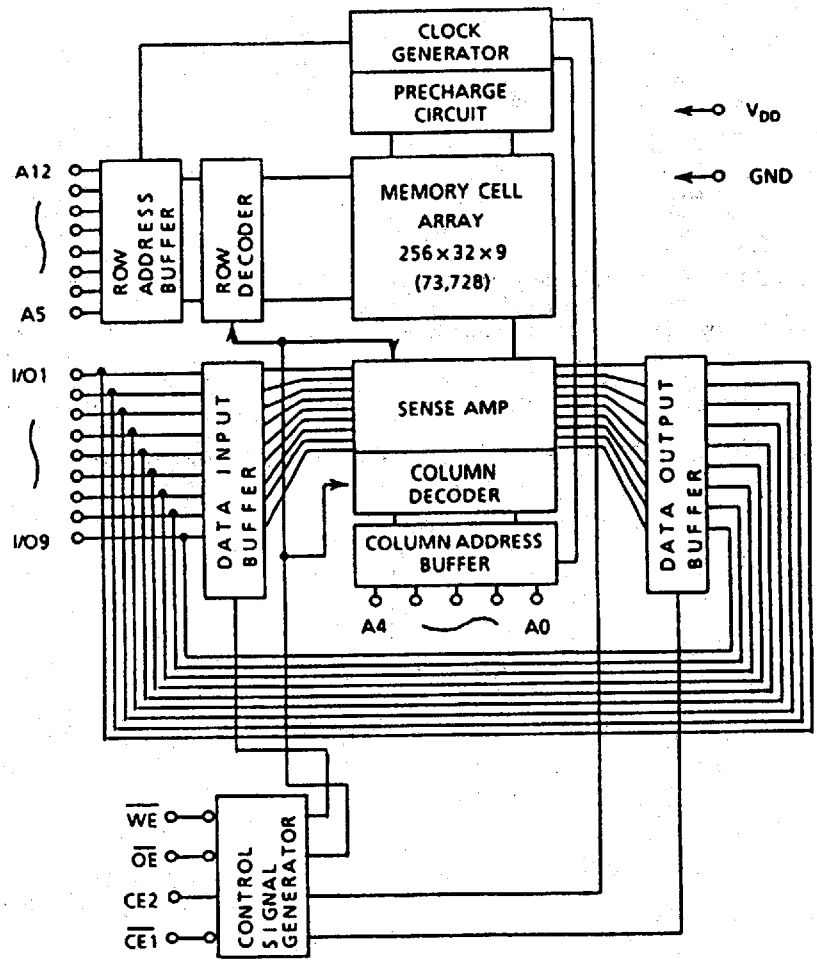
## Block Diagram




## Maximum Ratings

| SYMBOL | ITEM | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -0.5 ~ 7.0 | V |
| $V_{IN}$ | Input Voltage | -2.0 ~ 7.0 | V |
| $V_{I/O}$ | Input/Output Voltage | -0.5 ~ $V_{DD}$ + 0.5 | V |
| $P_D$ | Power Dissipation | 1.0 | W |
| $T_{SOLDER}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |
| $T_{STRG}$ | Storage Temperature | -65 ~ 150 | °C |
| $T_{OPR}$ | Operating Temperature | -10 ~ 85 | °C |



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## DC Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | – | $V_{DD}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage | -0.5* | – | 0.8 | V |

* -3V with a pulse width of 10ns

## DC Characteristics (Ta = 0 ~ 70°C, $V_{DD}$ = 5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 ~ $V_{DD}$ | | – | – | ±1 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ or $\overline{WE}$ = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = 0 ~ $V_{DD}$ | | – | – | ±1 | μA |
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | | -4 | – | – | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | | 8 | – | – | mA |
| $I_{DDO}$ | Operating Current | $V_{DD}$ = 5.5V $t_{cycle}$ = Min cycle<br>$\overline{CE1}$ = $V_{IL}$ and CE2 = $V_{IH}$<br>Other Inputs = $V_{IH}$/$V_{IL}$<br>$I_{OUT}$ = 0mA | -15 | – | – | 135 | mA |
| | | | -20 | – | – | 115 | |
| | | | -25 | | | | |
| | | | -35 | | | | |
| $I_{DDS1}$ | Standby Current | $V_{DD}$ = 5.5V $t_{cycle}$ = Min cycle<br>$\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$<br>Other Inputs = $V_{IH}$/$V_{IL}$ | | – | – | 25 | mA |
| $I_{DDS2}$* | | $\overline{CE1}$ = $V_{DD}$ - 0.2V or CE2 = 0.2V<br>Other Inputs = $V_{DD}$ - 0.2V or 0.2V | | – | – | 1 | |

* If $\overline{CE1}$ ≥ $V_{DD}$ - 0.2V, the specified limits are guaranteed under the condition CE2 ≥ $V_{DD}$ - 0.2V or CE2 ≤ 0.2V.

## Capacitance* (Ta = 25°C, f = 1.0MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = GND | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = GND | 7 | pF |

*This parameter is periodically sampled and is not 100% tested.



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## AC Characteristics (Ta = 0 ~ 70°C[1], $V_{DD}$ = 5V±10%)

### Read Cycle

| SYMBOL | PARAMETER | TC5589P/J-15 | | TC5589P/J-20 | | TC5589P/J-25 | | TC5589P/J-35 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{RC}$ | Read Cycle Time | 15 | – | 20 | – | 25 | – | 35 | – | ns |
| $t_{ACC}$ | Address Access Time | – | 15 | – | 20 | – | 25 | – | 35 | |
| $t_{CO1}$ | $\overline{CE1}$ Access Time | – | 15 | – | 20 | – | 25 | – | 35 | |
| $t_{CO2}$ | CE2 Access Time | – | 15 | – | 20 | – | 25 | – | 35 | |
| $t_{OE}$ | $\overline{OE}$ Access Time | – | 9 | – | 10 | – | 12 | – | 12 | |
| $t_{OH}$ | Output Data Hold Time from Address Change | 5 | – | 5 | – | 5 | – | 5 | – | |
| $t_{COE}$ | Output Enable Time from $\overline{CE1}$ or CE2 | 5 | – | 5 | – | 5 | – | 5 | – | |
| $t_{COD}$ | Output Disable Time from $\overline{CE1}$ or CE2 | – | 6 | – | 6 | – | 6 | – | 6 | |
| $t_{OEE}$ | Output Enable Time from $\overline{OE}$ | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{ODO}$ | Output Disable Time from $\overline{OE}$ | – | 5 | – | 5 | – | 5 | – | 5 | |
| $t_{PU}$ | Chip Selection to Power Up Time | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{PD}$ | Chip Deselection to Power Down Time | – | 15 | – | 20 | – | 25 | – | 35 | |

### Write Cycle

| SYMBOL | PARAMETER | TC5589P/J-15 | | TC5589P/J-20 | | TC5589P/J-25 | | TC5589P/J-35 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{WC}$ | Write Cycle Time | 15 | – | 20 | – | 25 | – | 35 | – | ns |
| $t_{CW}$ | Chip Enable to End of Write | 12 | – | 13 | – | 15 | – | 15 | – | |
| $t_{AS}$ | Address Setup Time | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{WP}$ | Write Pulse Width | 12 | – | 13 | – | 15 | – | 15 | – | |
| $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{DS}$ | Data Setup Time | 9 | – | 10 | – | 12 | – | 12 | – | |
| $t_{DH}$ | Data Hold Time | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{OEW}$ | Output Enable Time from $\overline{WE}$ | 0 | – | 0 | – | 0 | – | 0 | – | |
| $t_{ODW}$ | Output Disable Time from $\overline{WE}$ | – | 6 | – | 6 | – | 6 | – | 6 | |

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 3.0V/0.0V |
| Input Pulse Rise and Fall Time | 3ns |
| Input Timing Measurement Reference Levels | 2.2V/0.8V |
| Output Timing Measurement Reference Levels | 2.0V/0.8V |
| Output Load | Fig. 1 |

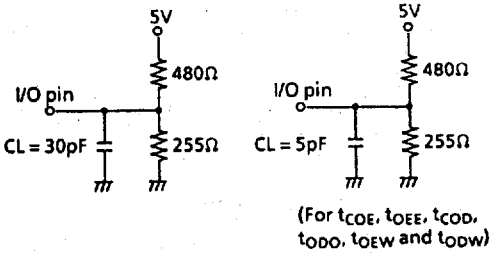


Figure 1.



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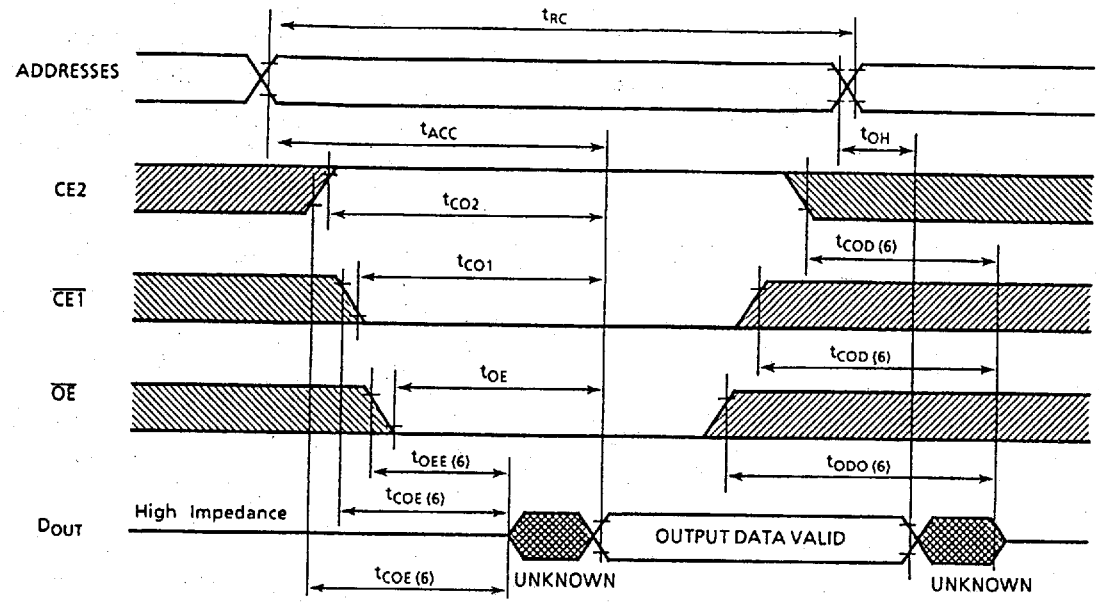
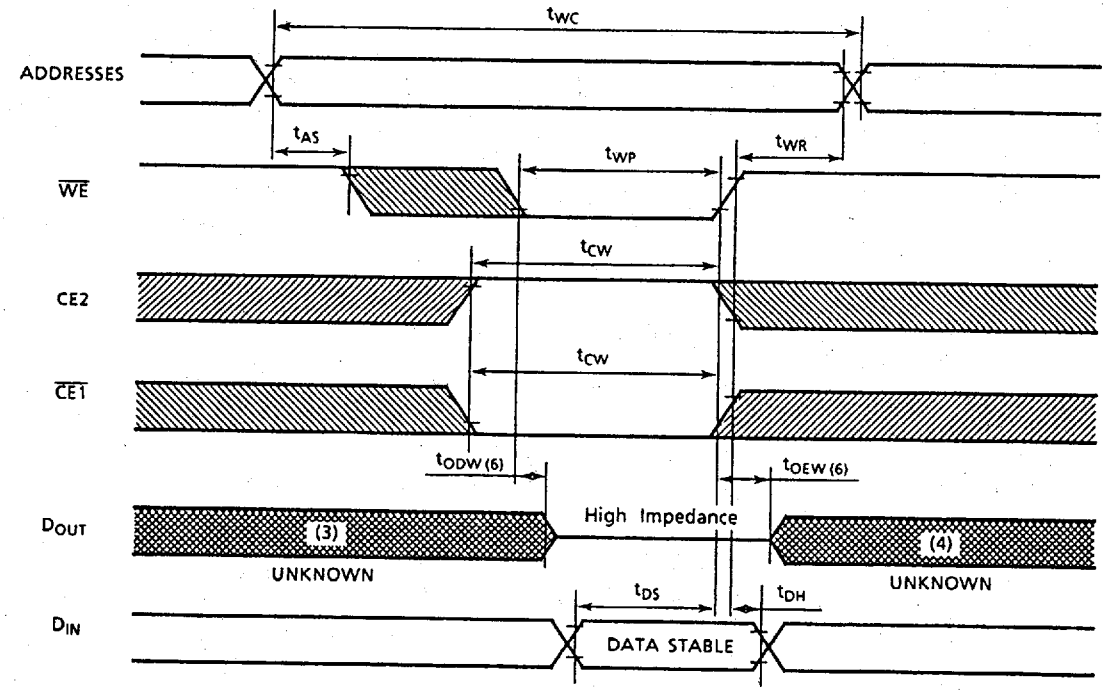
## Timing Waveforms

### Read Cycle (2)




### Write Cycle 1 (5) ($\overline{WE}$ Controlled Write)



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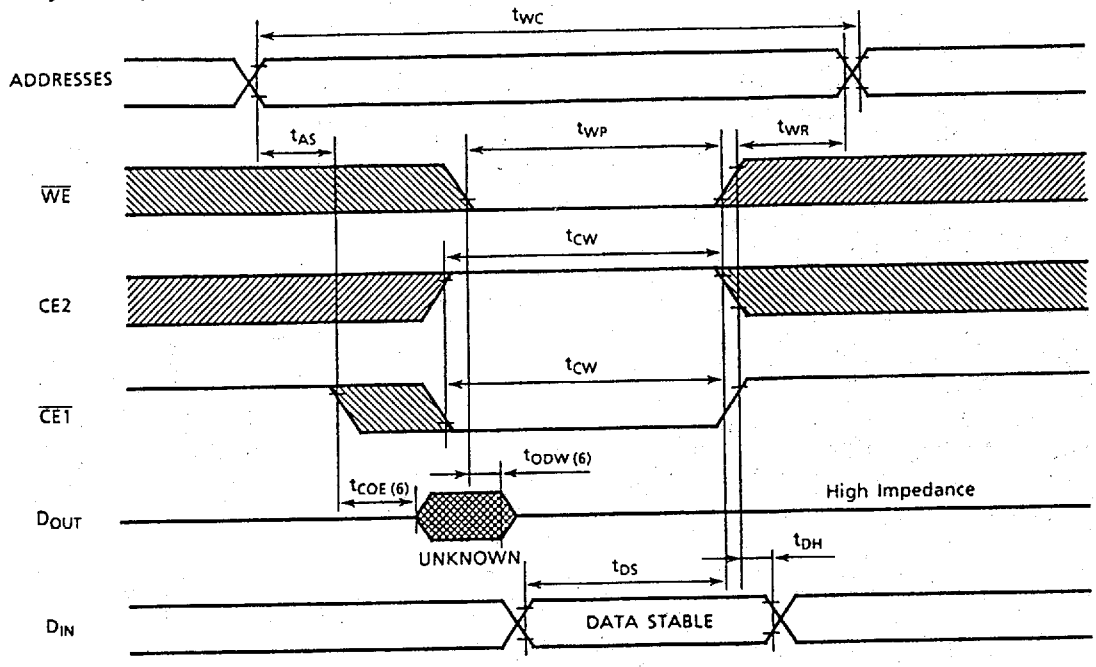
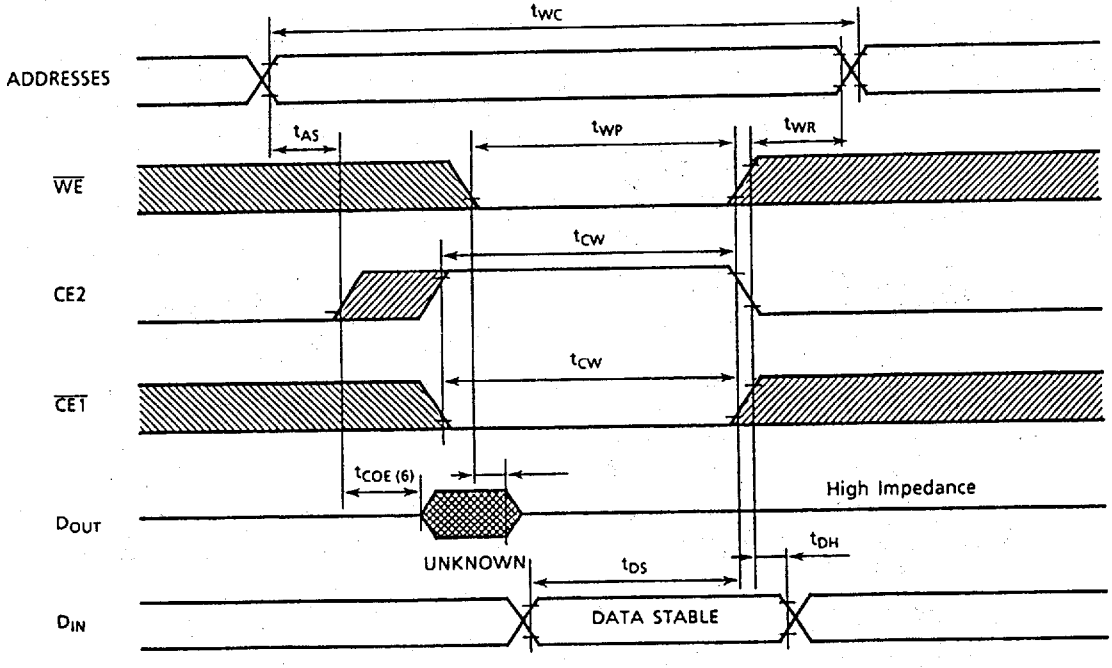
## Write Cycle 2 [5] ($\overline{CE1}$ Controlled Write)




## Write Cycle 3 [5] (CE2 Controlled Write)



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Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

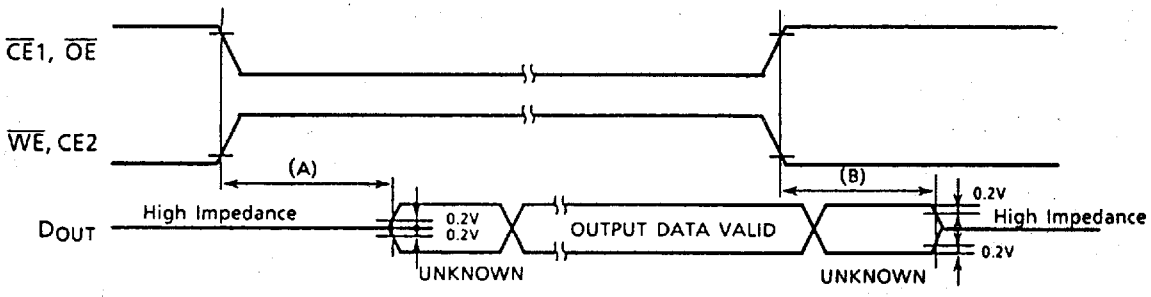
2. $\overline{WE}$ is high for read cycles.

3. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

4. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the $\overline{WE}$ high transition, outputs remain in a high impedance state.

5. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.
   (A) $t_{COE}$, $t_{OEE}$, $t_{OEW}$ . . . . . Output Enable Time
   (B) $t_{COD}$, $t_{ODO}$, $t_{ODW}$ . . . . Output Disable Time



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