16,384 WORD × 4 BIT BiCMOS STATIC RAM

DESCRIPTION

The TC55B417P/J is a 65,536 bits high speed static random access memory organized as 16,384 words by 4 bits using BiCMOS technology, and operated from a single 5 - volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 10ns / 12ns and maximum operating current of 120mA at minimum cycle time.

The TC55B417P/J also features an automatic stand - by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 10mA.

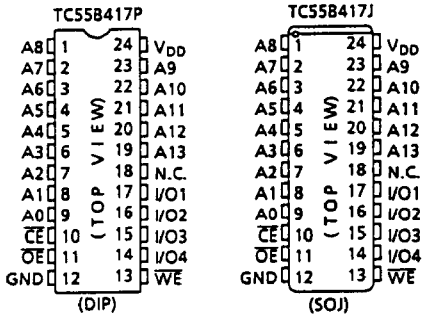
The TC55B417P/J is suitable for use in cache memory where high speed/high density are required.

The TC55B417P/J is packaged in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

FEATURES

- Fast access time:
  - TC55B417P/J-10 — 10ns (MAX.)
  - TC55B417P/J-12 — 12ns (MAX.)
- Low power dissipation:
  - Operation — 120mA (MAX.)
  - Standby — 10mA (MAX.)
- Fully static operation
- 5V single power supply : −10 : 5V±5% / −12 : 5V±10%
- Directly TTL compatible : All Inputs and Outputs
- Output buffer control : $\overline{OE}$
- Package : TC55B417P : DIP24-P-300B
  TC55B417J : SOJ24-P-300A

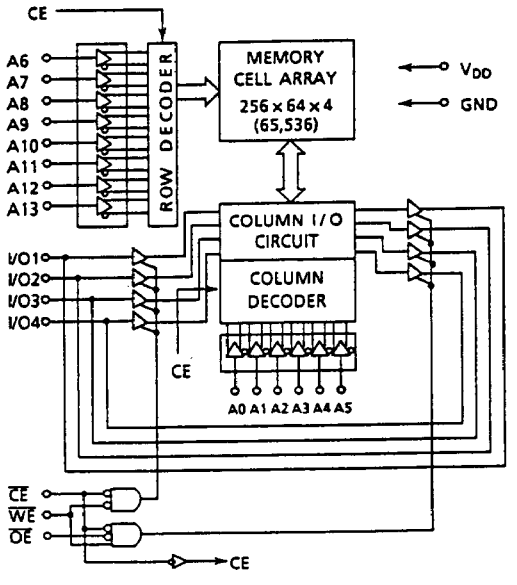
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+ 5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	850	mW
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−10	4.75	5.0	5.25	V
		−12	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		−0.5*	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −10 : V_{DD} = 5V ± 5% / −12 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}			−	−	±10	μA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL} Iout = 0mA Other Inputs = V_{IH} / V_{IL}	V_{DD} = 5.25V	−10	−	−	120	mA
			V_{DD} = 5.5V	−12				
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} / V_{IL}	V_{DD} = 5.25V	−10	−	−	30	mA
			V_{DD} = 5.5V	−12				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V			−	−	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (4), -10 : V_{DD} = 5V ± 5% / -12 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	-	12	-	ns
t_{ACC}	Address Access Time	-	10	-	12	
t_{CO}	Chip Enable Access Time	-	10	-	12	
t_{OE}	Output Enable Access Time	-	6	-	7	
t_{COE}	Output Enable Time from $\overline{CE}$	3	-	3	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	5	-	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	-	1	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	5	-	6	
t_{OH}	Output Data Hold Time from Address Change	3	-	3	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	10	-	12	

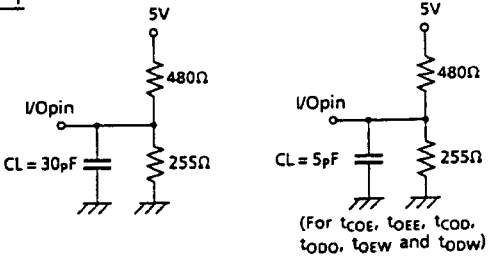
WRITE CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	-	12	-	ns
t_{WP}	Write Pulse Width	6	-	7	-	
t_{AW}	Address Valid to End of Write	7	-	8	-	
t_{CW}	Chip Enable to End of Write	7	-	8	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	5	-	6	
t_{DS}	Data Set Up Time	6	-	7	-	
t_{DH}	Data Hold Time	0	-	0	-	

AC TEST CONDITIONS

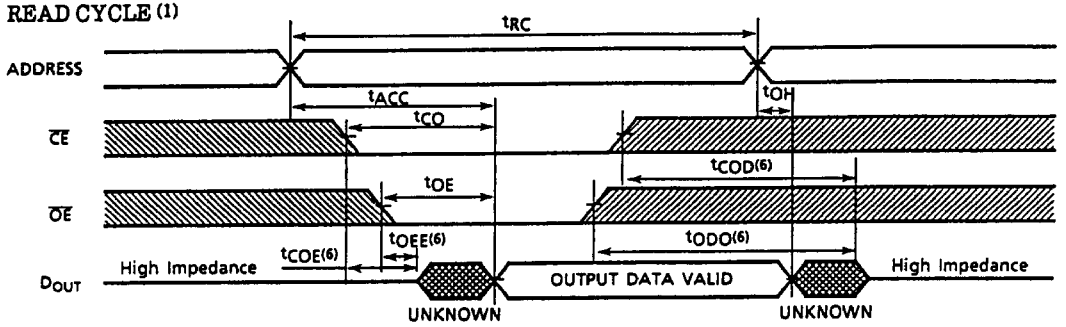
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

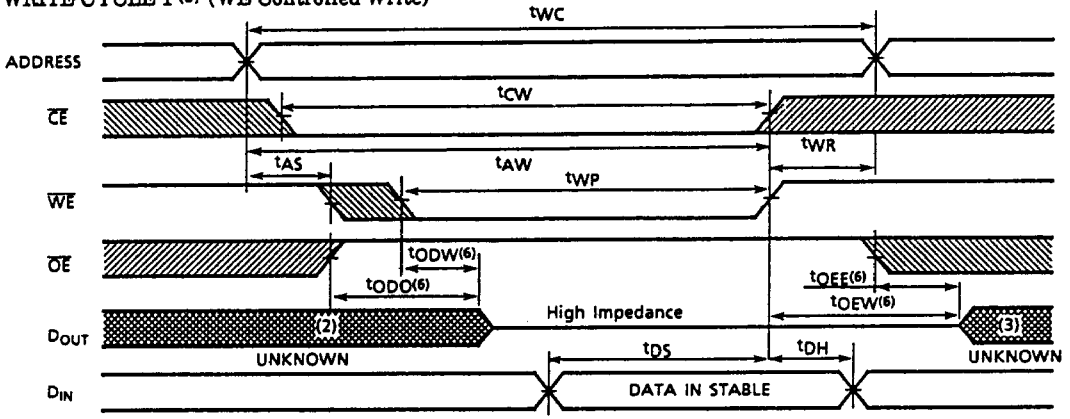


TIMING WAVEFORMS

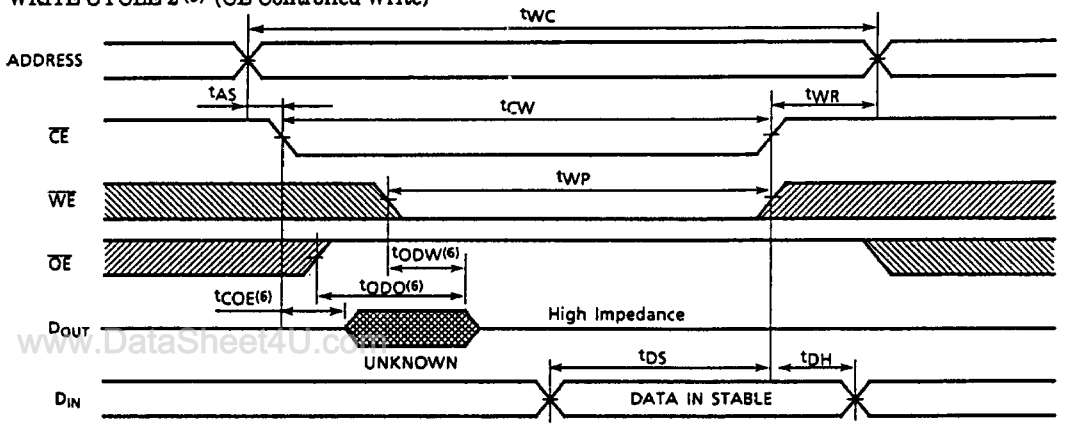
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

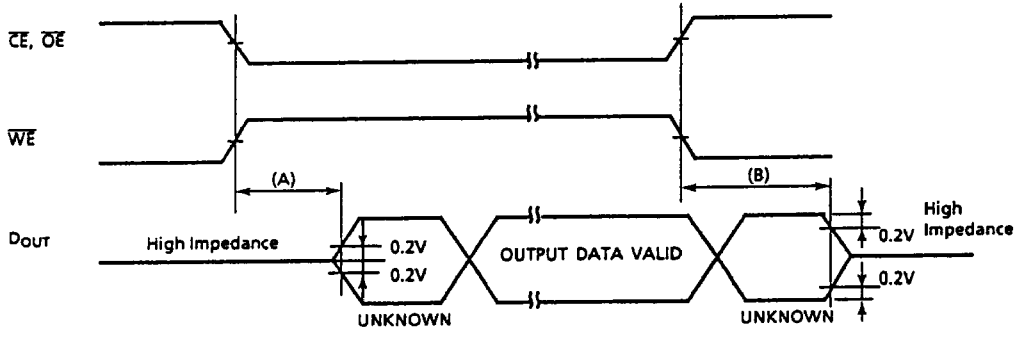
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

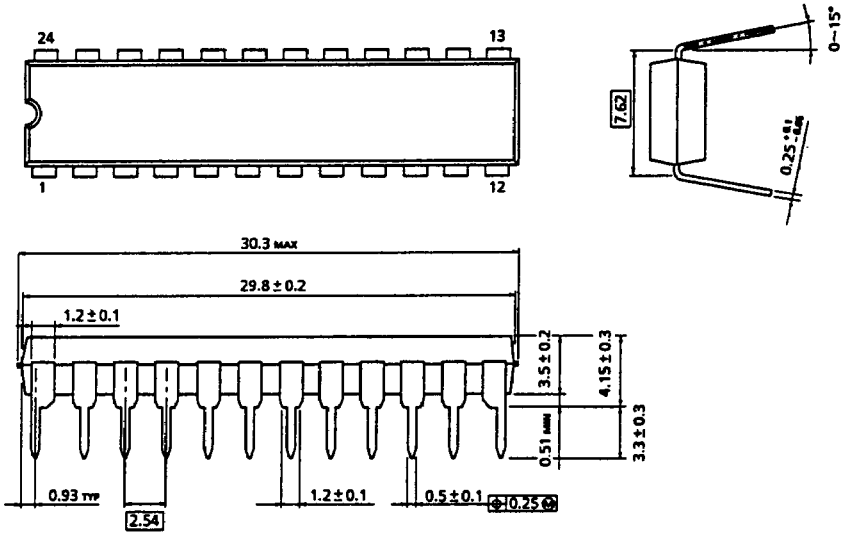
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24−P−300B)

Unit in mm

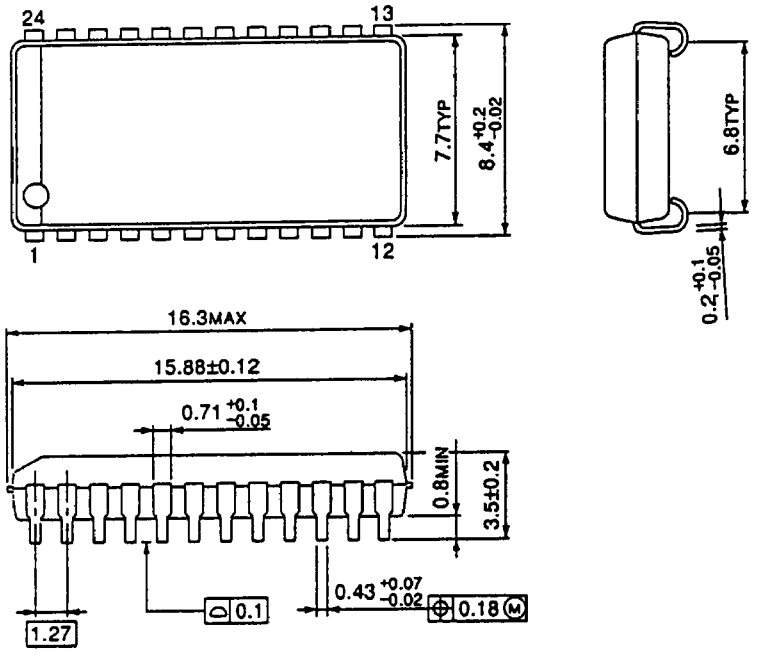


Weight : 1.72g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ24−P−300A)

Unit in mm



Weight : 0.72g (Typ.)