

SILICON GATE BiCMOS

65,536 WORD x 4 BIT BiCMOS STATIC RAM

Description

The TC55B464P/J is a 262,144 bit high speed BiCMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B464P/J features low power dissipation when the device is deselected using chip enable (\overline{CE}).

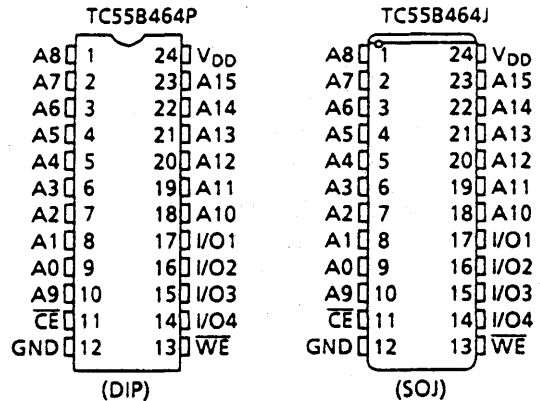
The TC55B464P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B464P/J is available in a 300mil width, 24-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B464P/J-10 10ns (max.)
 - TC55B464P/J-12 12ns (max.)
- Low power dissipation
 - Operation:
 - TC55B464P/J-10 140mA (max.)
 - TC55B464P/J-12 140mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Package:
 - TC55B464P: DIP24-P-300B
 - TC55B464J: SOJ24-P-300A

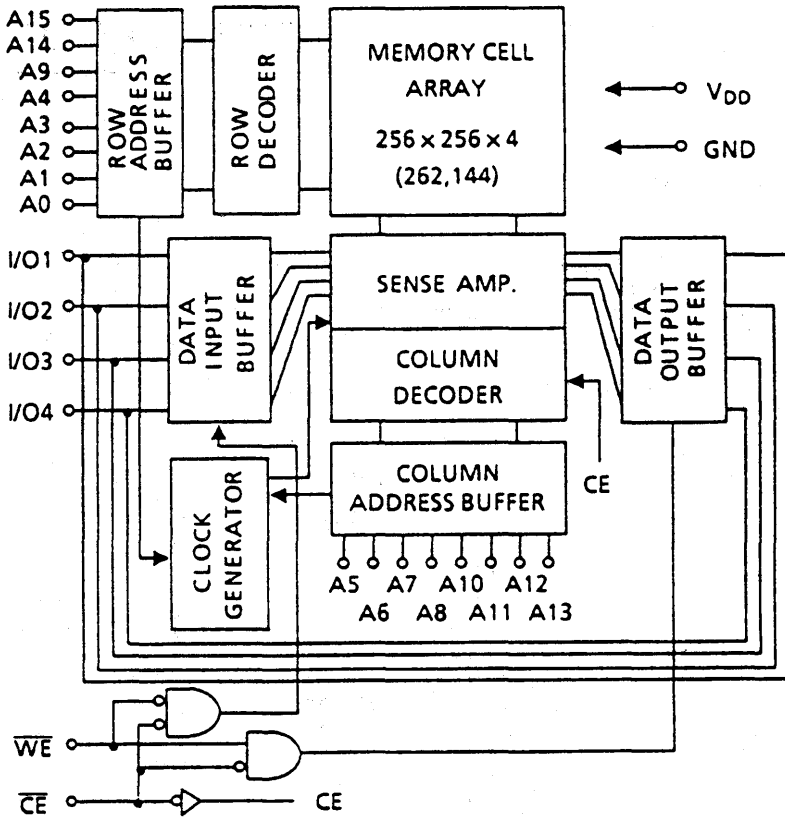
Pin Connection (Top View)



Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

Block Diagram



Operating Mode

MODE \ PIN	\overline{CE}	\overline{WE}	I/O1 ~ I/O4	POWER
Read	L	H	Output	I_{DDO}
Write	L	L	Input	I_{DDO}
Standby	H	*	High Impedance	I_{DSD}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	–	–	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	–	–	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL} , $I_{OUT} = 0\text{mA}$	–	–	140	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	–	–	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	–	–	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{ACC}	Address Access Time	—	10	—	12	
t_{CO}	\overline{CE} Access Time	—	10	—	12	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	
t_{COD}	Output Disable Time from \overline{CE}	—	5	—	6	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	

Write Cycle

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Enable to End of Write	7	—	8	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{AW}	Address Valid to End of Write	7	—	8	—	
t_{WP}	Write Pulse Width	6	—	7	—	
t_{WR}	Write Recovery Time	1	—	1	—	
t_{DS}	Data Setup Time	6	—	7	—	
t_{DH}	Data Hold Time	0	—	0	—	
$t_{OE\overline{W}}$	Output Enable Time from \overline{WE}	1	—	1	—	
$t_{OD\overline{W}}$	Output Disable Time from \overline{WE}	—	5	—	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

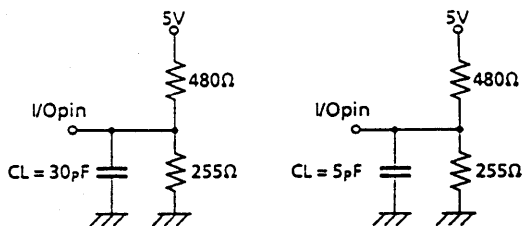
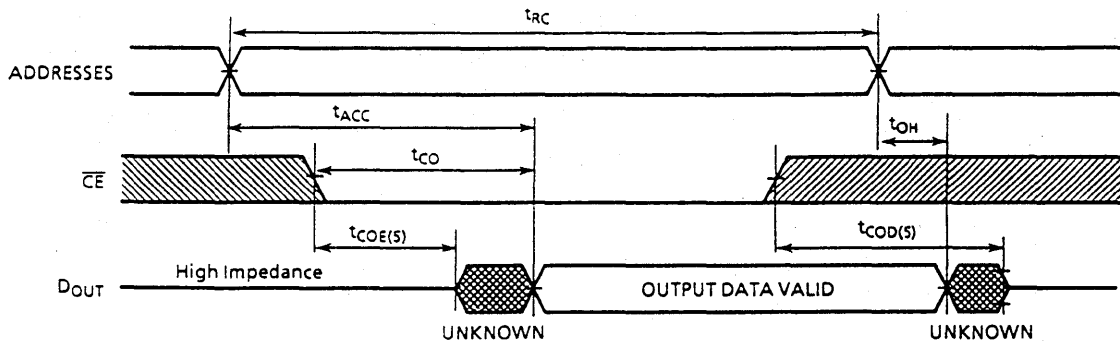
(For t_{COE} , t_{COD} , $t_{OE\overline{W}}$ and $t_{OD\overline{W}}$)

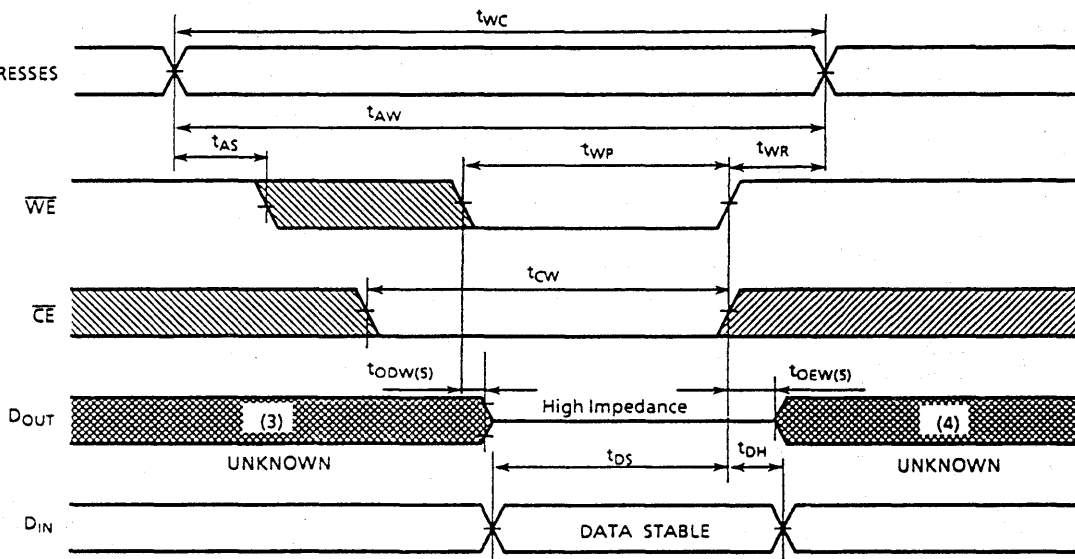
Figure 1.

Timing Waveforms

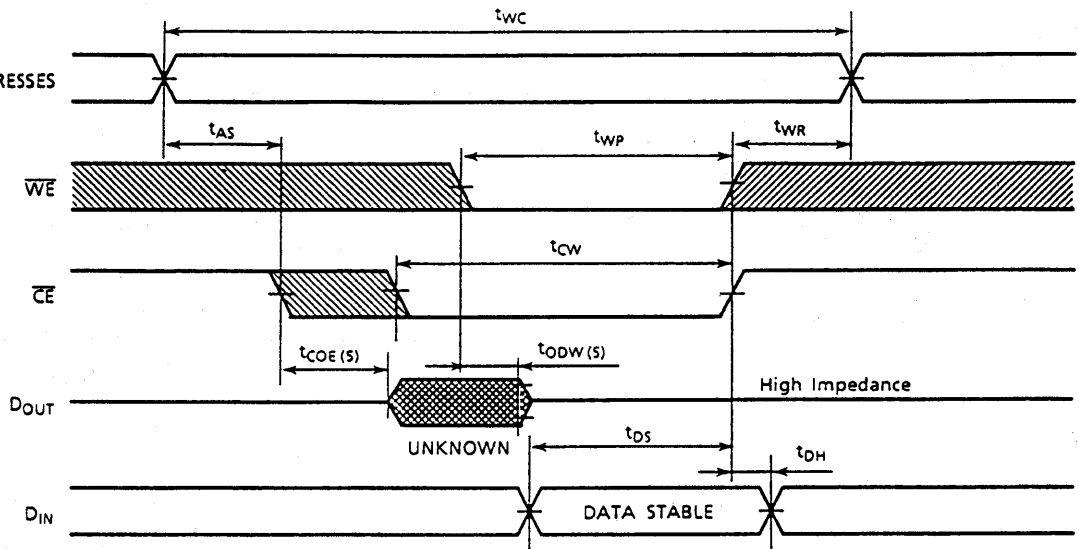
Read Cycle ⁽²⁾



Write Cycle 1 (\overline{WE} Controlled Write)



Write Cycle 2 ($\overline{\text{CE}}$ Controlled Write)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , $t_{OD\overline{W}}$ Output Disable Time

