# TOSHIBA

## 262,144 WORD x 4 BIT SYNCHRONOUS STATIC RAM
with Input Registers, Output Registers and Pass-Through Feature

### Description

The TC55BS4258J is a 1,048,576 bit synchronous static random access memory fabricated using BiCMOS technology and organized as 262,144 words by 4 bits. The TC55BS4258J has separate data inputs and outputs and a write-cycle pass-through feature.
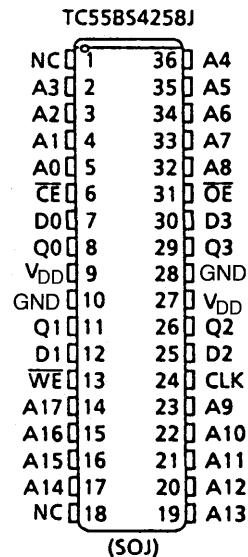
Designed for pipelined architectures, this device has internal input and output registers which latch on the positive edge of an external clock (CLK). All address, data, and control signals are latched. The setup and hold times for the inputs are 2ns and 1ns respectively. Synchronous SRAMs can lead to faster, more robust system operation by virtually eliminating the timing skew problems associated with conventional asynchronous SRAMs. For example, write operations are internally self-timed when initiated - eliminating the need for accurate write pulse generation and timing by the memory controller or microprocessor. A pass-through feature during write cycles allows the outputs to follow the inputs with a one clock cycle delay. For read cycles, data is available one clock cycle after the address is latched. All inputs and outputs are TTL compatible.

The TC55BS4258J is available in a 36-pin, 400mil SOJ package suitable for high density assembly.

### Features

- Fast cycle time
  - TC55BS4258J-10   10ns (max.)
  - TC55BS4258J-12   12ns (max.)
- Fast clock access time
  - TC55BS4258J-10    5ns (max.)
  - TC55BS4258J-12    6ns (max.)
- Input and output registers for synchronous operation
- Data pass-through for write cycles
- Single power supply: 5V ± 10%
- Separate data inputs and outputs
- Package: JEDEC standard pinout
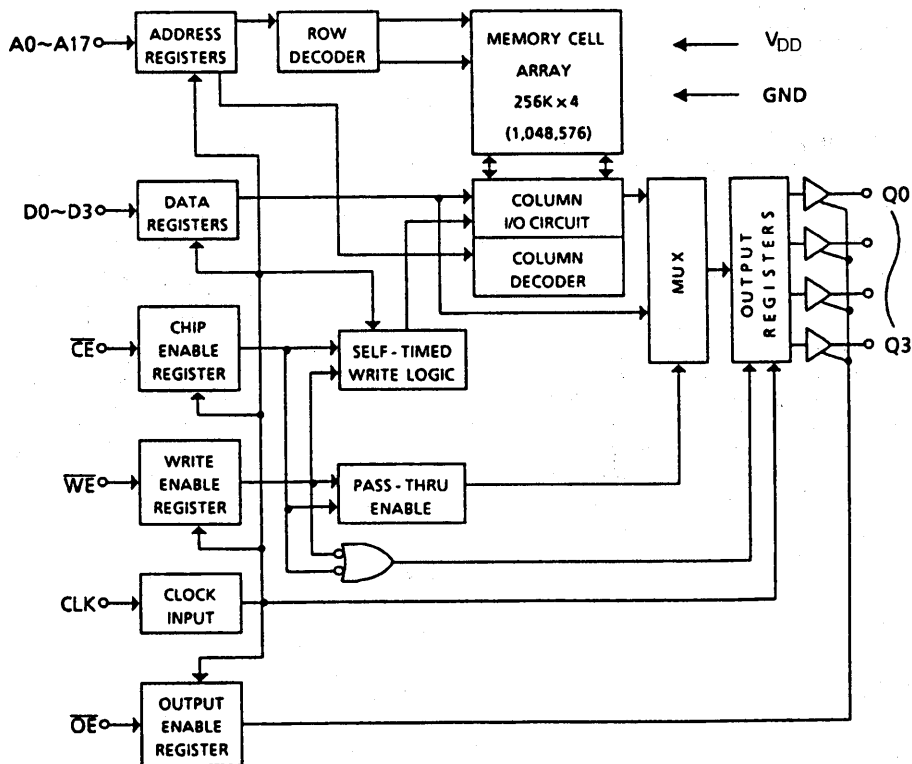  - 36-pin, 400mil SOJ: SOJ36-P-400

### Pin Names

| A0 ~ A17 | Address Inputs |
|----------|----------------|
| D0 ~ D3 | Data Inputs |
| Q0 ~ Q3 | Data Outputs |
| CLK | Clock Input |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{WE}$ | Write Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |
| NC | No Connection |

### Pin Connection (Top View)

TC55BS4258J

| | | | | |
|---|---|---|---|---|
| NC | 1 | | 36 | A4 |
| A3 | 2 | | 35 | A5 |
| A2 | 3 | | 34 | A6 |
| A1 | 4 | | 33 | A7 |
| A0 | 5 | | 32 | A8 |
| $\overline{CE}$ | 6 | | 31 | $\overline{OE}$ |
| D0 | 7 | | 30 | D3 |
| Q0 | 8 | | 29 | Q3 |
| $V_{DD}$ | 9 | | 28 | GND |
| GND | 10 | | 27 | $V_{DD}$ |
| Q1 | 11 | | 26 | Q2 |
| D1 | 12 | | 25 | D2 |
| $\overline{WE}$ | 13 | | 24 | CLK |
| A17 | 14 | | 23 | A9 |
| A16 | 15 | | 22 | A10 |
| A15 | 16 | | 21 | A11 |
| A14 | 17 | | 20 | A12 |
| NC | 18 | | 19 | A13 |

(SOJ)

## Block Diagram



## Operating Mode

| MODE | WE | CE | OE (next Cycle) | D | Q (next Cycle) |
|------|-----|-----|------|------|------|
| Write, Pass-Through | L | L | L | Valid | $D_{OUT}$ |
| Write | L | L | H | Valid | High - Z |
| Pass-Through | L | H | L | Valid | $D_{OUT}$ |
| Standby | L | H | H | * | High - Z |
| Read | H | L | L | * | $D_{OUT}$ |
| Output Disable | H | L | H | * | High - Z |
| Standby | H | H | * | * | High - Z |

* H or L

## Maximum Ratings

| SYMBOL | ITEM | RATING | UNIT |
|--------|------|--------|------|
| $V_{DD}$ | Power Supply Voltage | -0.5 ~ 7.0 | V |
| $V_{IN}$ | Input Voltage | -2.0 ~ 7.0 | V |
| $V_{OUT}$ | Output Voltage | -0.5 ~ $V_{DD}$ + 0.5 | V |
| $P_D$ | Power Dissipation | 1300 | mW |
| $T_{SOLDER}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |
| $T_{STRG}$ | Storage Temperature | -65~150 | °C |
| $T_{OPR}$ | Operating Temperature | -10~85 | °C |

## DC Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|--------|-----------|------|------|------|------|
| $V_{DD}$ | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | – | $V_{DD} + 0.5$ | V |
| $V_{IL}$ | Input Low Voltage | -0.5 | – | 0.8 | V |

## DC Characteristics (Ta = 0 ~ 70°C, $V_{DD}$ = 5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|--------|-----------|----------------|--|------|------|------|------|
| $I_{LI}$ | Input Leakage Current | $V_{IN} = 0 \sim V_{DD}$ | | – | – | ±10 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$ | | – | – | ±10 | μA |
| $I_{OH}$ | Output High Current | $V_{OH} = 2.4V$ | | -4 | – | – | mA |
| $I_{OL}$ | Output Low Current | $V_{OL} = 0.4V$ | | 8 | – | – | mA |
| $I_{DDO}$ | Operating Current | $t_{cycle}$ = Min cycle, $\overline{CE} = V_{IL}$ $I_{OUT}$ = 0 mA Other Inputs = $V_{IH}/V_{IL}$ | -10 | – | – | 200 | mA |
| | | | -12 | – | – | 190 | |

## Capacitance* (Ta = 25°C, f = 1.0MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|--------|-----------|----------------|------|------|
| $C_{IN}$ | Input Capacitance | $V_{IN} = GND$ | 6 | pF |
| $C_{CLK}$ | Clock Input Capacitance | $V_{CLK} = GND$ | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = GND$ | 8 | pF |

* This parameter is periodically sampled and is not 100% tested.

## AC Characteristics (Ta = 0 ~ 70°C [1], $V_{DD}$ = 5V±10%)

| SYMBOL | PARAMETER | TC55BS4258J-10 | | TC55BS4258J-12 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| $t_{CY}$ | Cycle Time | 10 | – | 12 | – | ns |
| $t_{CHH}$ | Clock Pulse High Width | 3 | – | 3 | – | |
| $t_{CLL}$ | Clock Pulse Low Width | 3 | – | 3 | – | |
| $t_{AS}$ | Address Setup Time | 2 | – | 2 | – | |
| $t_{DS}$ | Data Input Setup Time | 2 | – | 2 | – | |
| $t_{ES}$ | Chip Enable Input Setup Time | 2 | – | 2 | – | |
| $t_{WS}$ | Write Enable Input Setup Time | 2 | – | 2 | – | |
| $t_{GS}$ | Output Enable Input Setup Time | 2 | – | 2 | – | |
| $t_{AH}$ | Address Hold Time | 1 | – | 1 | – | |
| $t_{DH}$ | Data Input Hold Time | 1 | – | 1 | – | |
| $t_{EH}$ | Chip Enable Input Hold Time | 1 | – | 1 | – | |
| $t_{WH}$ | Write Enable Input Hold Time | 1 | – | 1 | – | |
| $t_{GH}$ | Output Enable Input Hold Time | 1 | – | 1 | – | |
| $t_{ACK}$ | Clock Access Time | 1 | 5 | 1 | 6 | |
| $t_{ECL(2)}$ | Output EnableTime from Clock | 1 | 5 | 1 | 6 | |
| $t_{DCL(2)}$ | Output DisableTime from Clock | 1 | 5 | 1 | 6 | |

(1) : The operating temperature (Ta) is guaranteed with transverse air flow exceeding 500 linear feet per minute.
(2) : Transition is measured ±200mV from steady voltage with the loading in Fig. 1.

## AC Test Conditions

| Input Pulse Levels | 3.0/0.0V |
|---|---|
| Input Pulse Rise and Fall Time | 3ns |
| Input Timing Measurement Reference Levels | 1.5V |
| Output Timing Measurement Reference Levels | 1.5V |
| Output Load | Fig. 1 |



Figure 1.

**TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.**                    **PRELIMINARY**
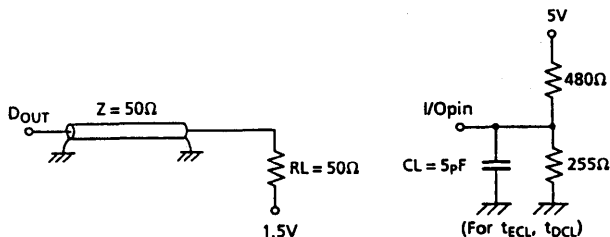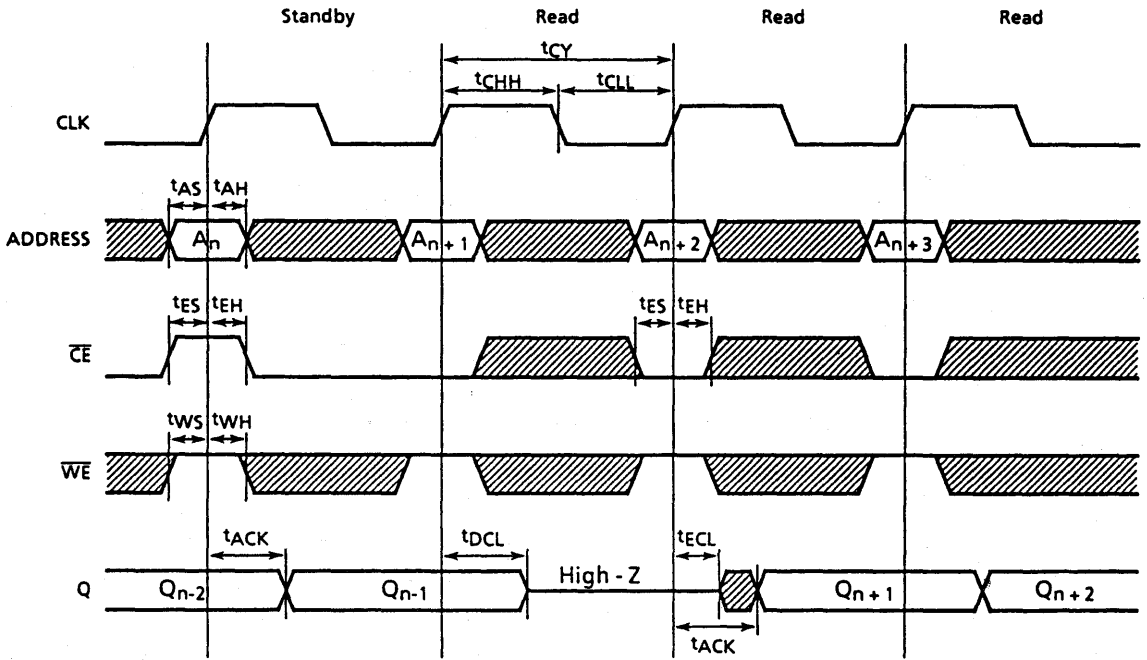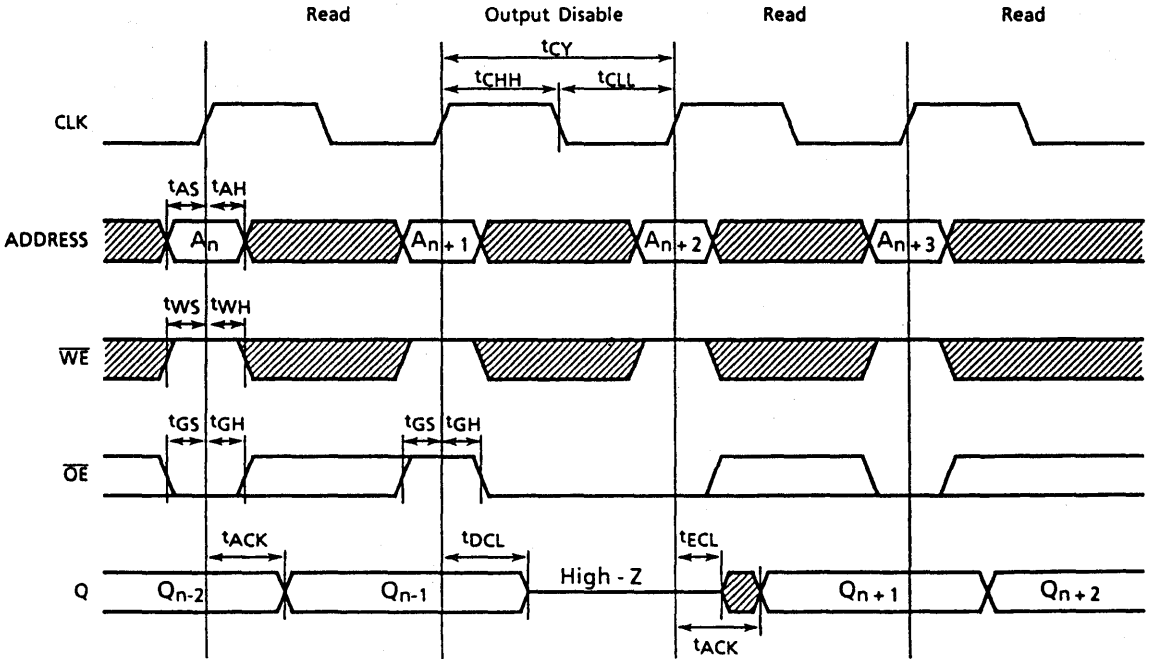
## Timing Waveforms

### Read Cycle 1 ($\overline{OE} = V_{IL}$)



### Read Cycle 2 ($\overline{CE} = V_{IL}$)

## Write and Pass-Through Mode

Write          Write and          Write and          Pass - Through
               Pass - Through     Pass - Through

$t_{CY}$

$t_{CHH}$        $t_{CLL}$

CLK

$t_{AS}$ $t_{AH}$

ADDRESS     $A_n$     $A_{n+1}$     $A_{n+2}$     $A_{n+3}$

$t_{ES}$ $t_{EH}$                                    $t_{ES}$ $t_{EH}$

$\overline{CE}$

$t_{WS}$ $t_{WH}$

$\overline{WE}$

$t_{GS}$ $t_{GH}$                    $t_{GS}$ $t_{GH}$

$\overline{OE}$

$t_{DS}$ $t_{DH}$

D     $D_n$     $D_{n+1}$     $D_{n+2}$     $D_{n+3}$

$t_{DCL}$          $t_{ECL}$

Q     $Q_{n-2}$     High - Z     $Q_n$     $Q_{n+1}$     $Q_{n+2}$

$t_{ACK}$