TC55BS8125J-10/12

PRELIMINARY

131,072 WORD x 8 BIT SYNCHRONOUS STATIC RAM

with Input Registers and Output Registers

Description

The TC55BS8125J is a 1,048,576 bit synchronous static random access memory fabricated using BiCMOS technology and organized as 131,072 words by 8 bits. The TC55BS8125J is similar to the TC55BS8128J but has common data I/O lines and does not have the write-cycle pass-through feature.

Designed for pipelined architectures, this device has internal input and output registers which latch on the positive edge of an external clock (CLK). All address, data, and control signals are latched. The setup and hold times for the inputs are 2ns and 1ns respectively. Synchronous SRAMs can lead to faster, more robust system operation by virtually eliminating the timing skew problems associated with conventional asynchronous SRAMs. For example, write operations are internally self-timed when initiated - eliminating the need for accurate write pulse generation and timing by the memory controller or microprocessor. For read cycles, data is available one clock cycle after the address is latched. All inputs and outputs are TTL compatible.

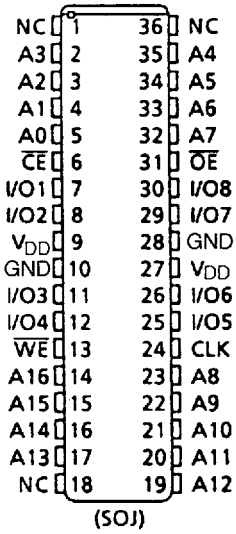
The TC55BS8125J is available in a 36-pin, 400mil SOJ package suitable for high density assembly.

Features

- Fast cycle time
  - TC55BS8125J-10 10ns (max.)
  - TC55BS8125J-12 12ns (max.)
- Fast clock access time
  - TC55BS8125J-10 5ns (max.)
  - TC55BS8125J-12 6ns (max.)
- Input and output registers for synchronous operation
- Single power supply: 5V±10%
- Common data I/O
- Package: JEDEC standard pinout
  - 36-pin, 400mil SOJ: SOJ36-P-400

Pin Connection (Top View)

TC55BS8125J

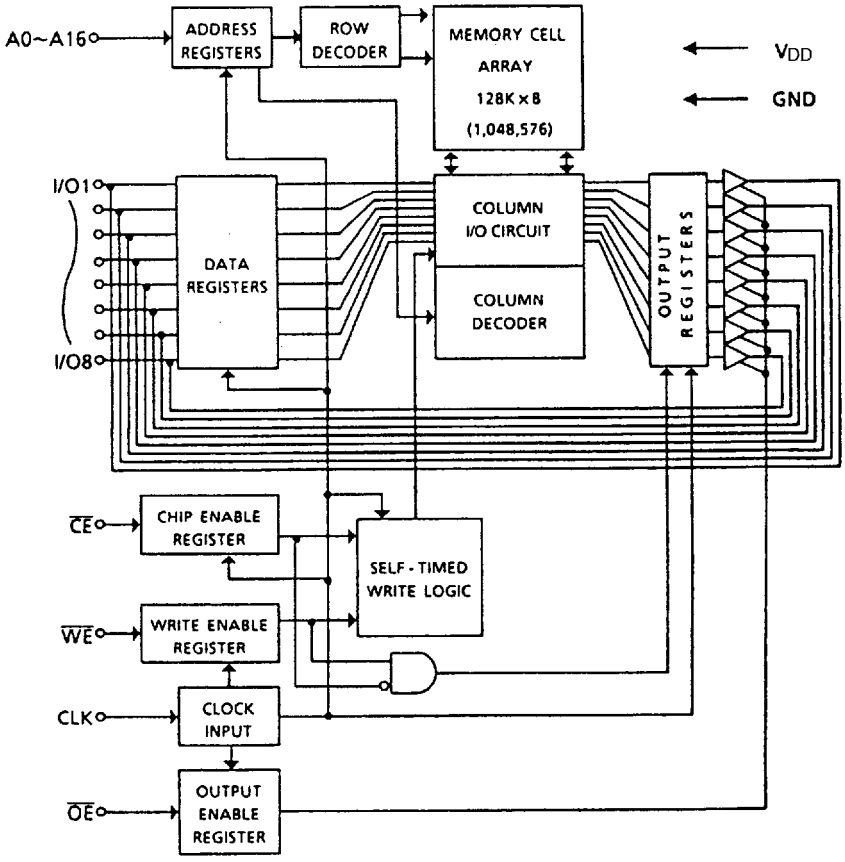


(SOJ)

Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Input and Output
CLK	Clock Input
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$ (next Cycle)	D	Q (next Cycle)
Write	L	L	*	D_{IN}	High - Z
Read	L	H	L	–	D_{OUT}
Output Disable	L	H	H	–	High - Z
Standby	H	*	*	–	High - Z

* H or L, –Not applicable

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1500	mW
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	–	0.8	V

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, Other Inputs = V_{IH}/V_{IL}	-10	–	–	230	mA
			-12	–	–	220	

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{CLK}	Clock Input Capacitance	V_{CLK} = GND	8	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = GND	8	pF

* This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C [1], V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TC55BS8125J-10		TC55BS8125J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CY}	Cycle Time	10	–	12	–	ns
t_{CHH}	Clock Pulse High Width	3	–	3	–	
t_{CLL}	Clock Pulse Low Width	3	–	3	–	
t_{AS}	Address Setup Time	2	–	2	–	
t_{DS}	Data Input Setup Time	2	–	2	–	
t_{ES}	Chip Enable Input Setup Time	2	–	2	–	
t_{WS}	Write Enable Input Setup Time	2	–	2	–	
t_{GS}	Output Enable Input Setup Time	2	–	2	–	
t_{AH}	Address Hold Time	1	–	1	–	
t_{DH}	Data Input Hold Time	1	–	1	–	
t_{EH}	Chip Enable Input Hold Time	1	–	1	–	
t_{WH}	Write Enable Input Hold Time	1	–	1	–	
t_{GH}	Output Enable Input Hold Time	1	–	1	–	
t_{ACK}	Clock Access Time	1	5	1	6	
$t_{ECL(2)}$	Output EnableTime from Clock	1	5	1	6	
$t_{DCL(2)}$	Output DisableTime from Clock	1	5	1	6	

(1) : The operating temperature (Ta) is guaranteed with transverse air flow exceeding 500 linear feet per minute.
(2) : Transition is measured ±200mV from steady voltage with the loading in Fig.1.

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

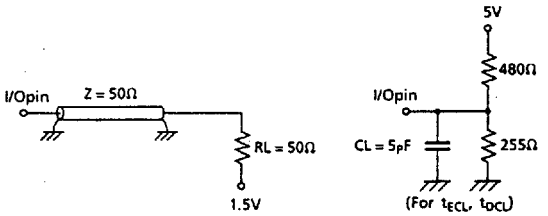
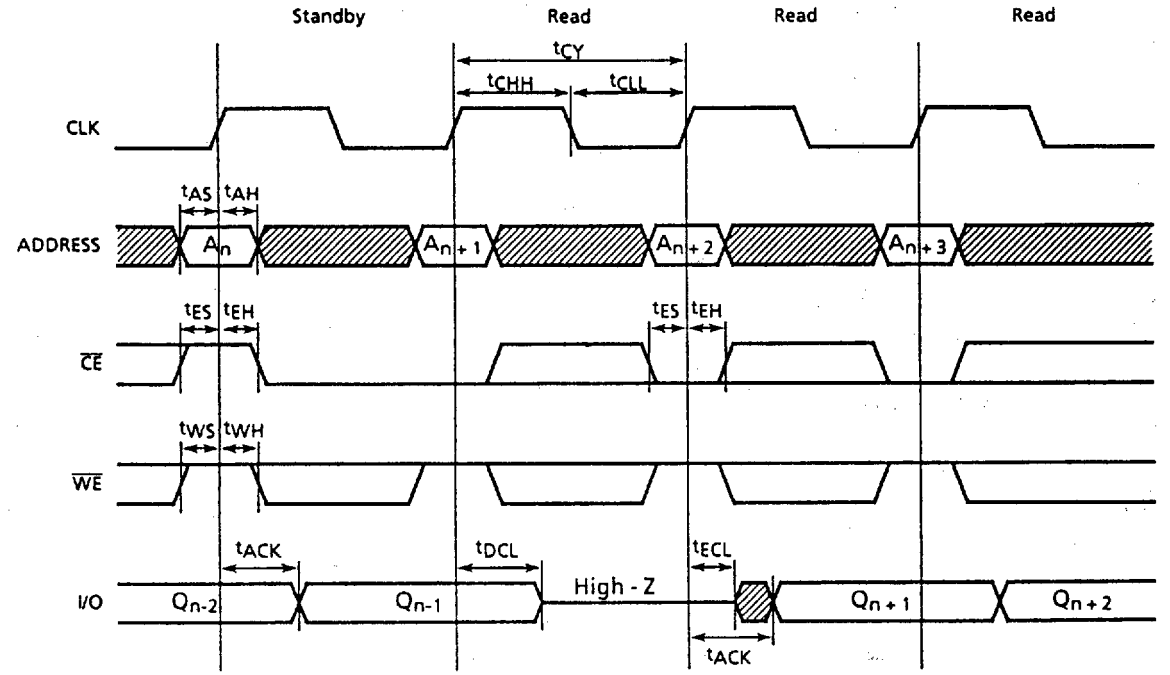


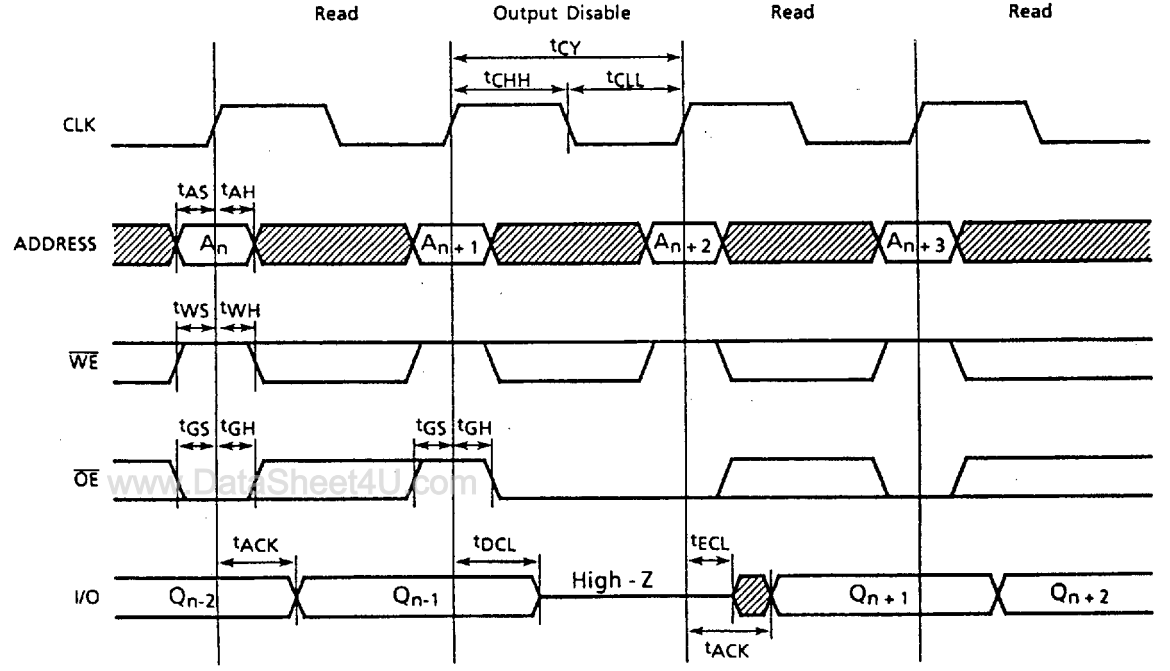
Figure 1.

Timing Waveforms

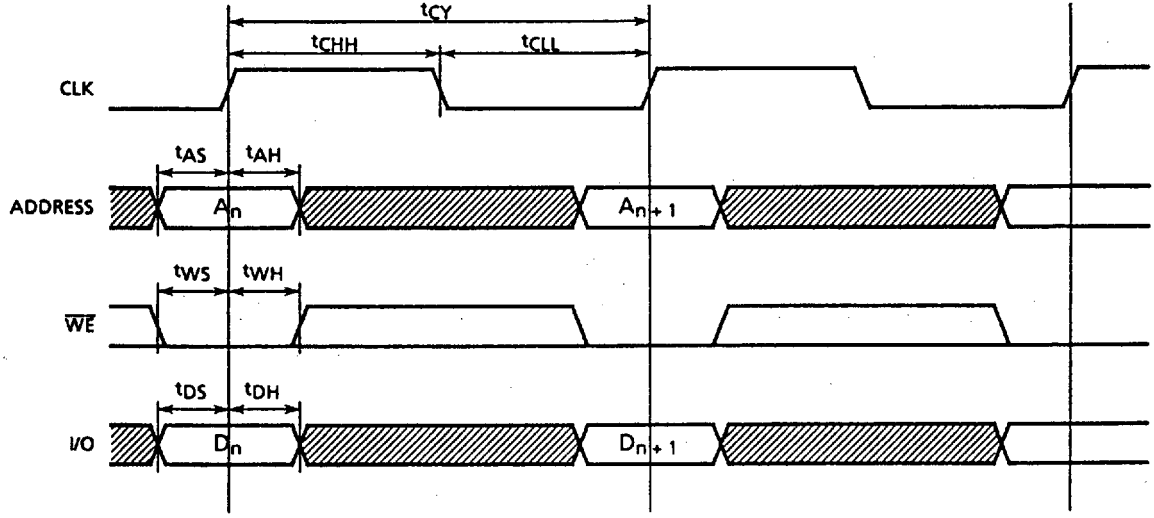
Read Cycle 1 ($\overline{OE}$ = V_{IL})



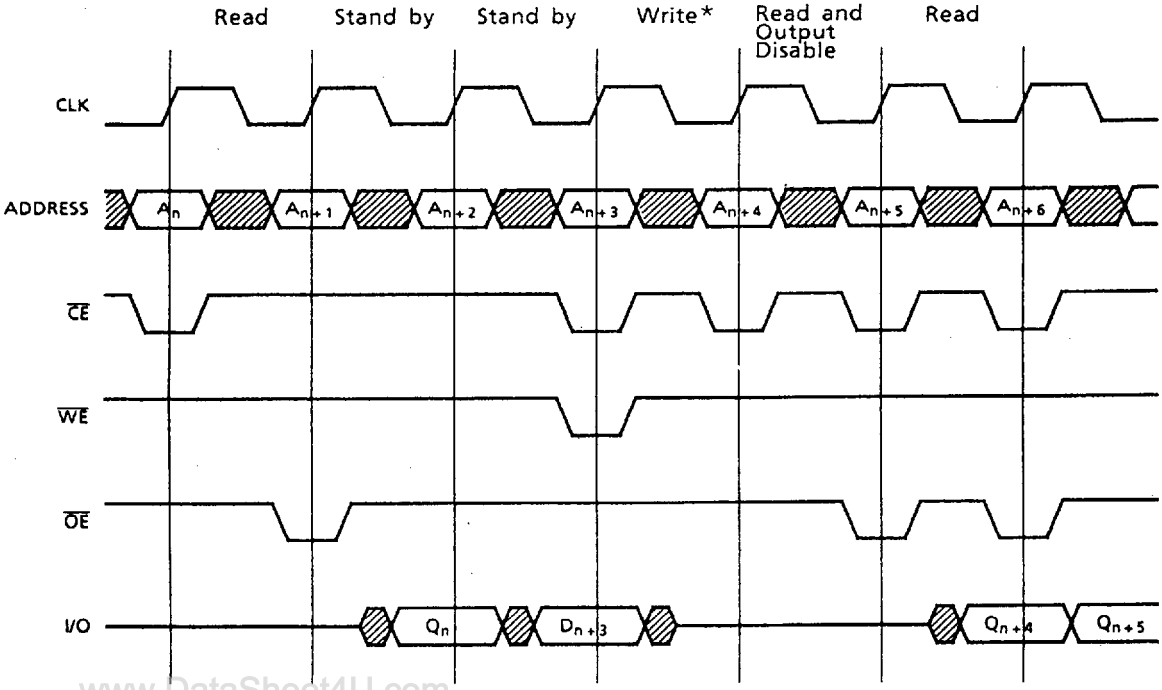
Read Cycle 2 ($\overline{CE}$ = V_{IL})



Write Cycle



Read and Write Cycle



* A minimum of two standby cycles must separate a write cycle which follows a read cycle.