

131,072-WORD BY 8-BIT STATIC RAM

## DESCRIPTION

The TC55V1001AF/AFT/ATR/AST/ASR is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5  $\mu$ A standby current (L-Version at  $V_{DD}=3V$ ,  $T_a=25^\circ C$ ) when chip enable ( $\overline{CE1}$ ) is asserted high or ( $CE2$ ) is asserted low. There are three control inputs.  $\overline{CE1}$  and  $CE2$  are used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V1001AF/AFT/ATR/AST/ASR is available in a plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

## FEATURES

- Low-power dissipation  
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.7 to 3.6 V
- Power down features using  $\overline{CE1}$  and  $CE2$ .
- Data retention supply voltage of 2 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Standby current ( $T_a=25^\circ C$  maximum)

	TC55V1001AF/AFT/ATR/AST/ASR	
	-70	-70L
3.6V	3 $\mu$ A	0.9 $\mu$ A
3.0V	1 $\mu$ A	0.5 $\mu$ A

- Access Times (maximum):

Access Time	70ns
$\overline{CE1}$ Access Time	70ns
$CE2$ Access Time	70ns
$\overline{OE}$ Access Time	35ns

- Packages:

SOP32-P-525-1.27 (AF) (Weight: 1.04 g typ)  
 TSOP I 32-P-0820-0.50 (AFT) (Weight: 0.34 g typ)  
 TSOP I 32-P-0820-0.50A (ATR) (Weight: 0.34 g typ)  
 TSOP I 32-P-0.50 (AST) (Weight: 0.24 g typ)  
 TSOP I 32-P-0.50A (ASR) (Weight: 0.24 g typ)

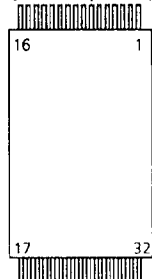
## PIN ASSIGNMENT (TOP VIEW)

o 32 PIN SOP

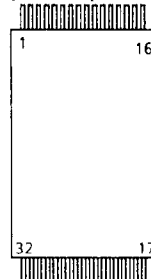
NC	1	32	$V_{DD}$
A16	2	31	A15
A14	3	30	$CE2$
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

o 32 PIN TSOP

(Normal pinout)



(Reverse pinout)



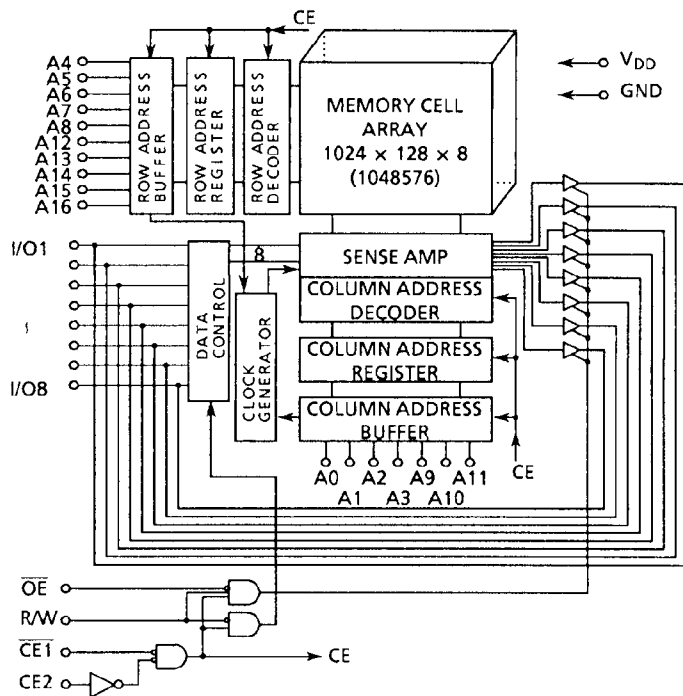
## PIN NAMES

A0 to A16	Address Inputs	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
R/W	Read/Write Control	Pin Name	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	$CE2$	A <sub>15</sub>	$V_{DD}$	NC	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
$\overline{OE}$	Output Enable	Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
$\overline{CE1}$ , $CE2$	Chip Enable	Pin Name	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A <sub>10</sub>	$\overline{OE}$
I/O1 to I/O8	Data Input/Output																	
$V_{DD}$	Power																	
GND	Ground																	
NC	No Connection																	

961001EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	H	x	L	D <sub>IN</sub>	I <sub>DDO</sub>
Outputs Disabled	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	x	x	x	High-Z	I <sub>DDs</sub>
	x	L	x	x	High-Z	I <sub>DDs</sub>

Note: x = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 4.6	V
V <sub>IN</sub>	Input Voltage	- 0.3* to 4.6	V
V <sub>I/O</sub>	Input/Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.8	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg.</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr.</sub>	Operating Temperature	0 to 70	°C

\* - 3.0 V when measured at a pulse width of 50 ns

\*\* SOP

**DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER	2.7 to 3.6 V			UNIT
		MIN	TYP	MAX	
V <sub>DD</sub>	Power Supply Voltage	2.7	-	3.6	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	- 0.3*	-	0.8	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	3.6	

\* - 3.0 V when measured at a pulse width of 50 ns

**DC CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 2.7 to 3.6 V)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT				
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA				
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V	-0.5	-	-	mA				
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.1	-	-	mA				
I <sub>LO</sub>	Output Leakage Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA				
I <sub>DDO1</sub>	Operating Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> and R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA Other Input = V <sub>IH</sub> /V <sub>IL</sub>	V <sub>DD</sub> = 3 V ± 10%	Tcycle	min	-	-	35	mA	
					1 μs	-	-	10		
I <sub>DDO2</sub>	Operating Current	CE1 = 0.2 V and CE2 = V <sub>DD</sub> - 0.2 V R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	V <sub>DD</sub> = 3.3 V ± 0.3 V	Tcycle	min	-	-	40		
					1 μs	-	-	12		
I <sub>DDO2</sub>	Operating Current	CE1 = 0.2 V and CE2 = V <sub>DD</sub> - 0.2 V R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	V <sub>DD</sub> = 3 V ± 10%	Tcycle	min	-	-	30		
					1 μs	-	-	5		
I <sub>DDO2</sub>	Operating Current	CE1 = 0.2 V and CE2 = V <sub>DD</sub> - 0.2 V R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	V <sub>DD</sub> = 3.3 V ± 0.3 V	Tcycle	min	-	-	35		
					1 μs	-	-	6		
I <sub>DDS1</sub>	Standby Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	-	-	2	mA				
I <sub>DDS2</sub> (Note)	Standby Current	CE1 = V <sub>DD</sub> - 0.2 V or CE2 = 0.2 V V <sub>DD</sub> = 2.0 to 3.6 V	V <sub>DD</sub> = 3 V ± 10%	Ta = 25°C	-70	-	1	2	μA	
					-70L	-	0.5	0.7		
				Ta = 0° to 70°C	-70	-	-	20		
					-70L	-	-	15		
					Ta = 25°C	-70	-	2		3
						-70L	-	0.7		0.9
			V <sub>DD</sub> = 3 V	Ta = 0° to 70°C	-70	-	-	25		
					-70L	-	-	20		
					Ta = 25°C	-70	-	-		1
						-70L	-	-		0.5
				Ta = 0° to 40°C	-70	-	-	3		
					-70L	-	-	2		
Ta = 0° to 70°C	-70	-	-	15						
	-70L	-	-	10						

Note: In standby mode with CE1 ≥ V<sub>DD</sub> - 0.2 V, these limits are assured for the condition CE2 ≥ V<sub>DD</sub> - 0.2 V or CE2 ≤ 0.2 V.

**CAPACITANCE (Ta = 25°C, f = 1 MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ( $T_a = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $3.6\text{ V}$ )READ CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{RC}$	Read Cycle Time	70	–	ns
$t_{ACC}$	Address Access Time	–	70	
$t_{CO1}$	Chip Enable (CE1) Access Time	–	70	
$t_{CO2}$	Chip Enable (CE2) Access Time	–	70	
$t_{OE}$	Output Enable Access Time	–	35	
$t_{COE}$	Chip Enable Low to Output Active	10	–	
$t_{OEE}$	Output Enable Low to Output Active	5	–	
$t_{OD}$	Chip Enable High to Output High-Z	–	25	
$t_{ODO}$	Output Enable High to Output High-Z	–	25	
$t_{OH}$	Output Data Hold Time	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{WC}$	Write Cycle Time	70	–	ns
$t_{WP}$	Write Pulse Width	50	–	
$t_{CW}$	Chip Enable to End of Write	60	–	
$t_{AS}$	Address Setup Time	0	–	
$t_{WR}$	Write Recovery Time	0	–	
$t_{ODW}$	R/W Low to Output High-Z	–	25	
$t_{OEW}$	R/W High to Output Active	5	–	
$t_{DS}$	Data Setup Time	30	–	
$t_{DH}$	Data Hold Time	0	–	

AC TEST CONDITIONS

Output load: 100 pF + one TTL gate

Input pulse level: 0.6 V, 2.2 V

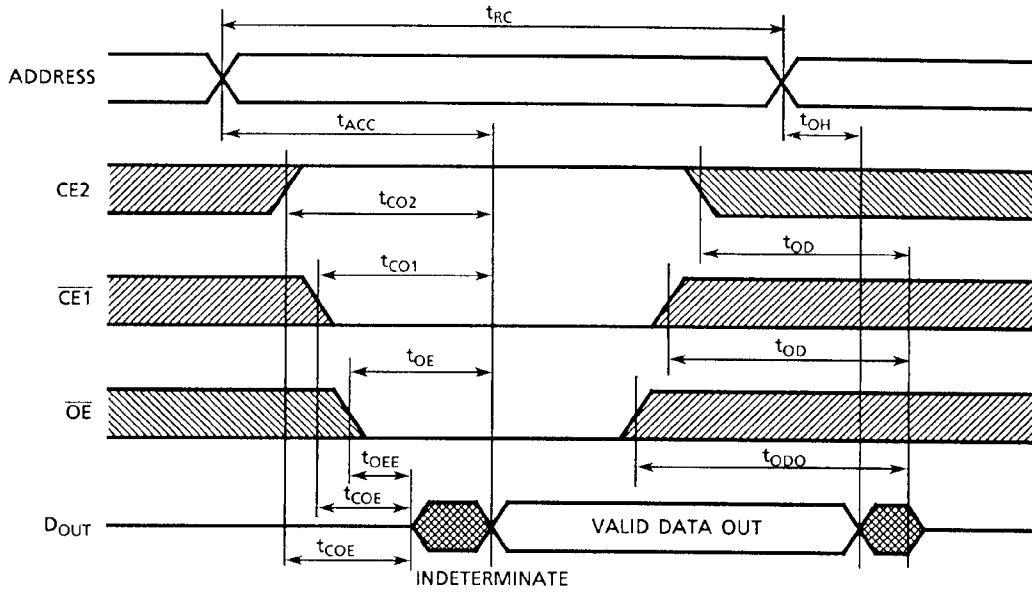
Timing measurements: 1.5 V

Reference level: 1.5 V

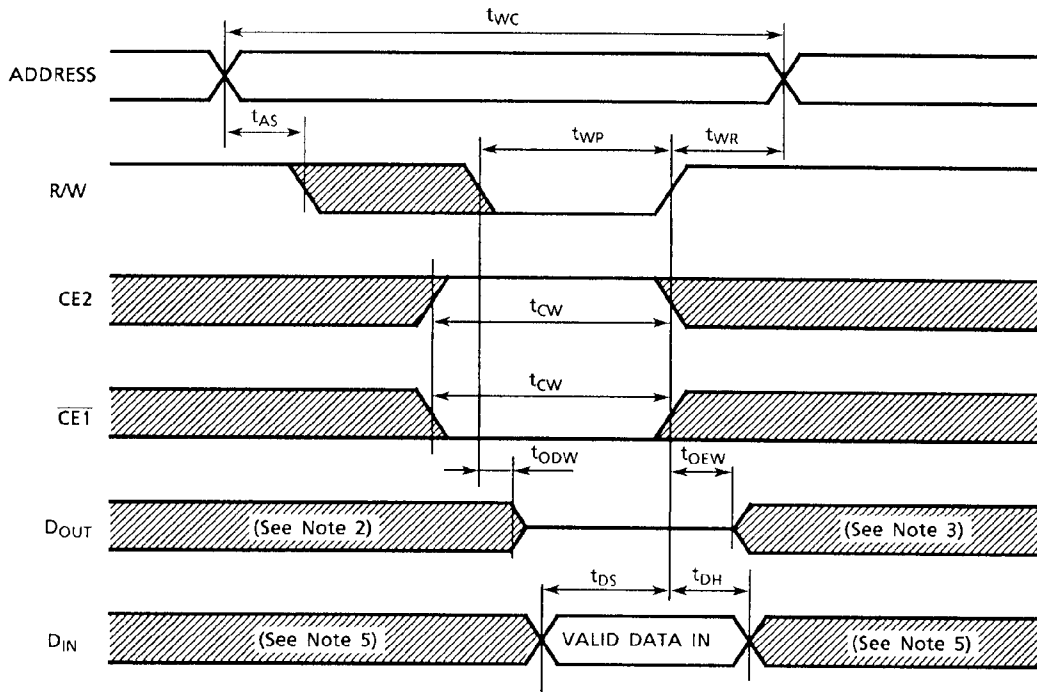
 $t_R, t_F: 5\text{ ns}$

**TIMING DIAGRAMS**

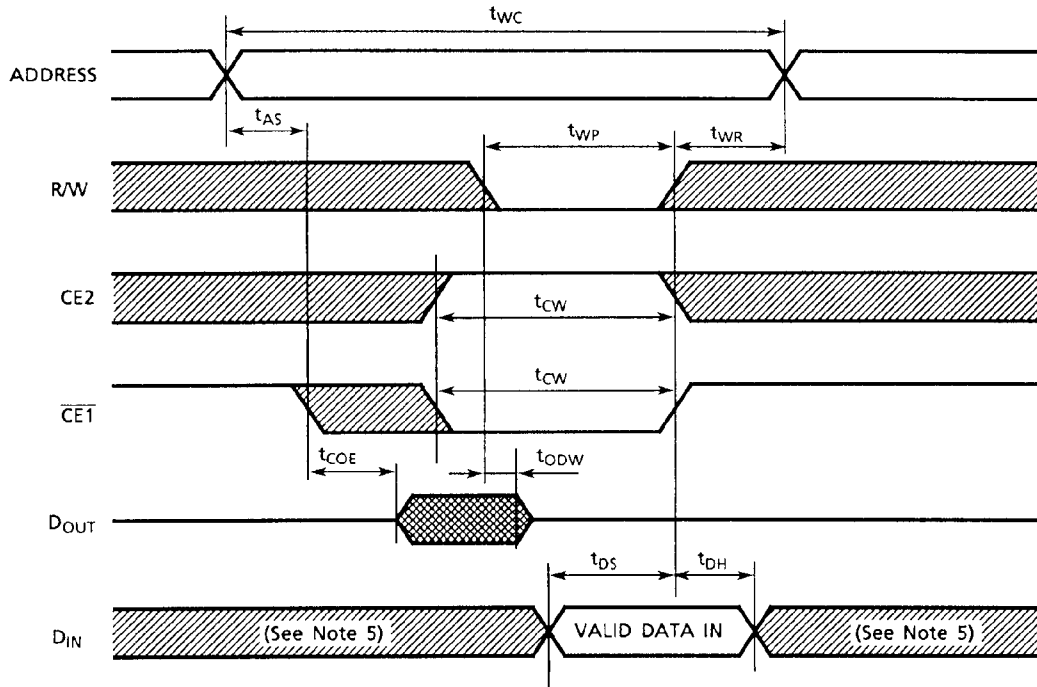
**READ CYCLE (See Note 1)**



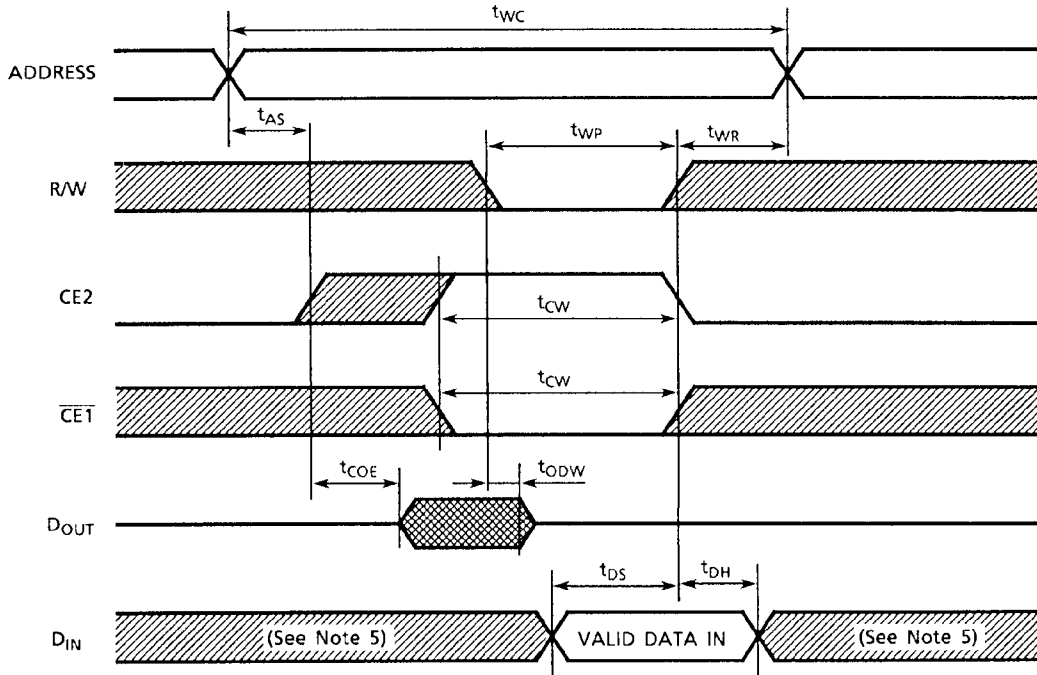
**WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)**



WRITE CYCLE 2 ( $\overline{CE1}$  CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If  $\overline{CE1}$  goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If  $\overline{CE1}$  goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

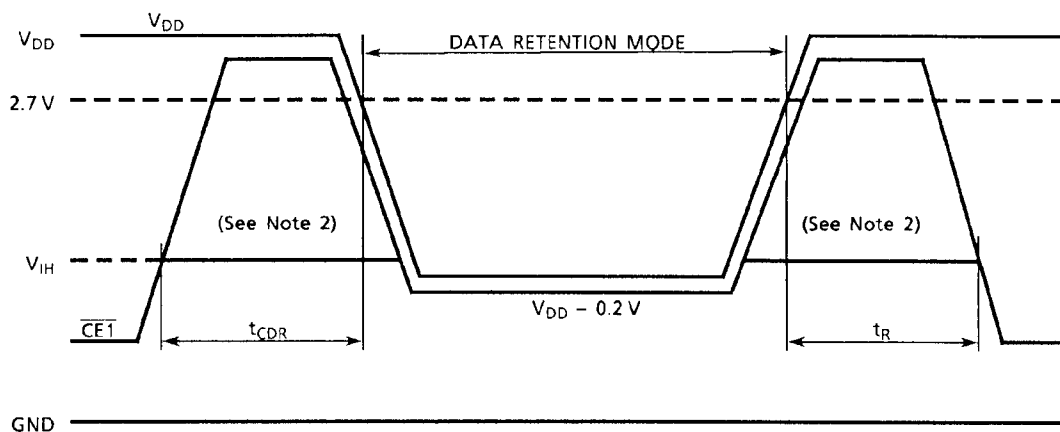
(4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

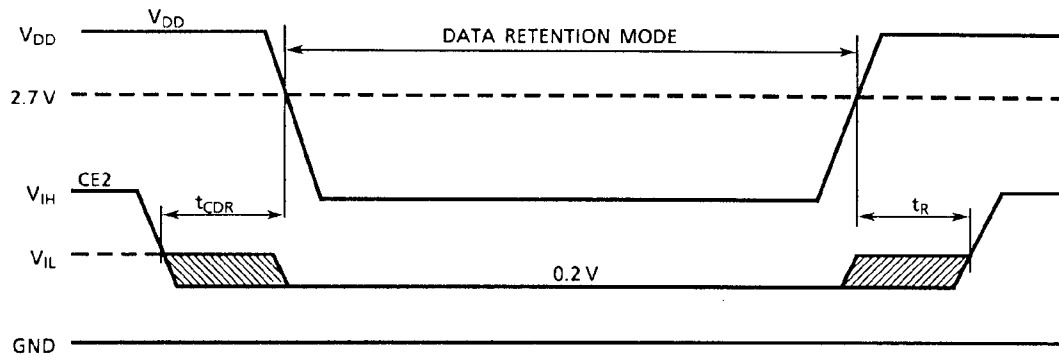
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

**DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	-	3.6	V	
I <sub>DDs2</sub>	Standby Current	V <sub>DH</sub> = 3.0V	Ta = 0° to 40°C	-70	-	3	μA
			-70L	-	-	2	
		V <sub>DH</sub> = 3.6V	Ta = 0° to 70°C	-70	-	15	
			-70L	-	-	10	
		V <sub>DH</sub> = 3.6V	Ta = 0° to 70°C	-70	-	25	
				-70L	-	20	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time		0	-	-	nS	
t <sub>R</sub>	Recovery Time		5	-	-	mS	

**CE1 CONTROLLED DATA RETENTION MODE (See Note 1)**



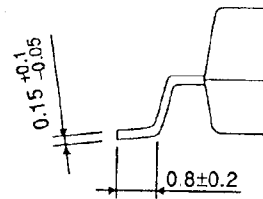
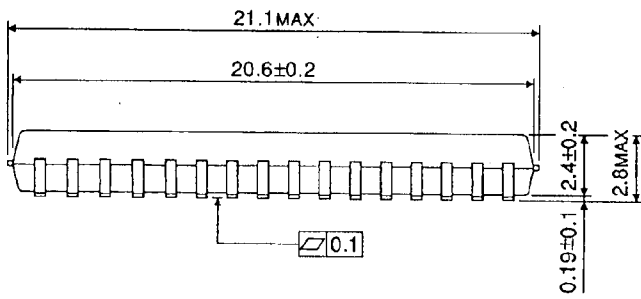
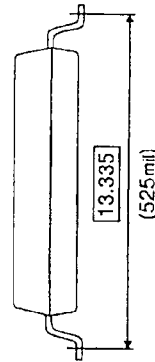
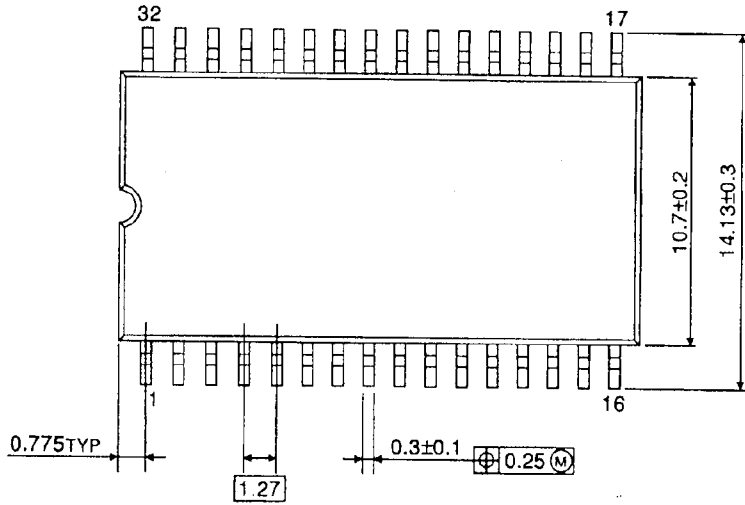
CE2 CONTROLLED DATA RETENTION MODE (See Note 3)

- Note: (1) In  $\overline{\text{CE1}}$  controlled data retention mode, minimum standby current mode is entered when  $\text{CE2} \leq 0.2 \text{ V}$  or  $\text{CE2} \geq V_{\text{DD}} - 0.2 \text{ V}$ .
- (2) When  $\overline{\text{CE1}}$  is operating at the  $V_{\text{IH}}$  level (2 V), the operating current is given by  $I_{\text{DDSI}}$  during the transition of  $V_{\text{DD}}$  from 3.6 to 2.2 V.
- (3) In CE2 controlled data retention mode, minimum standby current mode is entered when  $\text{CE2} \leq 0.2 \text{ V}$ .



PACKAGE DIMENSIONS (SOP32-P-525-1.27)

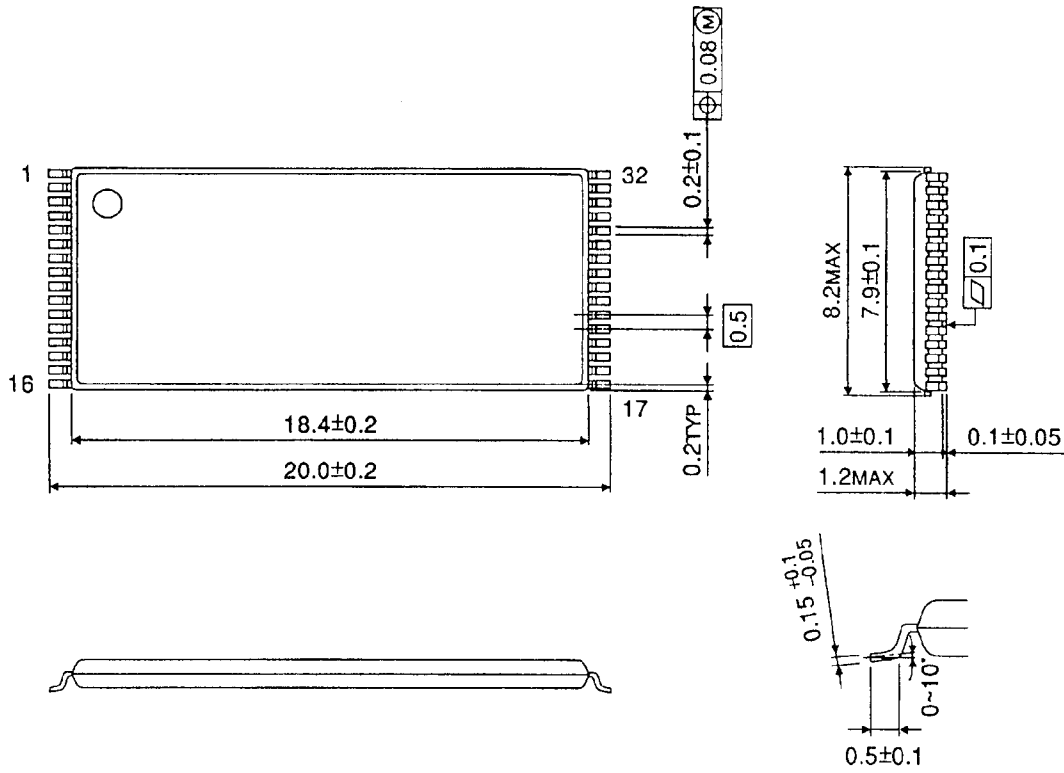
Units in mm



Weight: 1.04 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

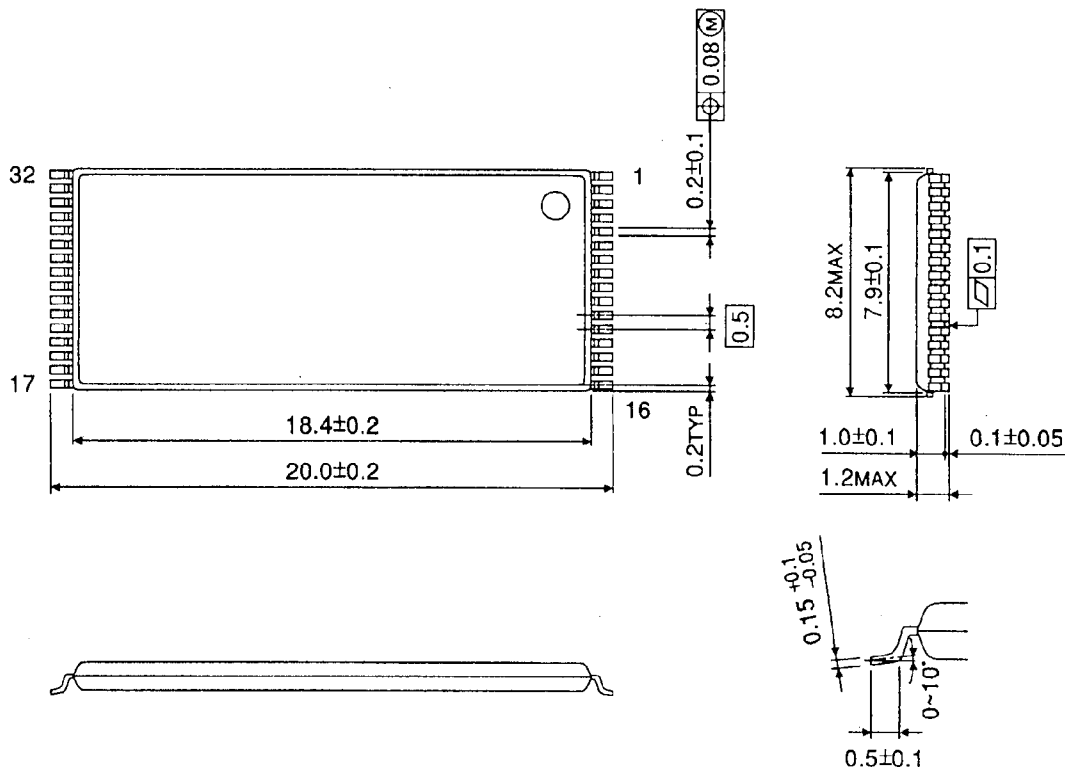
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)

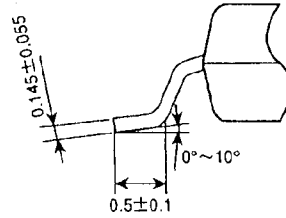
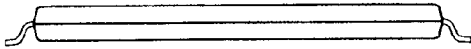
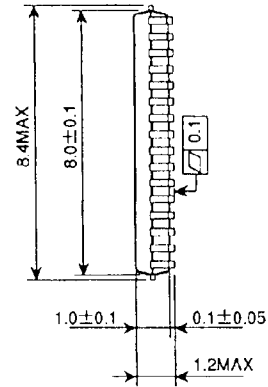
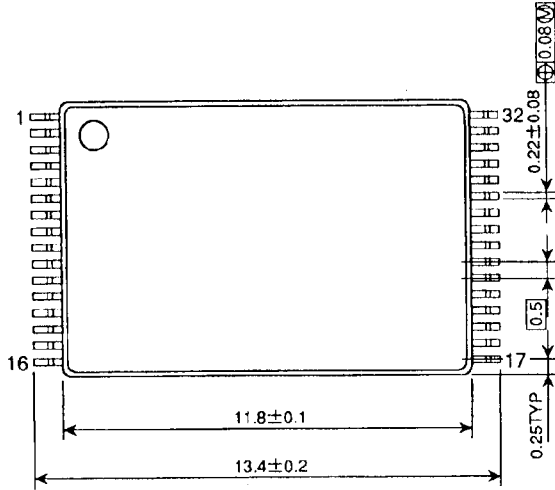
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

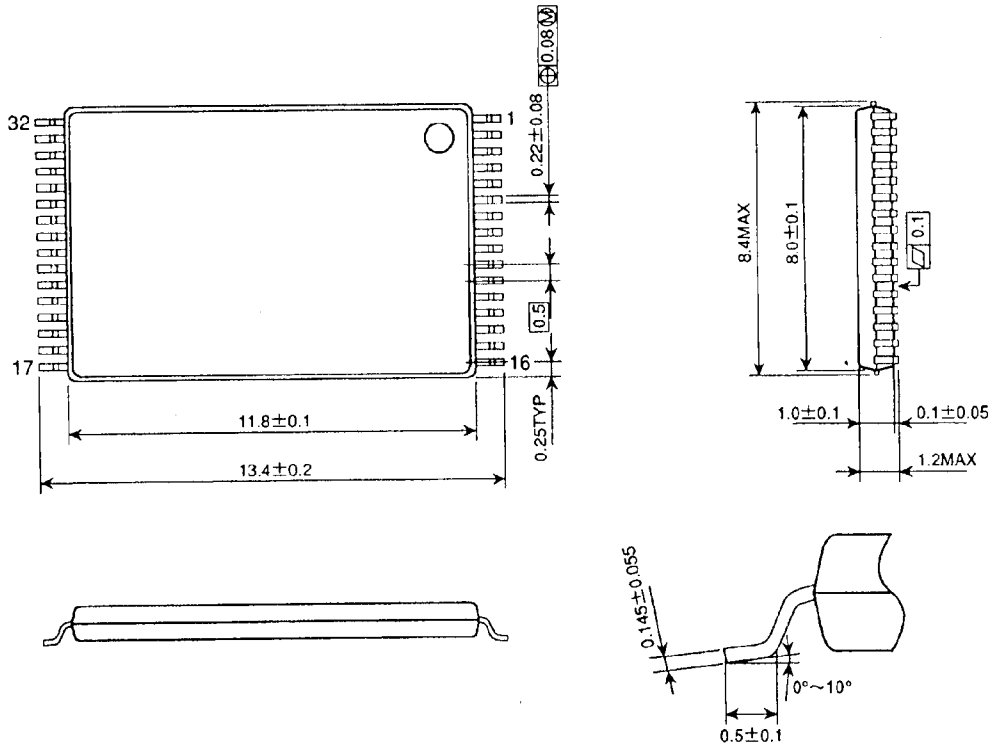
Units in mm



Weight: 0.24 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)

Units in mm



Weight: 0.24 g (typ)