

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V16100FT is a 16,777,216-bit high-speed static random access memory (SRAM) organized as 1,048,576 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. Data byte control signals (\overline{LB} , \overline{UB}) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTTL compatible. The TC55V16100FT is available in plastic 54-pin TSOP with 400mil width for high density surface assembly.

FEATURES

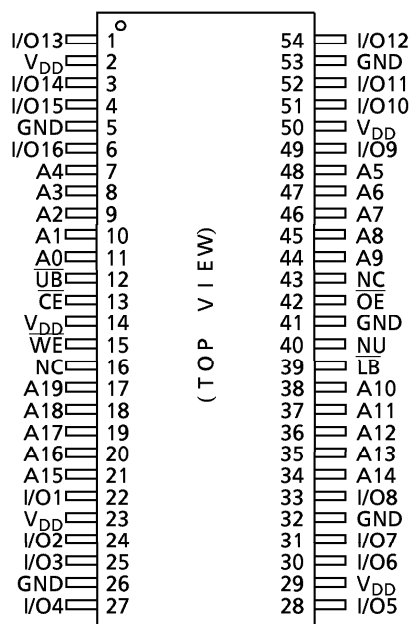
- Fast access time(the following are maximum values)
 - TC55V16100FT-10: 10 ns
 - TC55V16100FT-12: 12 ns
 - TC55V16100FT-15: 15 ns
- Low-power dissipation
- Single power supply voltage: $3.3V \pm 5\%$ (-10)
 $: 3.3V \pm 0.3V$ (-12, -15)
- Fully static operation
- All inputs and outputs are LVTTTL compatible
- Output buffer control using \overline{OE}
- Data byte control using \overline{LB} (I/O1 to I/O8) and \overline{UB} (I/O9 to I/O16)
- Package:
 TSOP II 54-P-400-0.80B(FT) (Weight: 0.55g typ)

Cycle Time	10	12	15	20	30	ns
Operation (max)	450	420	380	—	—	mA
Operation (typ)	340	280	250	190	150	mA

Typical condition : $V_{DD} = 3.3V$

Standby : 4mA(max)

PIN ASSIGNMENT



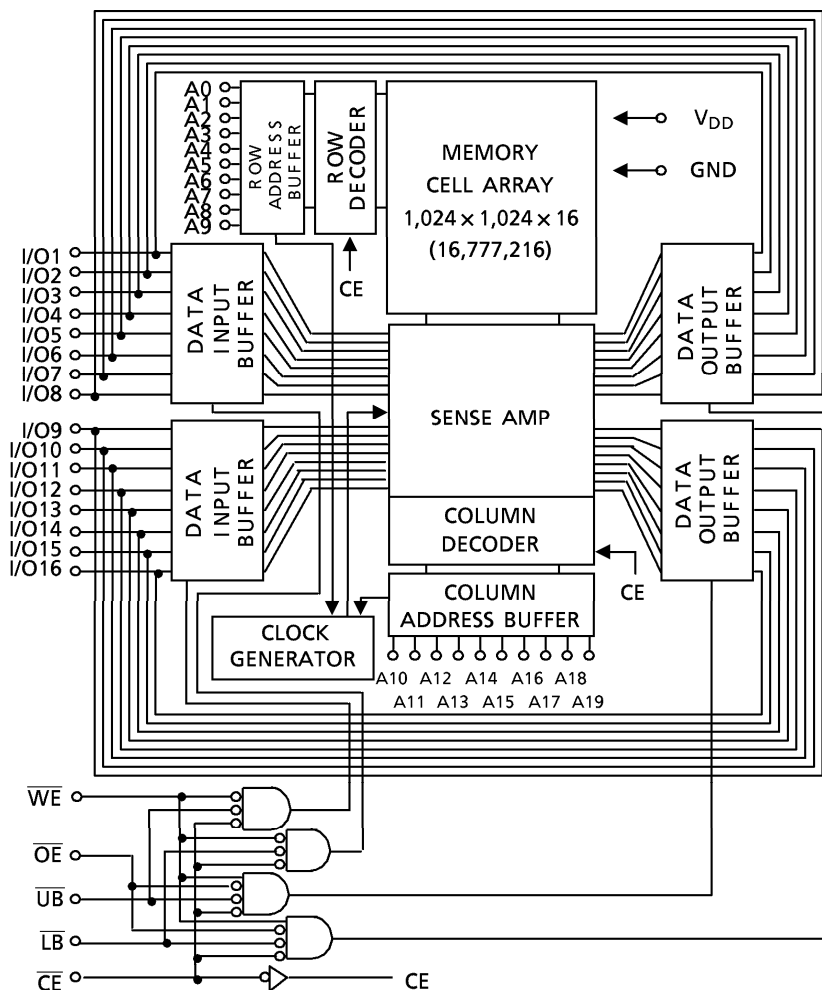
PIN NAMES

A0 to A19	Address Inputs
I/O1 to I/O16	Data Inputs / Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V_{DD}	Power (+ 3.3V)
GND	Ground
NC	No Connection
NU	Not Usable

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.5 to 4.6	V
V _{IN}	Input Terminal Voltage	- 0.5* to 4.6	V
V _{I/O}	Input/Output Terminal Voltage	- 0.5* to V _{DD} + 0.5**	V
P _D	Power Dissipation	1.8	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg}	Storage Temperature	- 65 to 150	°C
T _{opr}	Operating Temperature	- 10 to 85	°C

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD}+1.5V with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	-10	3.135	3.465	V
		-12,-15	3.0	3.6	
V _{IH}	Input High Voltage	2.0	-	V _{DD} + 0.3**	V
V _{IL}	Input Low Voltage	- 0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD}+1.0V with a pulse width of 20% · t_{RC} min (4ns max)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 3.3V ± 5% : -10, V_{DD} = 3.3V ± 0.3V : -12,-15)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP*	MAX	UNIT	
I _{IL}	Input Leakage Current (Except NU pin)	V _{IN} = 0 to V _{DD}	-1	-	1	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 to V _{DD}	-1	-	1	μA	
I _{I(NU)}	Input Current (NU pin)	V _{IN} = 0 to 0.8V	-1	-	20	μA	
		V _{IN} = 0 to 0.2V	-1	-	1		
V _{OH}	Output High Voltage	I _{OH} = -2mA	2.4	-	-	V	
		I _{OH} = -100μA	V _{DD} - 0.2	-	-		
V _{OL}	Output Low Voltage	I _{OL} = 2mA	-	-	0.4		
		I _{OL} = 100μA	-	-	0.2		
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0mA $\overline{OE} = V_{IH}$ Other Inputs = V _{DD} - 0.2V or 0.2V	t _{cycle} = 10ns	-	340	450	mA
			t _{cycle} = 12ns	-	280	420	
			t _{cycle} = 15ns	-	250	380	
			t _{cycle} = 20ns	-	190	-	
			t _{cycle} = 30ns	-	150	-	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IN} or V _{IL}	-	-	105	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	-	-	4		

* Typical Condition : V_{DD} = 3.3V

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I _{DDO}
				H	L	High Impedance	Output	I _{DDO}
				L	H	Output	High Impedance	I _{DDO}
Write	L	x	L	L	L	Input	Input	I _{DDO}
				H	L	High Impedance	Input	I _{DDO}
				L	H	Input	High Impedance	I _{DDO}
Outputs Disable	L	H	H	x	x	High Impedance	High Impedance	I _{DDO}
	L	x	x	H	H			
Standby	H	x	x	x	x	High Impedance	High Impedance	I _{DDS}

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.
You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C (Note 1), $V_{DD} = 3.3\text{V} \pm 5\%$:-10, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$:-12,-15)
READ CYCLE

SYMBOL	PARAMETER	TC55V16100FT-10		TC55V16100FT-12		TC55V16100FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	10	–	12	–	15	–	ns
t_{ACC}	Address Access Time	–	10	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	10	–	12	–	15	
t_{OE}	Output Enable Access Time	–	5	–	6	–	8	
t_{BA}	Upper Byte, Lower Byte Access Time	–	5	–	6	–	8	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	3	–	
t_{COE}	Output Enable Time from Chip Enable	3	–	3	–	3	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	1	–	
t_{BE}	Output Enable Time from Upper Byte, Lower Byte	1	–	1	–	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	6	–	7	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	6	–	7	–	8	
t_{BD}	Output Disable Time from Upper Byte, Lower Byte	–	6	–	7	–	8	

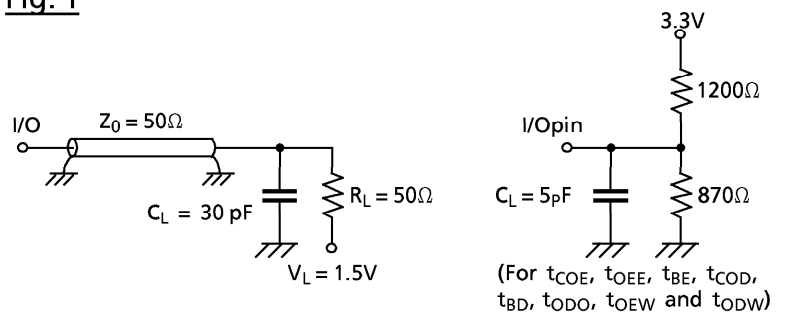
WRITE CYCLE

SYMBOL	PARAMETER	TC55V16100FT-10		TC55V16100FT-12		TC55V16100FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	10	–	12	–	15	–	ns
t_{WP}	Write Pulse Width	7	–	8	–	10	–	
t_{CW}	Chip Enable to End of Write	8.5	–	9	–	11	–	
t_{BW}	Upper Byte, Lower Byte Enable to End of Write	8.5	–	9	–	11	–	
t_{AW}	Address Valid to End of Write	8.5	–	9	–	11	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Setup Time	6	–	7	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from Write Enable	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from Write Enable	–	6	–	7	–	8	

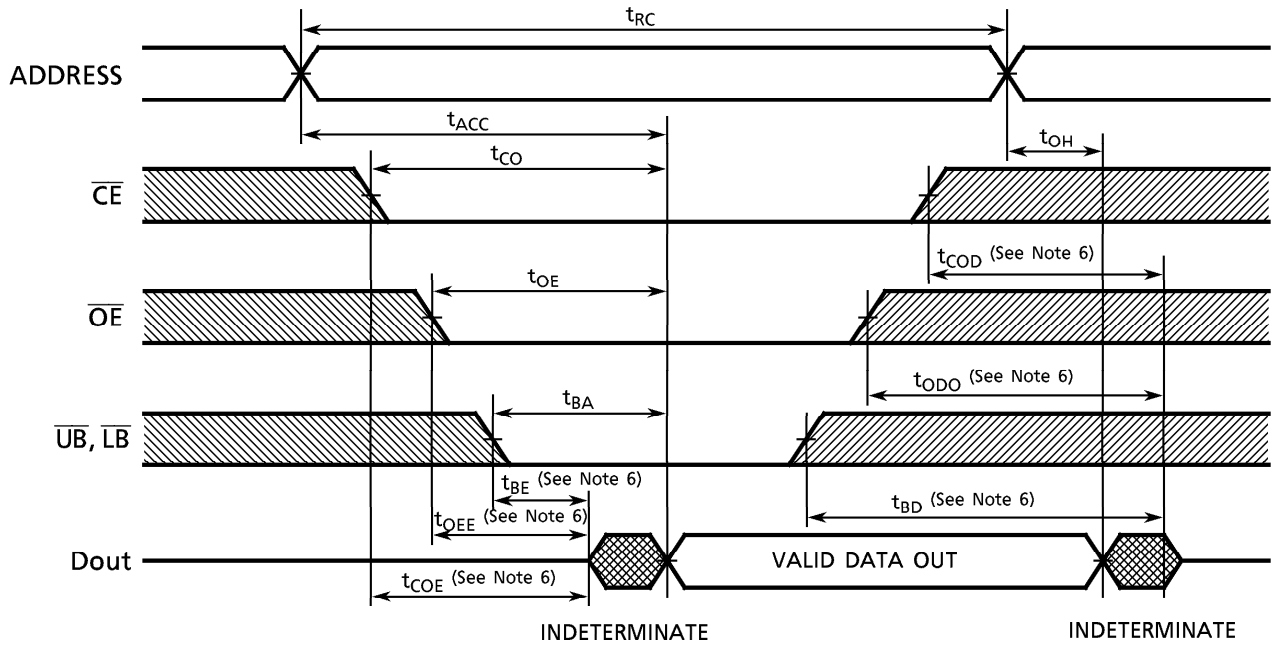
AC TEST CONDITIONS

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

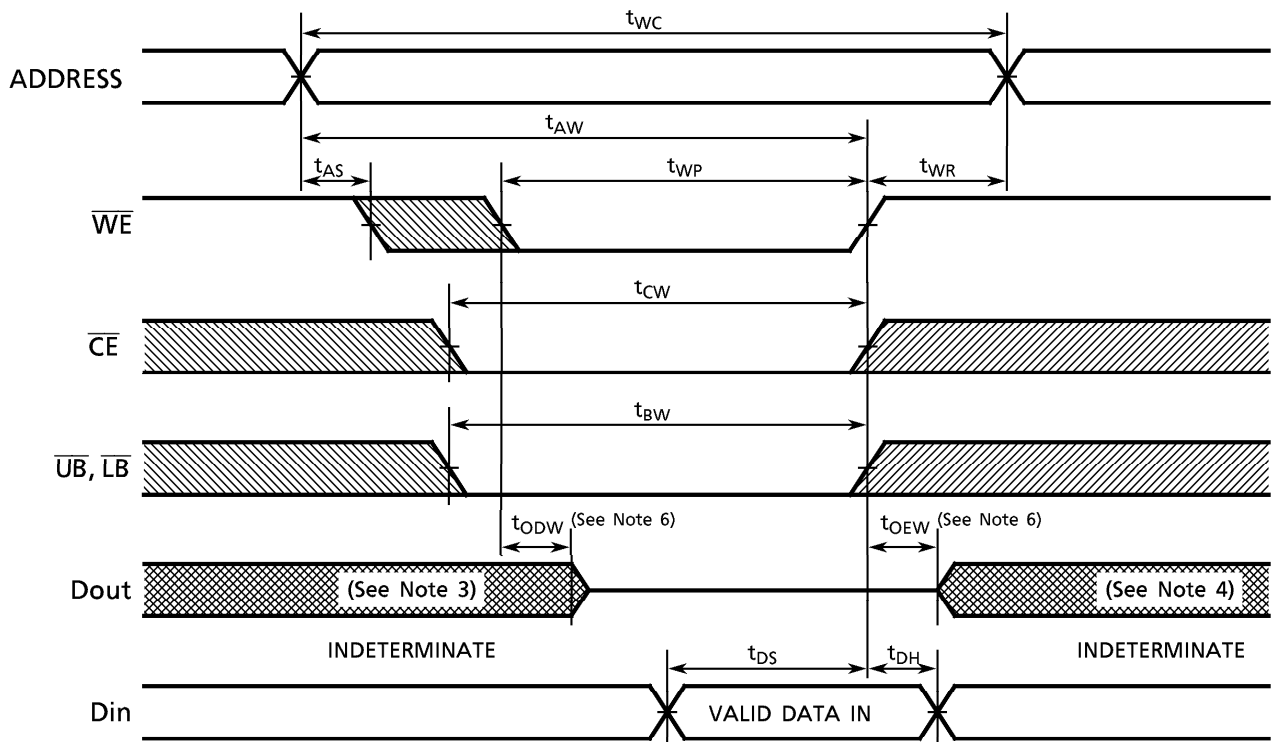
Fig. 1



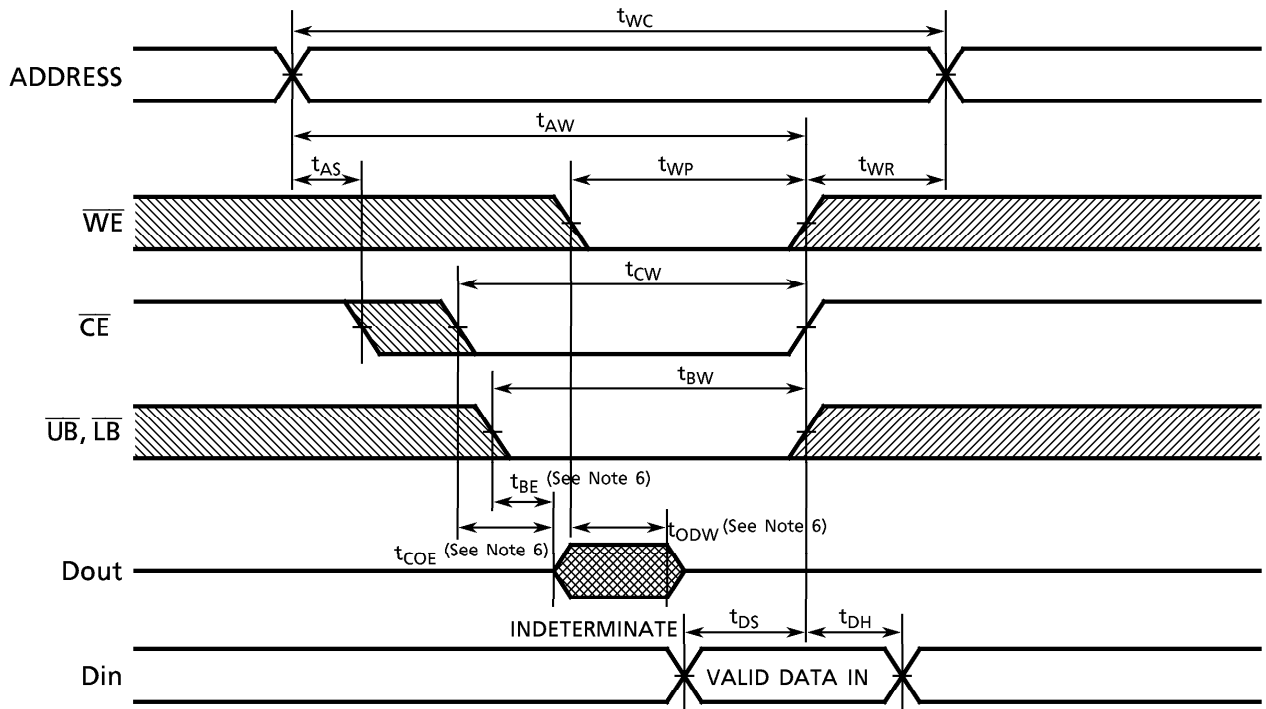
TIMING DIAGRAMS
READ CYCLE (See Note 2)



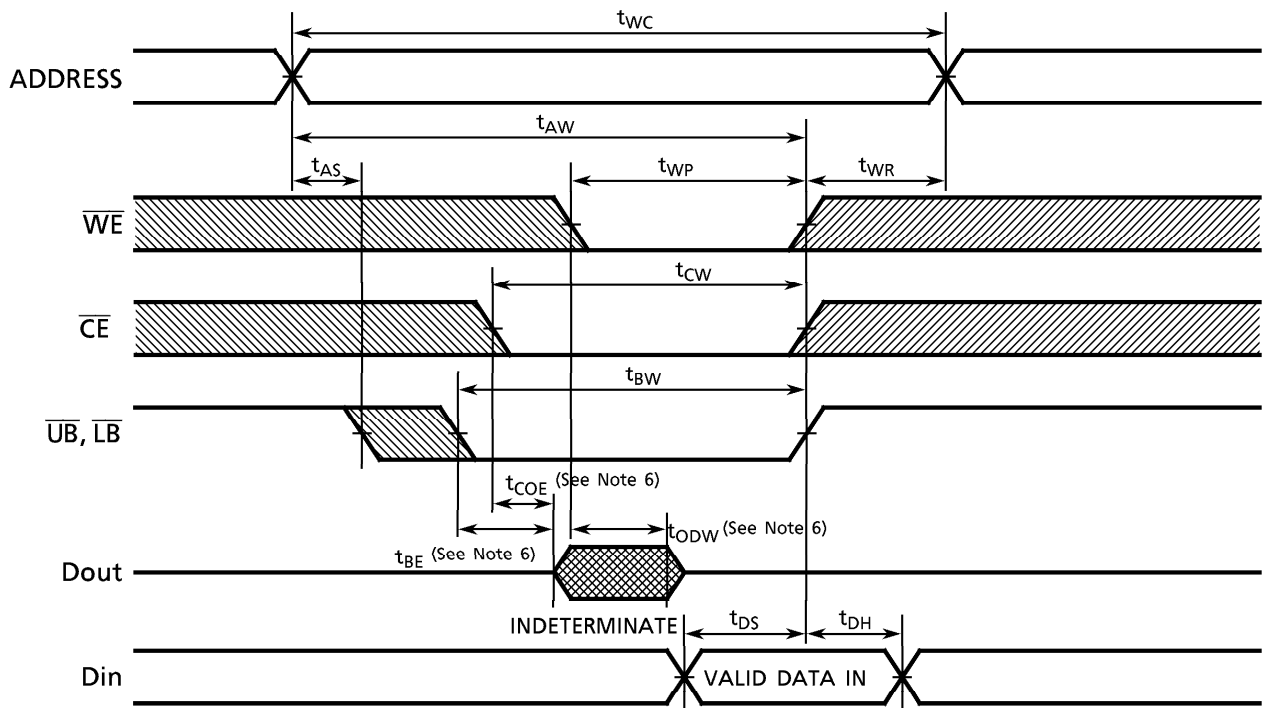
WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 5)

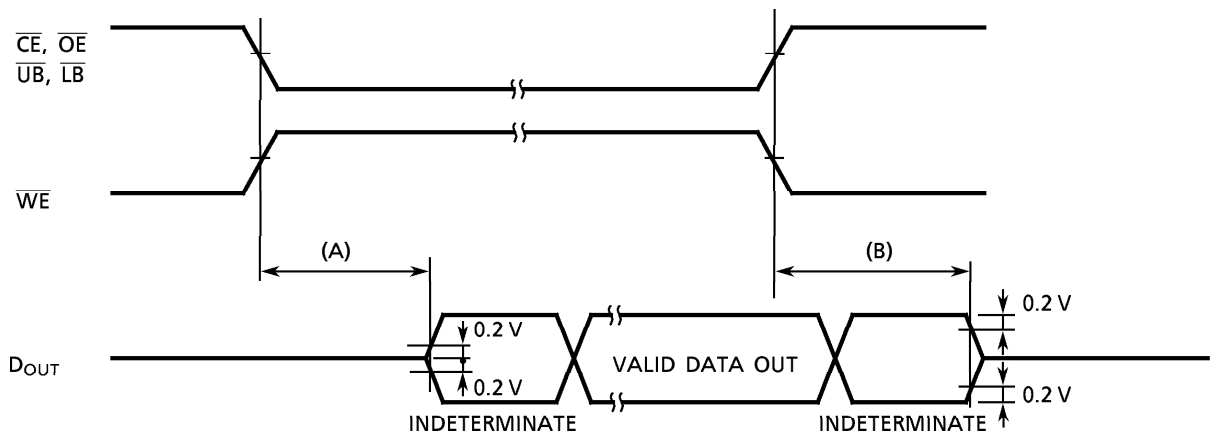


WRITE CYCLE 3 ($\overline{\text{UB}}, \overline{\text{LB}}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (T_a) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

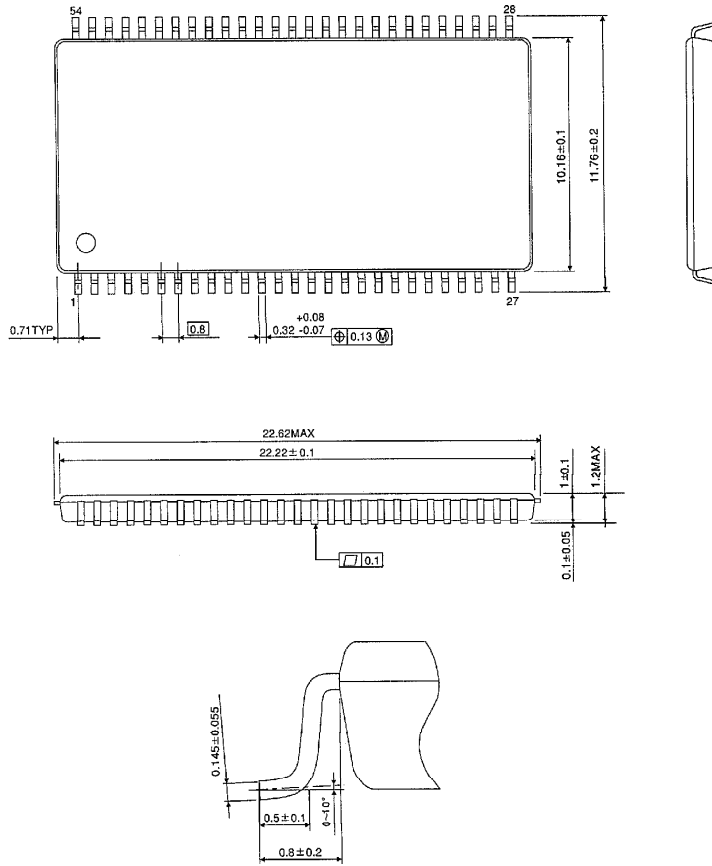
- (2) \overline{WE} remains HIGH for the Read Cycle.
- (3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.
- (4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.
- (5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (6) The parameters specified below are measured using the load shown in Fig. 1.
 - (A) $t_{COE}, t_{OEE}, t_{BE}, t_{OEw}$ Output Enable Time
 - (B) $t_{COD}, t_{ODO}, t_{BD}, t_{ODw}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 54-P-400-0.80B)

Unit in mm



Weight : 0.55g (Typ)