

SILICON GATE CMOS

65,536 WORD x 18 BIT CMOS STATIC RAM

Description

The TC55V1864J/FT is a 1,179,648 bit high speed CMOS static random access memory organized as 65,536 words by 18 bits and operated from a single 3.3V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55V1864J/FT features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC55V1864J/FT is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are LVTTTL compatible.

The TC55V1864J/FT is available in a 400mil width, 44-pin plastic SOJ and thin small outline package (forward type) suitable for high density surface assembly.

Features

- Fast access time
 - TC55V1864J/FT -10 10ns (max.)
 - TC55V1864J/FT -12 12ns (max.)
 - TC55V1864J/FT -15 15ns (max.)

- Low power dissipation

Cycle Time	10	12	15	20	30	ns
Operation (max.)	260	220	200	180	150	mA

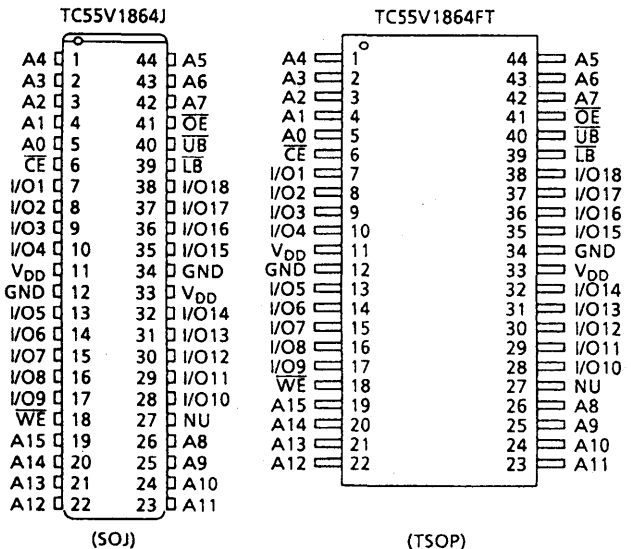
- Standby: 1mA (max.)
- Single 3.3V power supply: 3.3V±0.3V
- Fully static operation
- Inputs and outputs LVTTTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package
 - TC55V1864J: SOJ44-P-400
 - TC55V1864FT: TSOP44-P-400

Pin Names

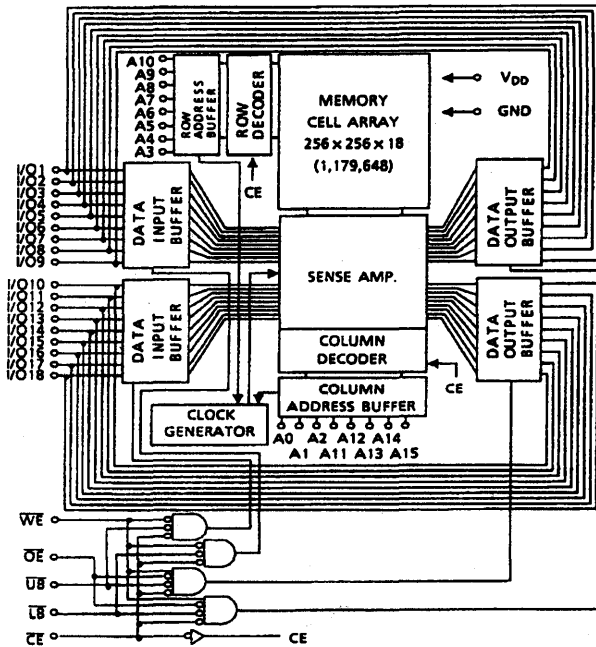
A0 ~ A15	Address Inputs
I/O1 ~ I/O18	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V _{DD}	Power (+3.3V)
GND	Ground
NU*	Not Usable (Input)

* The NU pin must be kept electronically open, pulled down to GND, or less than 0.8V. Applying a voltage greater than 0.8V to the NU pin is prohibited.

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 ~ I/O9	I/O10 ~ I/O18	POWER
Read		L	L	H	L	L	Output	Output	I_{DD0}
					H	L	High Impedance	Output	I_{DD0}
					L	H	Output	High Impedance	I_{DD0}
Write		L	*	L	L	L	Input	Input	I_{DD0}
					H	L	High Impedance	Input	I_{DD0}
					L	H	Input	High Impedance	I_{DD0}
Output Disable		L	H	H	*	*	High Impedance	High Impedance	I_{DD0}
		L	*	*	H	H	High Impedance	High Impedance	I_{DD0}
Standby		H	*	*	*	*	High Impedance	High Impedance	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V_{IN}	Input Voltage	-0.5* ~ 4.6	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	1.2	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

** Not yet specified

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V _{IH}	Input High Voltage	2.0	–	V _{DD} + 0.3**	V
V _{IL}	Input Low Voltage	-0.3*	–	0.8	V

*/** Not yet specified

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I _{LI}	Input Leakage Current (except NU Pin)	V _{IN} = 0 ~ V _{DD}	–	–	±1	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 ~ V _{DD}	–	–	±1	μA	
I _{I(NU)}	Input Current (NU Pin)	V _{IN} = 0 ~ 0.8V	-1	–	20	μA	
		V _{IN} = 0 ~ 0.2V	–	–	±1		
V _{OH}	Output High Voltage	I _{OH} = -2mA	2.4	–	–	V	
		I _{OH} = -20μA	V _{DD} - 0.2	–	–		
V _{OL}	Output Low Voltage	I _{OL} = 2mA	–	–	0.4	V	
		I _{OL} = 20μA	–	–	0.2		
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA, Other Inputs = V _{IH} /V _{IL}	t _{cycle} = 10ns	–	–	260	mA
			t _{cycle} = 12ns	–	–	220	
			t _{cycle} = 15ns	–	–	200	
			t _{cycle} = 20ns	–	–	180	
			t _{cycle} = 30ns	–	–	150	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} /V _{IL}	–	–	20	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	–	–	1		

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Read Cycle

SYMBOL	PARAMETER	TC55V1864J/FT -10		TC55V1864J/FT -12		TC55V1864J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{ACC}	Address Access Time	—	10	—	12	—	15	
t_{CO}	\overline{CE} Access Time	—	10	—	12	—	15	
t_{OE}	\overline{OE} Access Time	—	5	—	6	—	8	
t_{BA}	\overline{UB} , \overline{LB} Access Time	—	5	—	6	—	8	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	3	—	
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	3	—	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	—	1	—	1	—	
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	
t_{ODO}	Output Disable Time from \overline{OE}	—	6	—	7	—	8	
t_{BD}	Output Disable Time from \overline{UB} , \overline{LB}	—	6	—	7	—	8	

Write Cycle

SYMBOL	PARAMETER	TC55V1864J/FT -10		TC55V1864J/FT -12		TC55V1864J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	9	—	
t_{CW}	Chip Enable to End of Write	9	—	10	—	11	—	
t_{BW}	\overline{UB} , \overline{LB} Enable to End of Write	9	—	10	—	11	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Setup Time	6	—	7	—	8	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

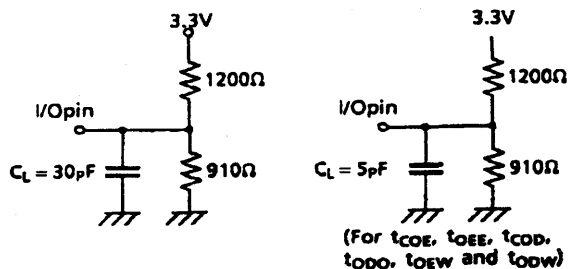
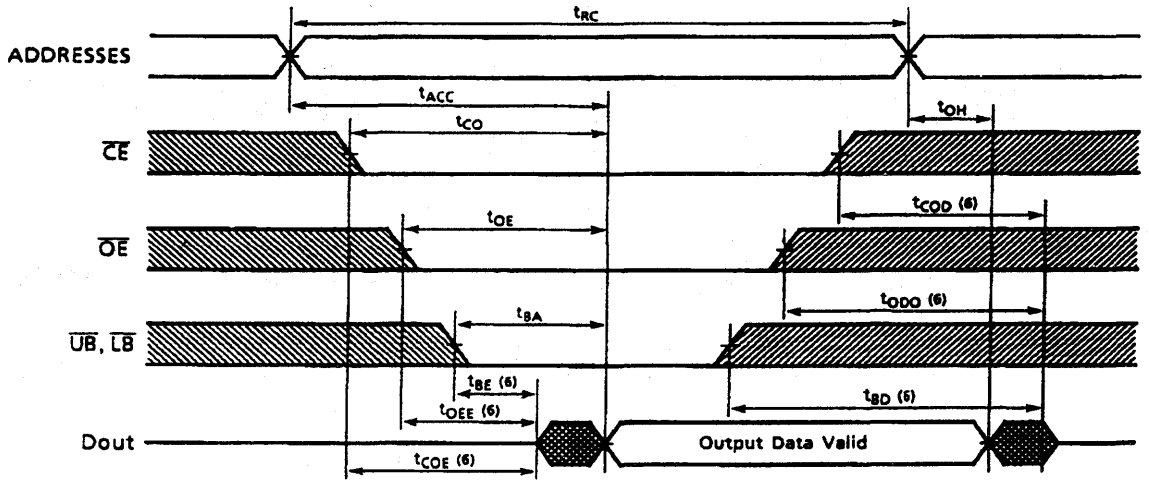


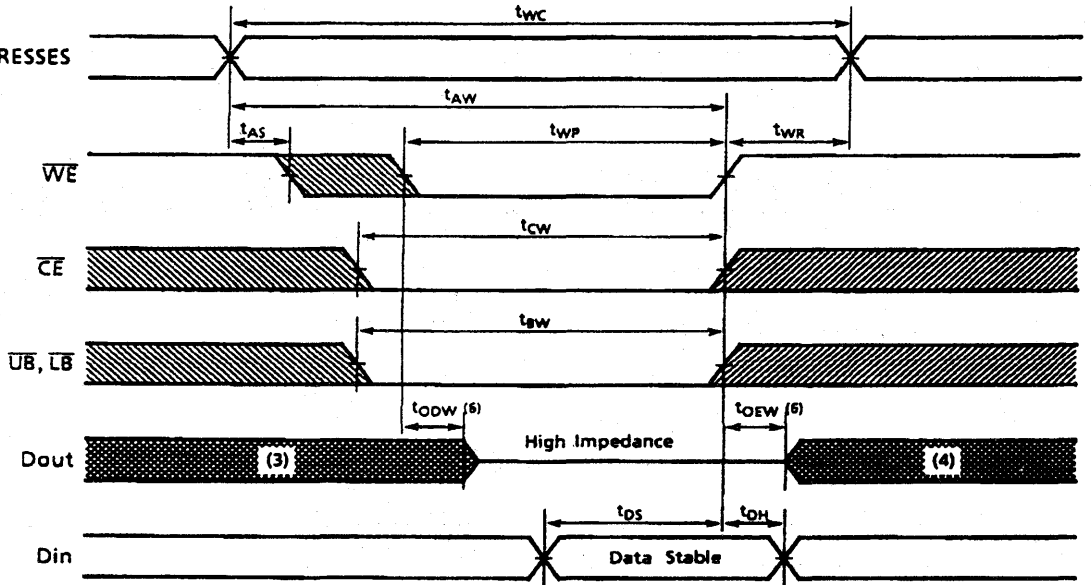
Figure 1.

Timing Waveforms

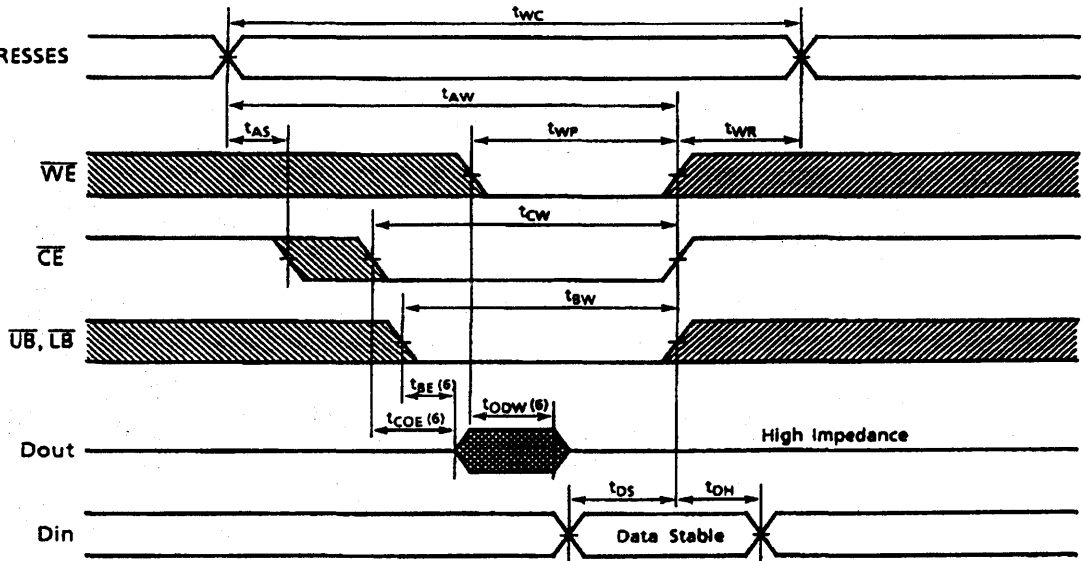
Read Cycle ⁽²⁾



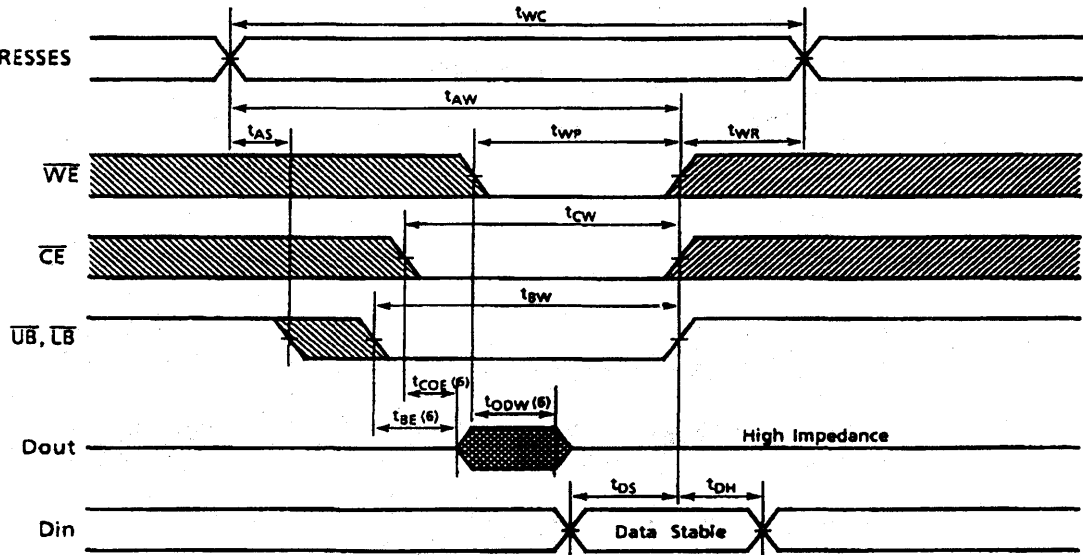
Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)



Write Cycle 2⁽⁵⁾ (\overline{CE} Controlled)



Write Cycle 3⁽⁵⁾ (\overline{UB} , \overline{LB} Controlled)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , t_{BE} , t_{OEw} Output Enable Time
 (B) t_{COD} , t_{ODO} , t_{BD} , t_{ODw} Output Disable Time

