**TENTATIVE** TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

# 131,072-WORD BY 16-BIT STATIC RAM

## DESCRIPTION

The TC55V2161FT is a 2,097,152-bit static random access memory (SRAM) organized as 131,072 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 1 $\mu$A standby current (for the L-Version $V_{DD}$ = 3V, Ta = 25°C) when chip enable ($\overline{CE}$) is asserted high or chip select (CS) is asserted low. There are three control inputs. $\overline{CE}$ is used to select the device and for data retention control, CS is used for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V2161FT is available in a plastic 44-pin thin-small-outline package (TSOP).

## FEATURES

- Low-power dissipation
  Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.7 to 3.6V
- Power down features using $\overline{CE}$ and CS
- Data retention supply voltage of 2 to 3.6V
- Direct TTL compatibility for all inputs and outputs
- Standby current (Ta = 25°C, maximum)

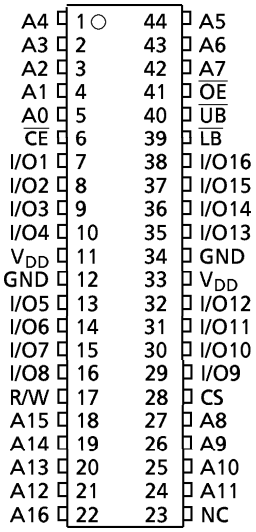
| | TC55V2161FT | |
|---|---|---|
| | -85, -10 | -85L, -10L |
| 3.6V | 3 $\mu$A | 1.4 $\mu$A |
| 3.0V | 2 $\mu$A | 1 $\mu$A |

- Access Times (maximum):

| | TC55V2161FT | |
|---|---|---|
| | -85, -85L | -10, -10L |
| Access Time | 85 ns | 100 ns |
| $\overline{CE}$ Access Time | 85 ns | 100 ns |
| $\overline{OE}$ Access Time | 45 ns | 50 ns |

- Package:
  TSOP II 44-P-400-0.80 (FT) (Weight : 0.45g typ)

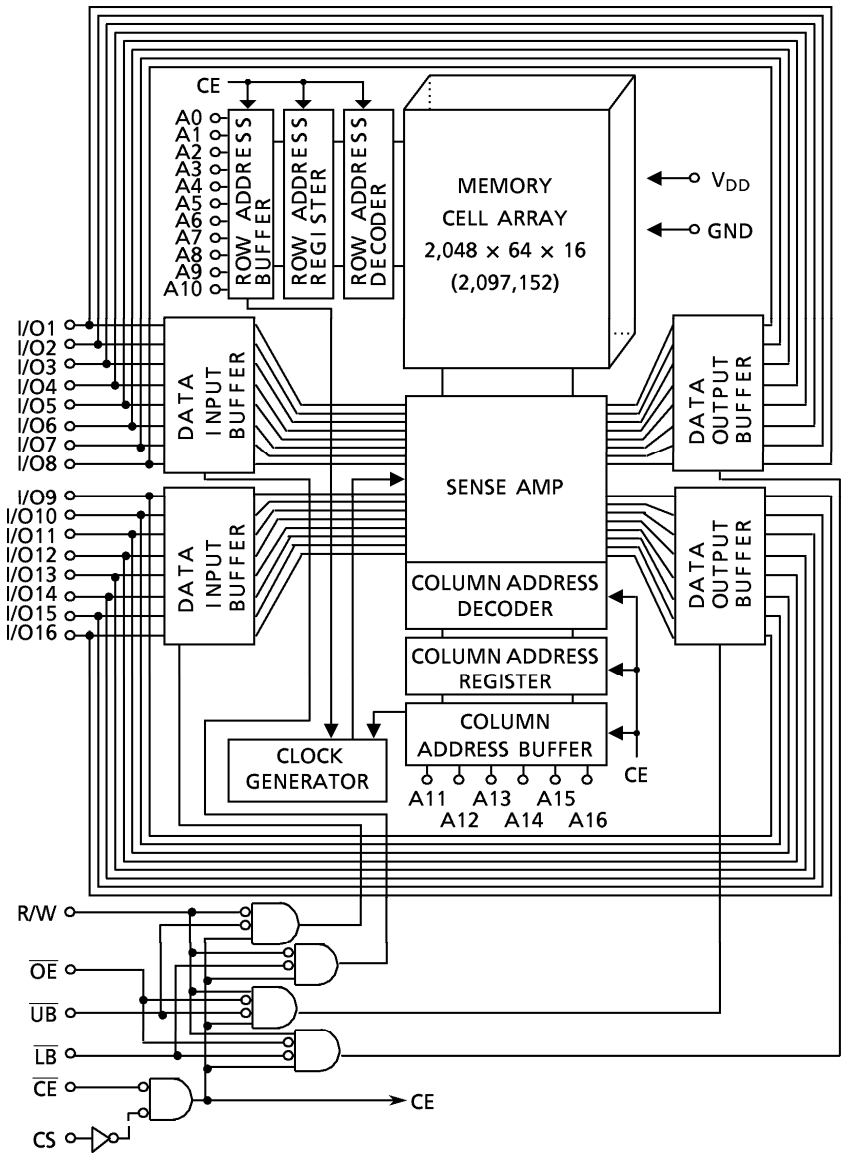
## PIN ASSIGNMENT (TOP VIEW)




## PIN NAMES

| | |
|---|---|
| A0 to A16 | Address Inputs |
| $\overline{CE}$ | Chip Enable Input |
| CS | Chip Select Input |
| R/W | Read / Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{LB}$, $\overline{UB}$ | Data Byte Control Inputs |
| I/O1 to I/O16 | Data Inputs / Outputs |
| $V_{DD}$ | Power |
| GND | Ground |
| NC | No Connection |

## BLOCK DIAGRAM




## OPERATING MODE

| MODE | $\overline{CE}$ | CS | $\overline{OE}$ | R/W | $\overline{LB}$ | $\overline{UB}$ | I/O1 to I/O8 | I/O9 to I/O16 | POWER |
|---|---|---|---|---|---|---|---|---|---|
| Read | L | H | L | H | L | L | $D_{OUT}$ | $D_{OUT}$ | $I_{DDO}$ |
| | | | | | H | L | High-Z | $D_{OUT}$ | $I_{DDO}$ |
| | | | | | L | H | $D_{OUT}$ | High-Z | $I_{DDO}$ |
| Write | L | H | × | L | L | L | $D_{IN}$ | $D_{IN}$ | $I_{DDO}$ |
| | | | | | H | L | High-Z | $D_{IN}$ | $I_{DDO}$ |
| | | | | | L | H | $D_{IN}$ | High-Z | $I_{DDO}$ |
| Output Deselect | L | H | H | H | × | × | High-Z | High-Z | $I_{DDO}$ |
| | | | × | × | H | H | | | |
| CS Standby | × | L | × | × | × | × | High-Z | High-Z | $I_{DDS}$ |
| Standby | H | × | × | × | × | × | High-Z | High-Z | $I_{DDS}$ |

Note: × = don't care. H = logic high. L = logic low.

## MAXIMUM RATINGS

| SYMBOL | RATING | VALUE | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | − 0.3 to 4.6 | V |
| $V_{IN}$ | Input Voltage | − 0.3 * to 4.6 | V |
| $V_{I/O}$ | Input/Output Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $P_D$ | Power Dissipation | 0.8 | W |
| $T_{solder}$ | Soldering Temperature (10 s) | 260 | °C |
| $T_{strg}$ | Storage Temperature | − 55 to 150 | °C |
| $T_{opr}$ | Operating Temperature | 0 to 70 | °C |

* − 3.0 V when measured at a pulse width of 30 ns.

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 2.7 | − | 3.6 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | − | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | − 0.3 * | − | 0.8 | V |
| $V_{DH}$ | Data Retention Supply Voltage | 2.0 | − | 3.6 | V |

* − 3.0 V when measured at a pulse width of 30 ns.

## DC CHARACTERISTICS (Ta = 0° to 70°C, $V_{DD}$ = 2.7 to 3.6V)

| SYMBOL | PARAMETER | TEST CONDITION | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0 V to $V_{DD}$ | | | | | − | − | ± 1.0 | μA |
| $I_{OH}$ | Output High Current | $V_{OH}$ = $V_{DD}$ − 0.5 V | | | | | − 0.5 | − | − | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4 V | | | | | 2.1 | − | − | mA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE}$ = $V_{IL}$ or CS = $V_{IH}$ or R/W = $V_{IL}$<br>$V_{OUT}$ = 0 V to $V_{DD}$ | | | | | − | − | ± 1.0 | μA |
| $I_{DDO1}$ | Operating Current | $\overline{CE}$ = $V_{IL}$ and CS = $V_{IH}$ and R/W = $V_{IH}$ and $I_{OUT}$ = 0 mA<br>Other Input = $V_{IH}$/$V_{IL}$ | $V_{DD}$ = 3 V ± 10% | Tcycle | min | | − | − | 55 | mA |
| | | | | | 1 μs | | − | − | 10 | |
| | | | $V_{DD}$ = 3.3 V ± 0.3 V | Tcycle | min | | − | − | 60 | |
| | | | | | 1 μs | | − | − | 12 | |
| $I_{DDO2}$ | | $\overline{CE}$ = 0.2 V and<br>CS = $V_{DD}$ − 0.2 V and<br>R/W = $V_{DD}$ − 0.2 V, $I_{OUT}$ = 0 mA<br>Other Inputs = $V_{DD}$ − 0.2 V/0.2 V | $V_{DD}$ = 3 V ± 10% | Tcycle | min | | − | − | 45 | |
| | | | | | 1 μs | | − | − | 5 | |
| | | | $V_{DD}$ = 3.3 V ± 0.3 V | Tcycle | min | | − | − | 50 | |
| | | | | | 1 μs | | − | − | 6 | |
| $I_{DDS1}$ | Standby Current | $\overline{CE}$ = $V_{IH}$ or CS = $V_{IL}$ | | | | | − | − | 2 | mA |
| $I_{DDS2}$ (Note) | | $\overline{CE}$ = $V_{DD}$ − 0.2 V<br>or CS = 0.2 V<br>$V_{DD}$ = 2.0 to 3.6 V | $V_{DD}$ = 3V ± 10% | Ta = 25°C | -85, -10 | | − | 1 | 2.5 | μA |
| | | | | | -85L, -10L | | − | 0.5 | 1.2 | |
| | | | | Ta = 0° to 70°C | -85, -10 | | − | − | 30 | |
| | | | | | -85L, -10L | | − | − | 20 | |
| | | | $V_{DD}$ = 3.3V ± 0.3V | Ta = 25°C | -85, -10 | | − | 1.5 | 3 | |
| | | | | | -85L, -10L | | − | 0.7 | 1.4 | |
| | | | | Ta = 0° to 70°C | -85, -10 | | − | − | 35 | |
| | | | | | -85L, -10L | | − | − | 25 | |
| | | | $V_{DD}$ = 3V | Ta = 25°C | -85, -10 | | − | 1 | 2 | |
| | | | | | -85L, -10L | | − | 0.5 | 1 | |
| | | | | Ta = 0° to 40°C | -85, -10 | | − | − | 5 | |
| | | | | | -85L, -10L | | − | − | 3 | |
| | | | | Ta = 0° to 70°C | -85, -10 | | − | − | 25 | |
| | | | | | -85L, -10L | | − | − | 15 | |

Note: In standby mode with $\overline{CE} \geqq V_{DD} - 0.2V$, these limits are assured for the condition $CS \geqq V_{DD} - 0.2V$ or $CS \leqq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = GND | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = GND | 10 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, $V_{DD}$ = 2.7 to 3.6V)

### READ CYCLE

| SYMBOL | PARAMETER | TC55V2161FT | | | | UNIT |
|---|---|---|---|---|---|---|
| | | -85, -85L | | -10, -10L | | |
| | | MIN | MAX | MIN | MAX | |
| $t_{RC}$ | Read Cycle Time | 85 | – | 100 | – | ns |
| $t_{ACC}$ | Address Access Time | – | 85 | – | 100 | |
| $t_{CO}$ | Chip Enable Access Time | – | 85 | – | 100 | |
| $t_{OE}$ | Output Enable Access Time | – | 45 | – | 50 | |
| $t_{BA}$ | Data Byte Control Access Time | – | 45 | – | 50 | |
| $t_{COE}$ | Chip Enable Low to Output Active | 10 | – | 10 | – | |
| $t_{OEE}$ | Output Enable Low to Output Active | 5 | – | 5 | – | |
| $t_{BE}$ | Data Byte Control Low to Output Active | 5 | – | 5 | – | |
| $t_{OD}$ | Chip Enable High to Output High-Z | – | 30 | – | 35 | |
| $t_{ODO}$ | Output Enable High to Output High-Z | – | 30 | – | 35 | |
| $t_{BD}$ | Data Byte Control High to Output High-Z | – | 30 | – | 35 | |
| $t_{OH}$ | Output Data Hold Time | 10 | – | 10 | – | |

### WRITE CYCLE

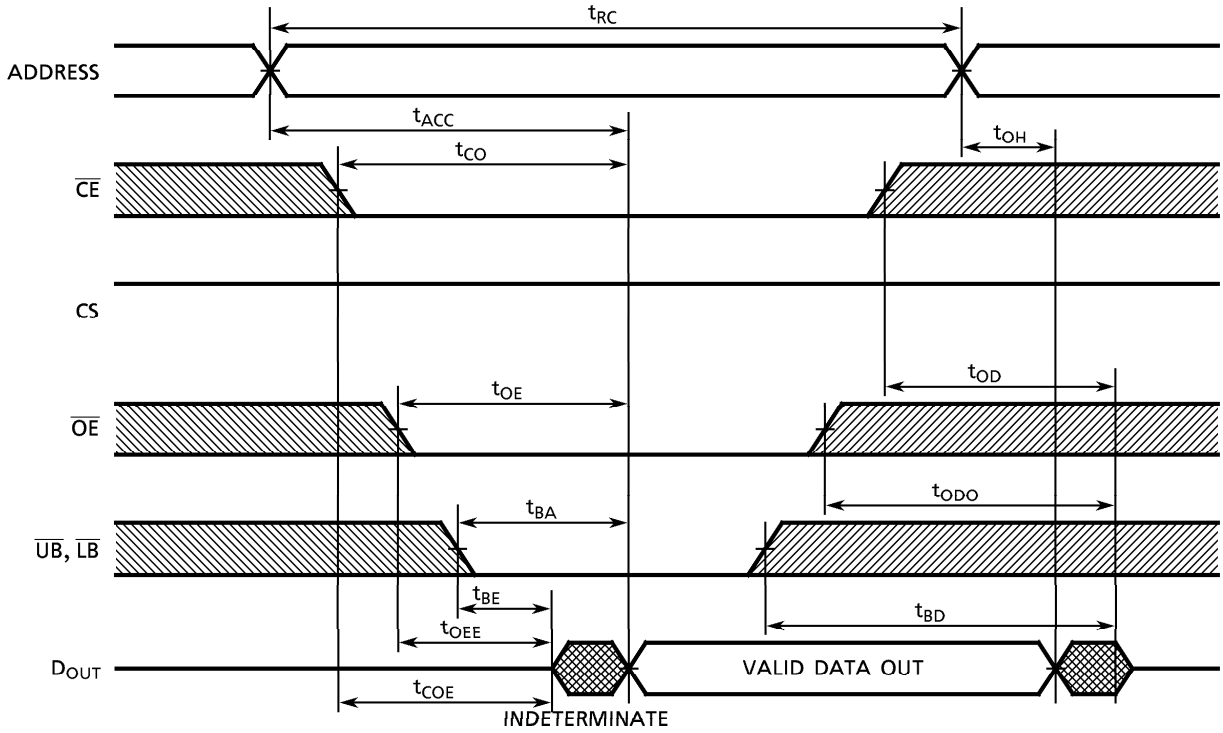
| SYMBOL | PARAMETER | TC55V2161FT | | | | UNIT |
|---|---|---|---|---|---|---|
| | | -85, -85L | | -10, -10L | | |
| | | MIN | MAX | MIN | MAX | |
| $t_{WC}$ | Write Cycle Time | 85 | – | 100 | – | ns |
| $t_{WP}$ | Write Pulse Width | 55 | – | 60 | – | |
| $t_{CW}$ | Chip Enable to End of Write | 75 | – | 80 | – | |
| $t_{BW}$ | Data Byte Control to End of Write | 55 | – | 60 | – | |
| $t_{AS}$ | Address Setup Time | 0 | – | 0 | – | |
| $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | |
| $t_{ODW}$ | R/W Low to Output High-Z | – | 30 | – | 35 | |
| $t_{OEW}$ | R/W High to Output Active | 5 | – | 5 | – | |
| $t_{DS}$ | Data Setup Time | 35 | – | 40 | – | |
| $t_{DH}$ | Data Hold Time | 0 | – | 0 | – | |

### AC TEST CONDITIONS

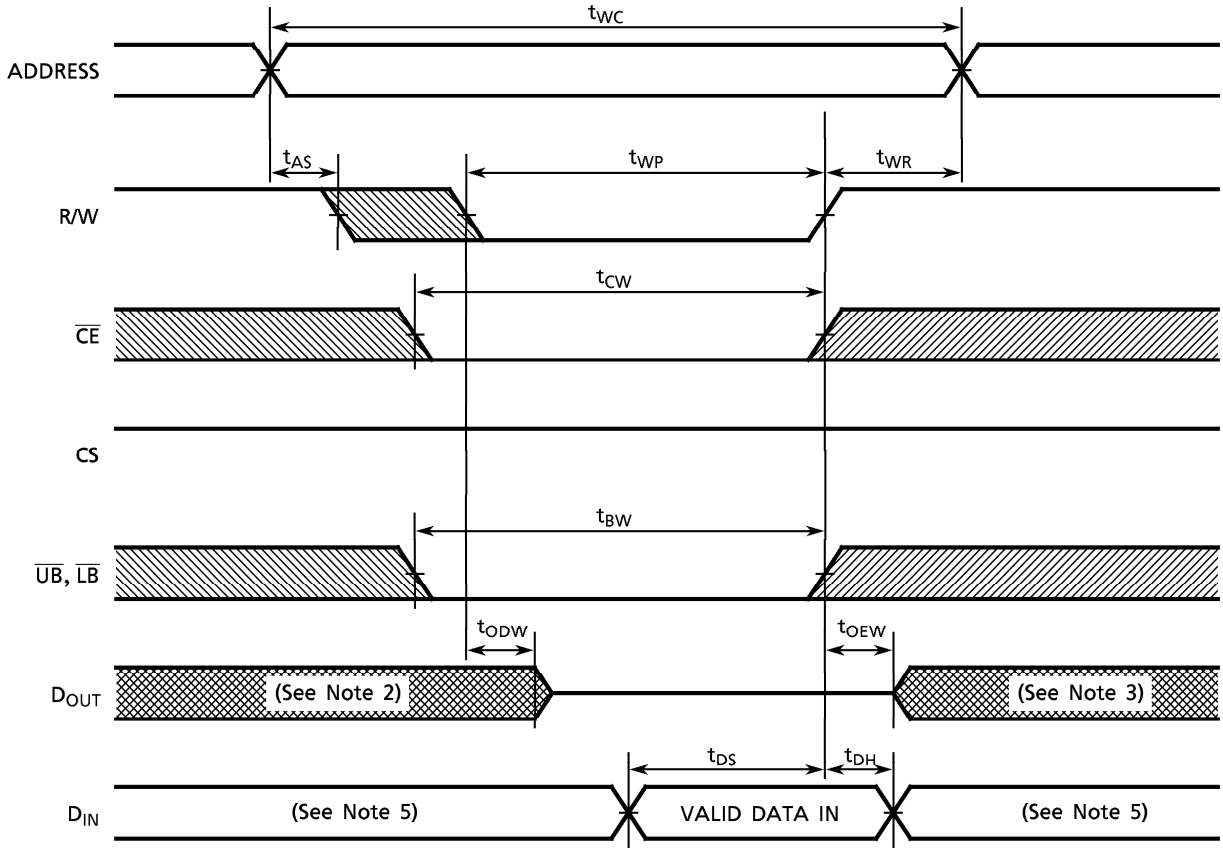
Output load: 100 pF + one TTL gate
Input pulse level: 0.6 V, 2.2 V
Timing measurements: 1.5 V
Reference level: 1.5 V
$t_R$, $t_F$: 5 ns

## TIMING DIAGRAMS

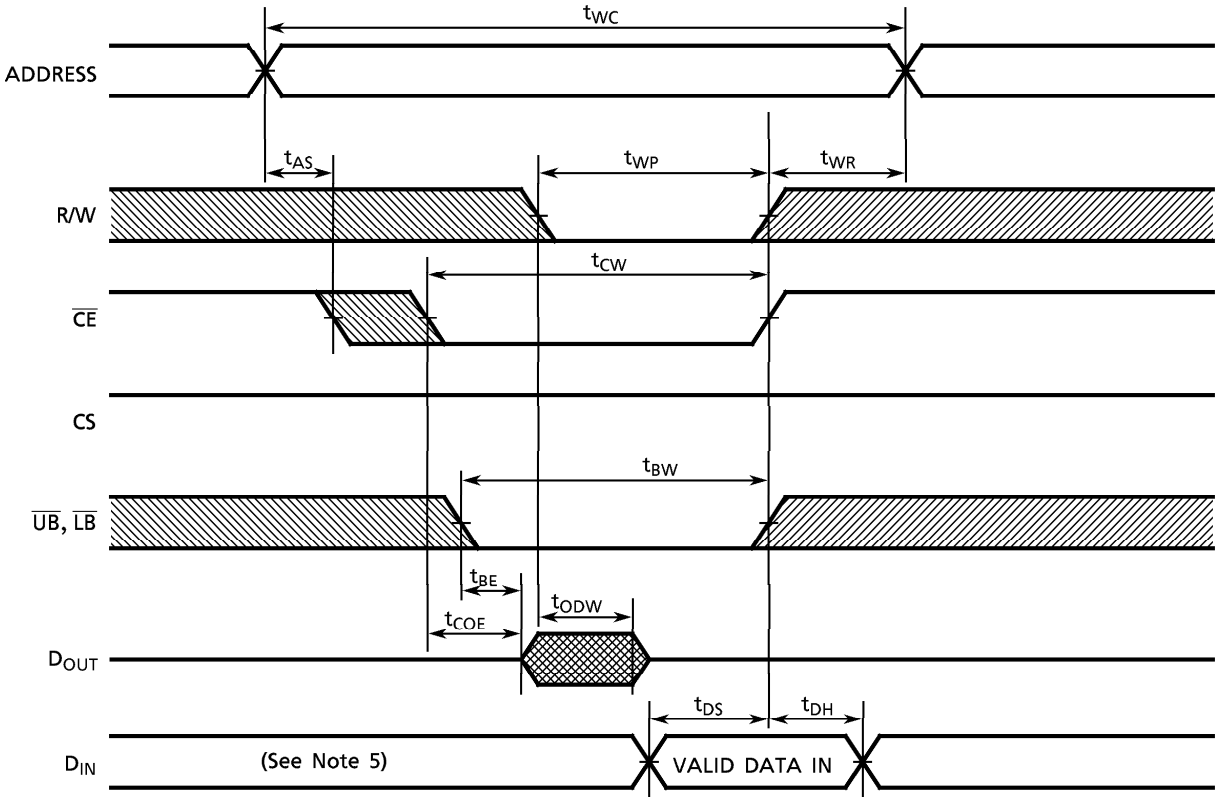
### READ CYCLE (See Note 1)



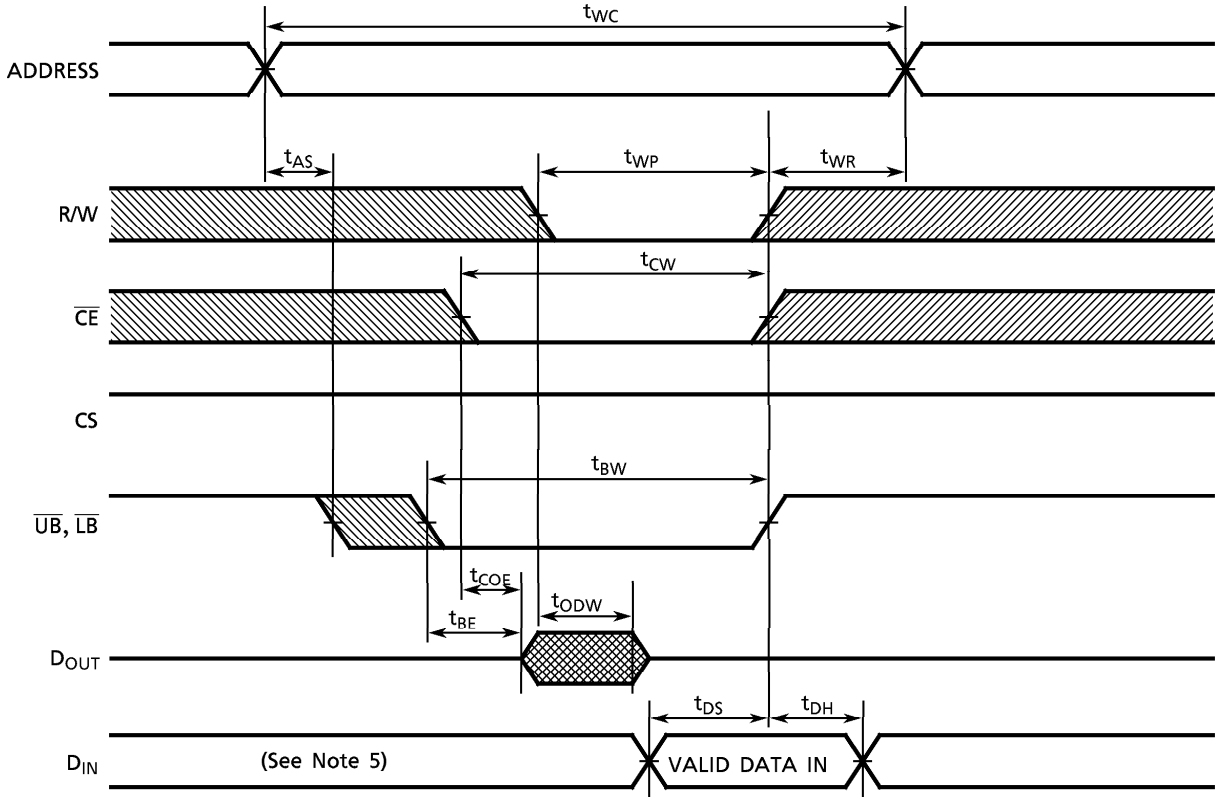

### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)




WRITE CYCLE 3 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE}$ goes LOW (or CS goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE}$ goes HIGH (or CS goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

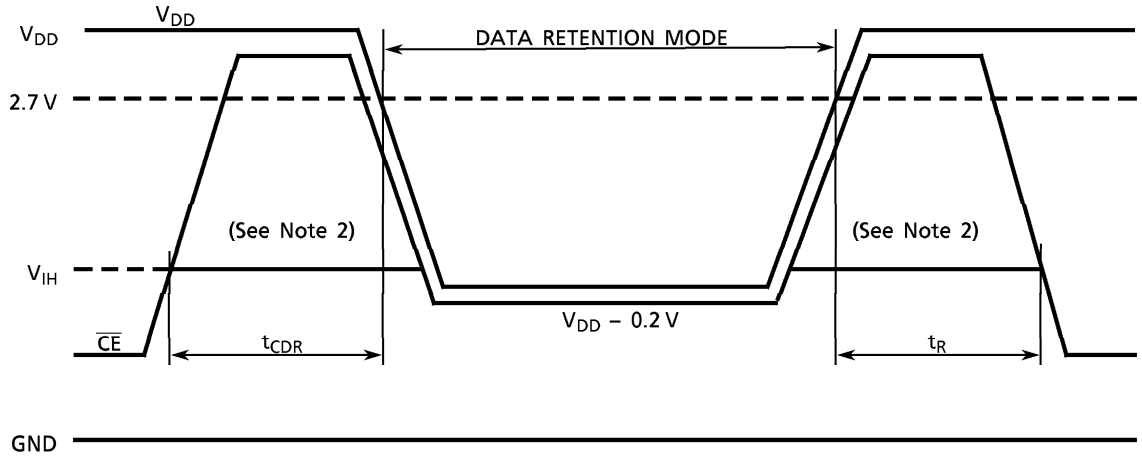
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

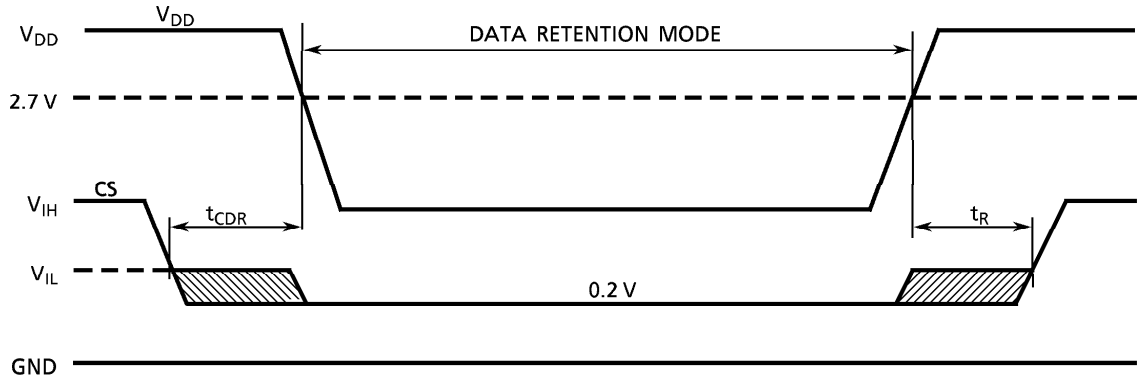
## DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

| SYMBOL | PARAMETER | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{DH}$ | Data Retention Supply Voltage | | | | 2.0 | – | 3.6 | V |
| $I_{DDS2}$ | Standby Current | $V_{DH}$ = 3.0 V | Ta = 0° to 40°C | -85, -10 | – | – | 5 | μA |
| | | | | -85L, -10L | – | – | 3 | |
| | | | Ta = 0° to 70°C | -85, -10 | – | – | 25 | |
| | | | | -85L, -10L | – | – | 15 | |
| | | $V_{DH}$ = 3.6 V | Ta = 0° to 70°C | -85, -10 | – | – | 35 | |
| | | | | -85L, -10L | – | – | 25 | |
| $t_{CDR}$ | Chip Deselect to Data Retention Mode Time | | | | 0 | – | – | nS |
| $t_R$ | Recovery Time | | | | 5 | – | – | mS |

## $\overline{CE}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CS CONTROLLED DATA RETENTION MODE (See Note 3)



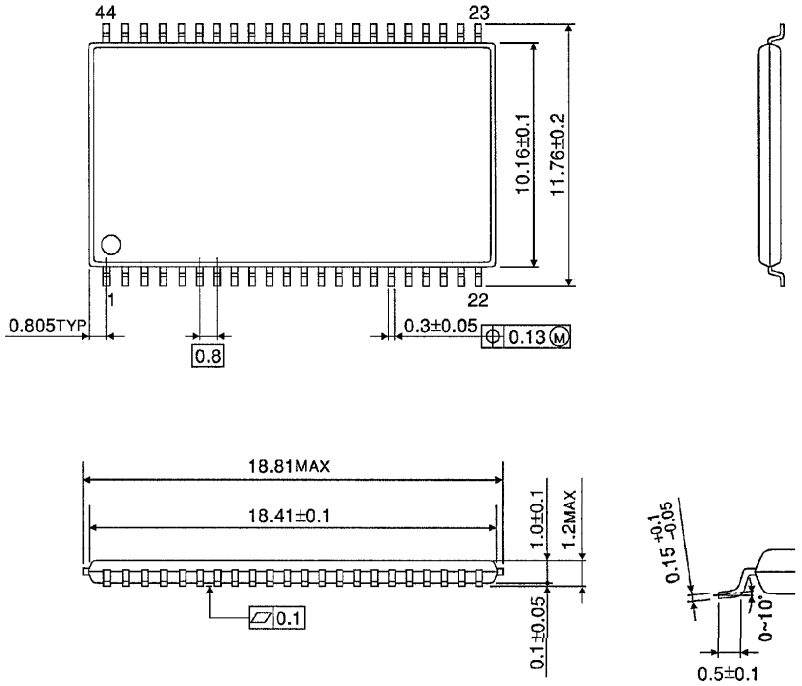

Note: (1) In $\overline{CE}$ controlled data retention mode, minimum standby current mode is entered when CS $\leqq$ 0.2 V or CS $\geqq$ $V_{DD}$ − 0.2 V.

(2) When $\overline{CE}$ is operating at the $V_{IH}$ level (2.0 V), the operating current is given by $I_{DDS1}$ during the transition of $V_{DD}$ from 3.6 to 2.2 V.

(3) In CS controlled data retention mode, minimum standby current mode is entered when CS $\leqq$ 0.2 V.

PACKAGE DIMENSIONS (TSOPII 44-P-400-0.80)

Units in mm




Weight: 0.45 g (typ)

Search

Select One

DRAM Components
DRAM Components (Archive)
DRAM Modules
DRAM Modules (Archive)
Flash - NOR
Flash - NAND 5V
Flash - NAND 3.3V
Flash - SmartMedia
Multi-Chip Package
SRAM - Low Power Asynchronous
SRAM - High Speed Asynchronous
SRAM - High Speed Synchronous
SRAM - Announced EOL Parts



# SRAM - Low Power Asynchronous

Press Releases |

PRODUCTS

| Available Products | Organization | Speed (ns) | Package | Functionality | Capacity |
|---|---|---|---|---|---|
| TC551001C, -L | 128Kx8 | 55,70,85 | DIP,SOP,TSOP,STSOP, and reverses | Standard and Low Power | 1Mb |
| TC551001CI, -L | 128Kx8 | 70,85 | DIP,SOP,TSOP, STSOP, and reverses | Industrial Temp, and Ind. Temp with Low Power | 1Mb |
| TC554001A-V | 512Kx8 | 70,85 | SOP, TSOPII, Reverse TSOPII | Low voltage tolerant | 4Mb |
| TC554001AI | 512Kx8 | 70,85 | SOP, TSOPII, Reverse TSOPII | Industrial Temp | 4Mb |
| TC554001AI-V | 512Kx8 | 70,85 | SOP, TSOPII, Reverse TSOPII | Industrial Temp, low voltage tolerant | 4Mb |
| TC55V020 | 256Kx8 | 70,85,100 | TSOPI,BGA | Full CMOS | 2Mb |
| TC55V040 | 512Kx8 | 70,85,100 | TSOPI,BGA | Full CMOS | 4Mb |
| TC55V1001A, -L | 128Kx8 | 85,100 | SOP,TSOP,STSOP and reverses | 3.3V and available in Low Power | 1Mb |
| TC55V1001A, -L | 128Kx8 | 70 | SOP,TSOP,STSOP and reverses | 3.3V and available in Low Power | 1Mb |
| TC55V1001AI, -L | 128Kx8 | 85,100 | SOP,TSOP,STSOP and reverses | Industrial Temp and Low Power | 1Mb |
| TC55V1001AI, -L | 128Kx8 | 70 | SOP,TSOP,STSOP and reverses | Industrial Temp and Low Power | 1Mb |

| | | | | | |
|---|---|---|---|---|---|
| TC55V200 | 128Kx16 | 70,85,100 | TSOPI,BGA | Full CMOS | 2Mb |
| TC55V2001 | 256Kx8 | 85,100 | SOP,TSOP,STSOP, and reverses | 3.3V | 2Mb |
| TC55V2001I | 256Kx8 | 85,100 | SOP,TSOP,STSOP, and reverses | 3.3V, Industrial Temp | 2Mb |
| TC55V2161,-L | 128Kx16 | 85,100 | TSOP | 3.3V | 2Mb |
| TC55V2161I,-L | 128Kx16 | 85,100 | TSOP | 3.3V, Industrial Temp | 2Mb |
| TC55V400 | 256Kx16 | 70,85,100 | TSOPI,BGA | Full CMOS | 4Mb |
| TC55V4000 | 512Kx8 | 70,85 | TSOPI | 32pin,Full CMOS | 4Mb |