

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V8128BJ/BFT is a 1,048,576 bits high speed static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 3.3V supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55V8128BJ/BFT has low power feature with device control using chip enable (\overline{CE}), and has output enable (\overline{OE}) for fast memory access. The TC55V8128BJ/BFT is suitable for use in cache memory where high speed is required, and high speed storage. All inputs and outputs are directly LVTTL compatible.

The TC55V8128BJ/BFT is packaged in 32-pin plastic SOJ and TSOP(0.8mm pitch) with 400 mil width for high density surface assembly.

FEATURES

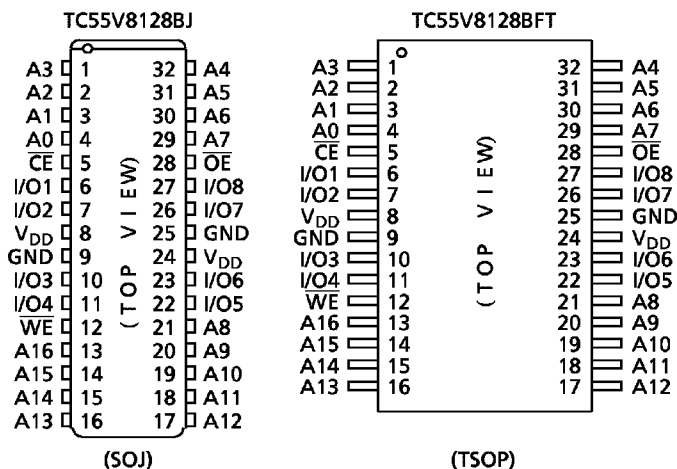
- Fast access time :

TC55V8128BJ/BFT-8	8ns (MAX)
-------------------	-----------
- Low power dissipation

Cycle Time	8	10	12	15	20	ns
Operation (MAX)	230	200	160	140	120	mA

Standby : 2mA (MAX)
- 3.3V single power supply : $3.3V \pm 5\%$
- Fully static operation
- All Inputs and Outputs : LVTTL compatible
- Output buffer control : \overline{OE}
- Package :
 - SOJ32-P-400-1.27A (BJ) (Weight : 1.22gm Typ)
 - TSOP II 32-P-400-0.80C (BFT) (Weight : 0.34gm Typ)

PIN CONNECTION



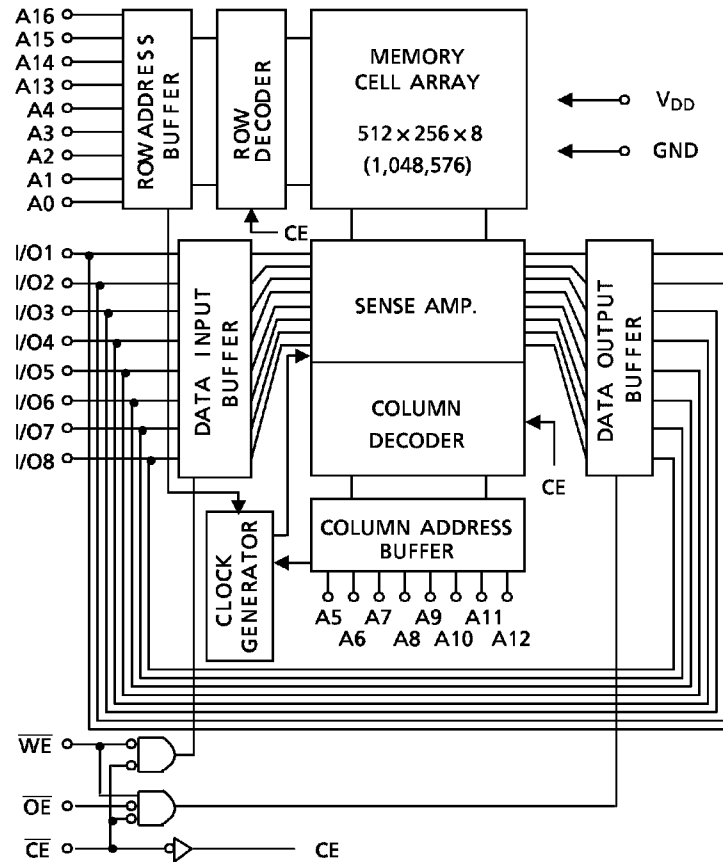
PIN NAMES

A0 to A16	Address Inputs
I/O1 to I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+ 3.3V)
GND	Ground

961001EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	-0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	-0.5* to 4.6	V
V_{IO}	Input/Output Terminal Voltage	-0.5* to $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	0.85	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{strg}	Storage Temperature	-65 to 150	°C
T_{opr}	Operating Temperature	-10 to 85	°C

* : -1.5V with a pulse width of $20\% \cdot t_{RC}$ min (4ns max)

** : $V_{DD} + 1.5V$ with a pulse width of $20\% \cdot t_{RC}$ min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	3.135	3.3	3.465	V
V _{IH}	Input High Voltage	2.0	-	V _{DD} + 0.3**	V
V _{IL}	Input Low Voltage	-0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD} + 1.0V with a pulse width of 20% · t_{RC} min (4ns max)

DC and OPERATING CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 3.3V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current (Except A8, OE pin)	V _{IN} = 0 to V _{DD}	-1	-	1	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 to V _{DD}	-1	-	1	μA	
I _{I (A8, OE)}	Input Leakage Current	V _{IN} = 0 to V _{DD}	-1	-	10	μA	
V _{OH}	Output High Voltage	I _{OH} = -2mA	2.4	-	-	V	
		I _{OH} = -100μA	V _{DD} - 0.2	-	-		
V _{OL}	Output Low Voltage	I _{OL} = 2mA	-	-	0.4		
		I _{OL} = 100μA	-	-	0.2		
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0mA Other Inputs = V _{IH} / V _{IL}	t _{cycle} = 8ns	-	-	230	mA
			t _{cycle} = 10ns	-	-	200	
			t _{cycle} = 12ns	-	-	160	
			t _{cycle} = 15ns	-	-	140	
			t _{cycle} = 20ns	-	-	120	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} / V _{IL}	-	-	50	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	-	-	2		

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 to I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	X	L	Input	I_{DDO}
Outputs Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	X	X	High Impedance	I_{DDS}

X : H or L

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C ⁽¹⁾, $V_{DD} = 3.3\text{V} \pm 5\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55V8128BJ/BFT-8		UNIT
		MIN	MAX	
t_{RC}	Read Cycle Time	8	-	ns
t_{ACC}	Address Access Time	-	8	
t_{CO}	\overline{CE} Access Time	-	8	
t_{OE}	\overline{OE} Access Time	-	4	
t_{OH}	Output Data Hold Time from Address Change	3	-	
t_{COE}	Output Enable Time from \overline{CE}	3	-	
t_{OEE}	Output Enable Time from \overline{OE}	1	-	
t_{COD}	Output Disable Time from \overline{CE}	-	5	
t_{ODO}	Output Disable Time from \overline{OE}	-	5	

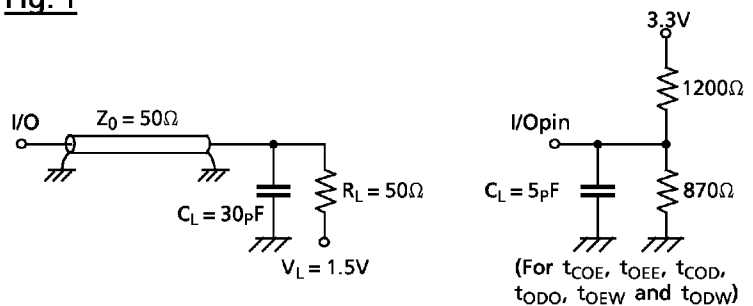
WRITE CYCLE

SYMBOL	PARAMETER	TC55V8128BJ/BFT-8		UNIT
		MIN	MAX	
t_{WC}	Write Cycle Time	8	-	ns
t_{WP}	Write Pulse Width	6	-	
t_{CW}	Chip Enable to End of Write	7	-	
t_{AW}	Address Valid to End of Write	7	-	
t_{AS}	Address Set Up Time	0	-	
t_{WR}	Write Recovery Time	0	-	
t_{DS}	Data Set Up Time	5	-	
t_{DH}	Data Hold Time	0	-	
t_{OEW}	Output Enable Time from \overline{WE}	1	-	
t_{ODW}	Output Disable Time from \overline{WE}	-	5	

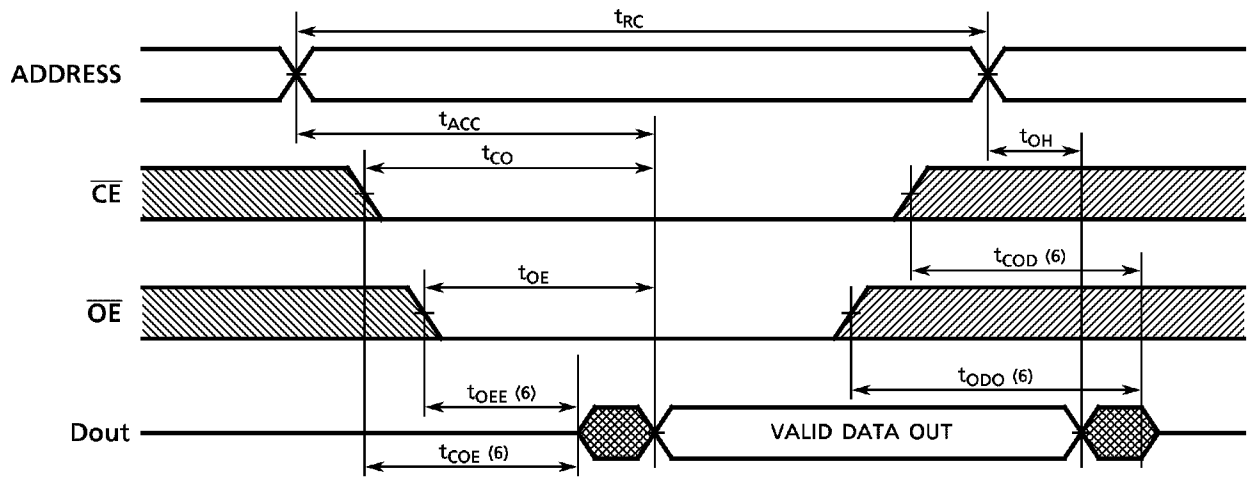
AC TEST CONDITIONS

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

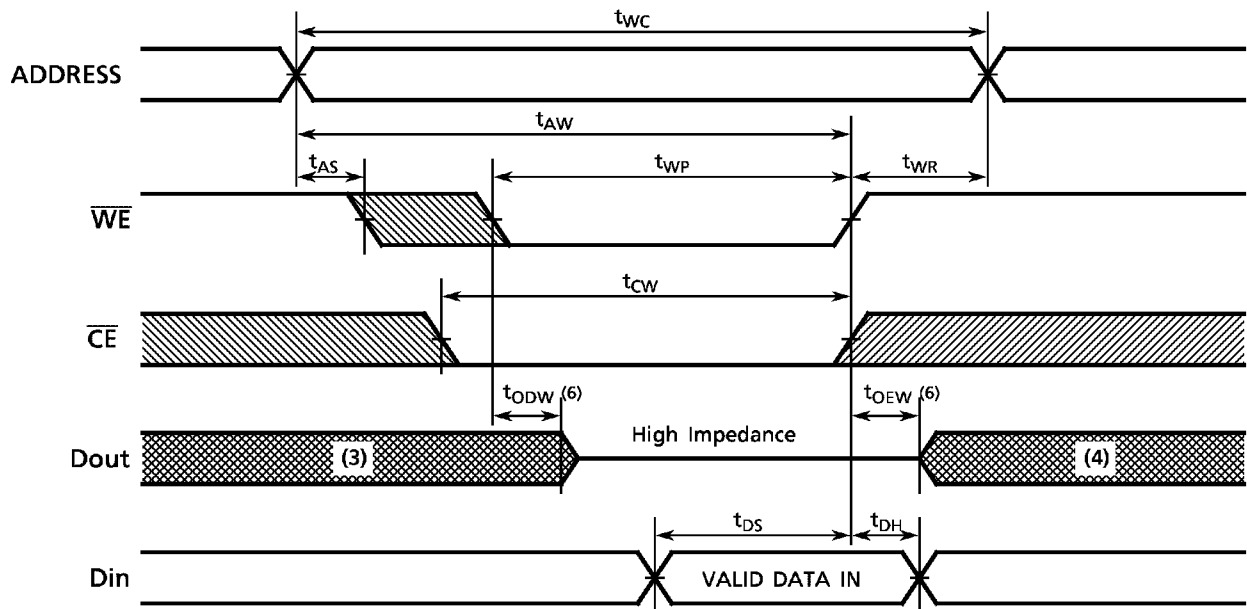
Fig. 1



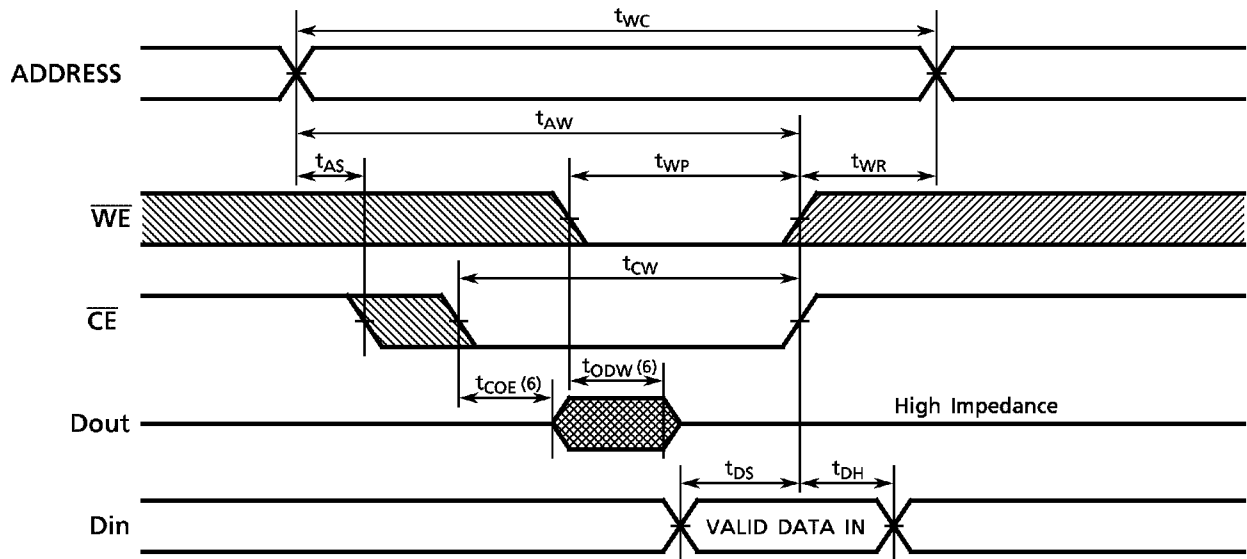
TIMING WAVEFORMS
READ CYCLE (2)



WRITE CYCLE 1 (5) (\overline{WE} Controlled)



WRITE CYCLE 2 (6) (\overline{CE} Controlled)

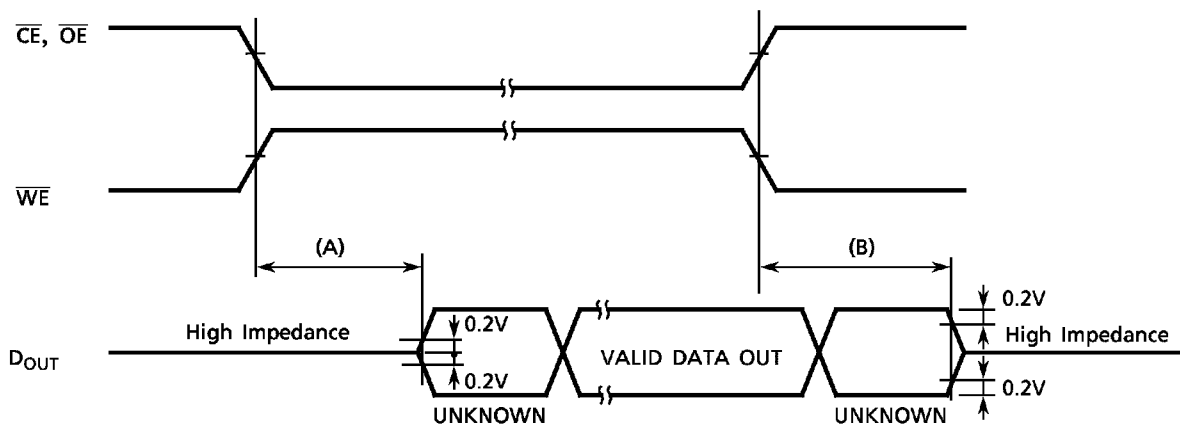


NOTE :

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is High for Read Cycle.
3. Assuming that \overline{CE} Low transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
4. Assuming that \overline{CE} High transition occurs coincident with or prior \overline{WE} High transition, Outputs remain in a high impedance state.
5. Assuming that \overline{OE} is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OE\overline{W}}$ Output Enable Time

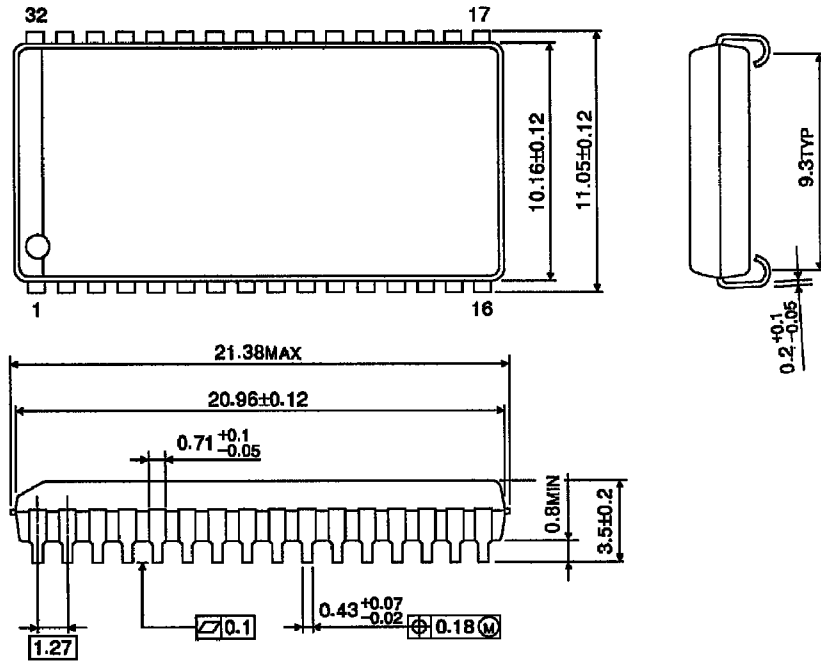
(B) $t_{COD}, t_{ODO}, t_{OD\overline{W}}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ32-P-400-1.27A)

Unit in mm

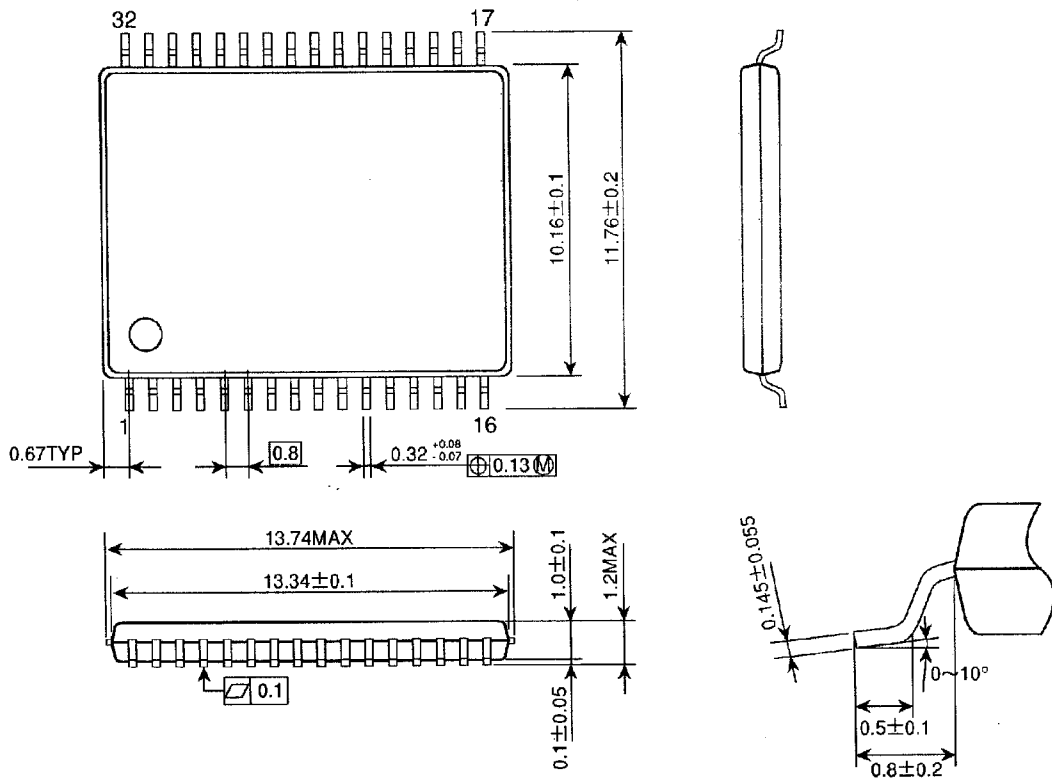


Weight : 1.22g (Typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 32-P-400-0.80C)

Units in mm



Weight: 0.34 g (typ)