TOSHIBA

TC58DVG02A1FT00

TENTATIVE   TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1-GBIT (128M × 8 BITS) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58DVG02A1 is a single 3.3 V 1-Gbit (1,107,296,256) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as 528 bytes × 32 pages × 8192 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages).

The TC58DVG02A1 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization
  Memory cell allay   528 × 256K × 8
  Register   528 × 8
  Page size   528 bytes
  Block size   (16K + 512) bytes
- Modes
  Read, Reset, Auto Page Program,
  Auto Block Erase, Status Read,
  Multi Block Program, Multi Block Erase
- Mode control
  Serial input/output
  Command control

- Power supply V_{CC} = 2.7 V to 3.6 V
- Program/Erase Cycles 1E5 cycle (with ECC)
- Access time
  Cell array to register 25 μs max
  Serial Read Cycle   50 ns min
- Operating current
  Read (50 ns cycle)   10 mA typ.
  Program (avg.)   10 mA typ.
  Erase (avg.)   10 mA typ.
  Standby   50 μA max.
- Package
  TSOPI48-P-1220-0.50 (Weight: g typ.)

PIN ASSIGNMENT (TOP VIEW)

```
NC   □ 1  ○           48 □ NC
NC   □ 2             47 □ NC
NC   □ 3             46 □ NC
NC   □ 4             45 □ NC
NC   □ 5             44 □ I/O8
GND  □ 6             43 □ I/O7
RY/BY □ 7            42 □ I/O6
RE   □ 8             41 □ I/O5
CE   □ 9             40 □ NC
NC   □ 10            39 □ NC
NC   □ 11            38 □ NC
VCC  □ 12            37 □ VCC
VSS  □ 13            36 □ VSS
NC   □ 14            35 □ NC
NC   □ 15            34 □ NC
CLE  □ 16            33 □ NC
ALE  □ 17            32 □ I/O4
WE   □ 18            31 □ I/O3
WP   □ 19            30 □ I/O2
NC   □ 20            29 □ I/O1
NC   □ 21            28 □ NC
NC   □ 22            27 □ NC
NC   □ 23            26 □ NC
NC   □ 24            25 □ NC
```
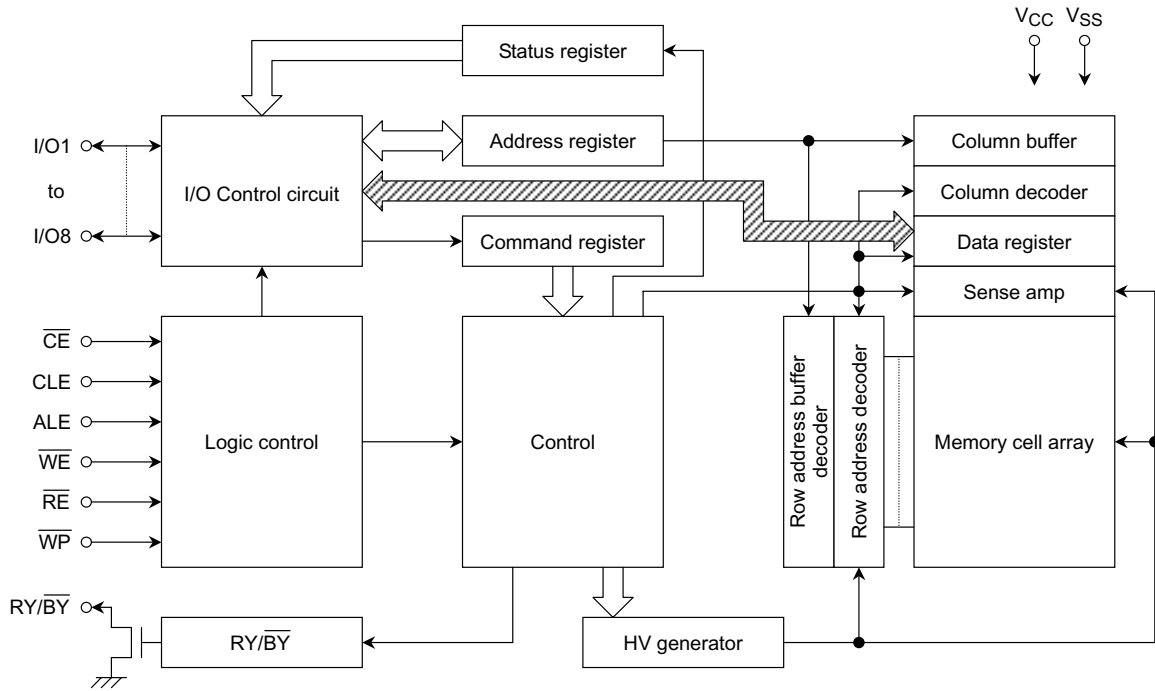
PIN NAMES

Pin	Description
I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
GND	Ground input
V_{CC}	Power supply
V_{SS}	Ground

000707EBA1

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input/Output Voltage	−0.6 V to V_{CC} + 0.3 V ($\leq$ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55 to 150	°C
T_{opr}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	8032	—	8192	Blocks

(1) The TC58DVG02A1 occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document. The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	3.3	3.6	V
V_{IH}	High Level input Voltage	2.0	—	$V_{CC} + 0.3$	V
V_{IL}	Low Level Input Voltage	−0.3*	—	0.8	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	10	30	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO7}	Programming Current	—	—	10	30	mA
I_{CCO8}	Erasing Current	—	—	10	30	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = $V_{IH,}$ $\overline{WP}$ = 0V/V_{CC}	—	—	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0V/V_{CC}	—	10	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V	—	8	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	—	35	ns	
t_{CEA}	$\overline{CE}$ Access Time (Serial Data Access, ID Read)	—	45	ns	
t_{ALEA}	ALE Access Time (ID Read)	—	45	ns	
t_{CEH}	$\overline{CE}$ High Time for Last Address in Serial Read Cycle	100	—	ns	(2)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	—	35	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	—	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	—	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_R	Memory Cell Array to Starting Address	—	25	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	—	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	—	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (When interrupted by $\overline{CE}$ in Read Mode)	—	$1 + t_r (RY/\overline{BY})$	μs	(1) (2)
t_{RST}	Device Reset Time (Read/Program/Erase)	—	6/10/500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3 ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C_L (100 pF) + 1 TTL

Note: (1) $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

(2) Sequential Read is terminated when t$_{CEH}$ is greater than or equal to 100 ns. If the $\overline{RE}$ to $\overline{CE}$ delay is less than 30 ns, RY/$\overline{BY}$ signal stays Ready.
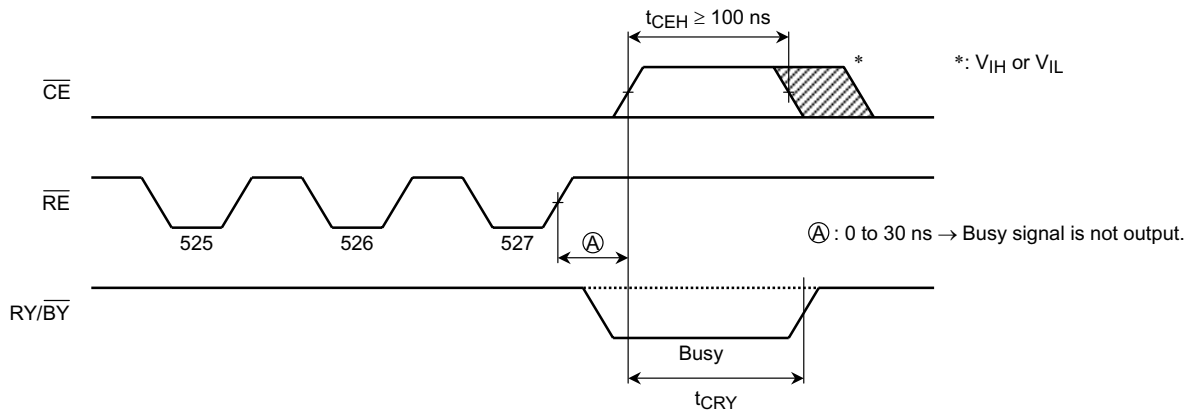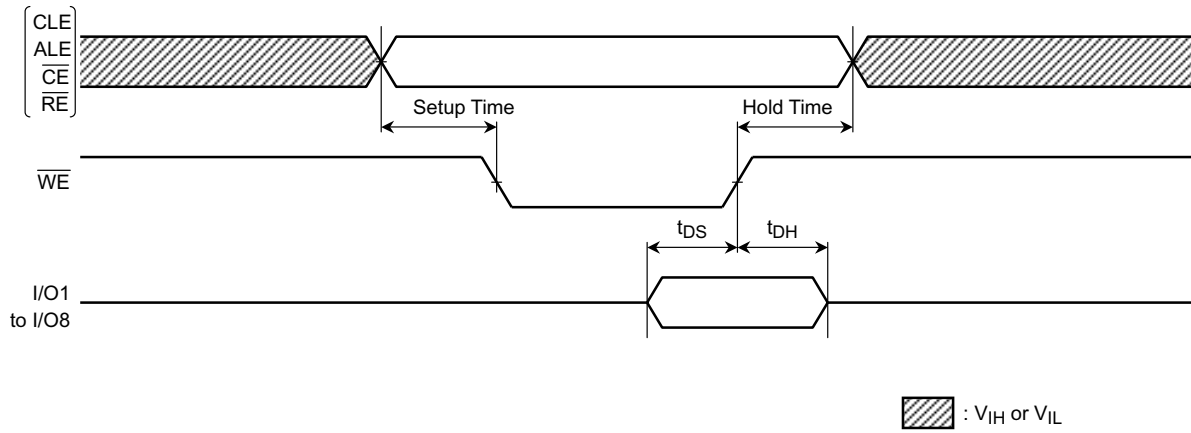

PROGRAMMING AND ERASING CHARACTERISTICS

(Ta = 0° to 70°C, V$_{CC}$ = 2.7 V to 3.6 V)

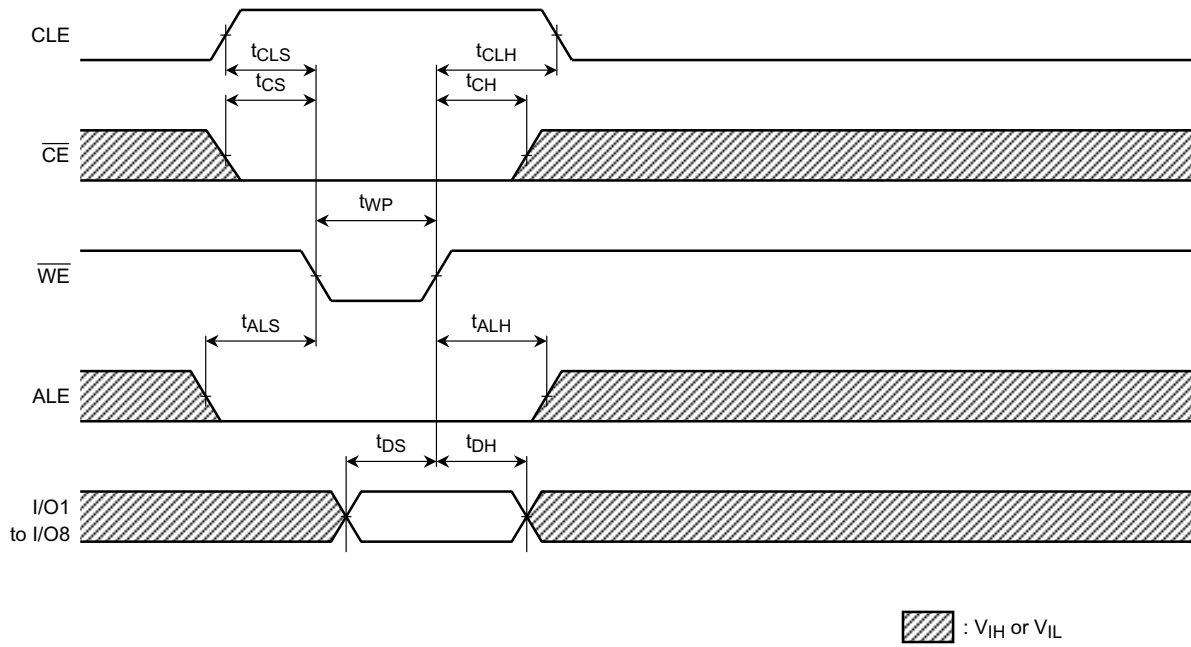| SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t$_{PROG}$	Programming Time	—	200	1000	μs	
t$_{DBSY}$	Dummy Busy Time for Multi Block Programming	—	2	10	μs	
t$_{MBPBSY}$	Multi Block Program Busy Time	—	200	1000	μs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t$_{BERASE}$	Block Erasing Time	—	2	10	ms	

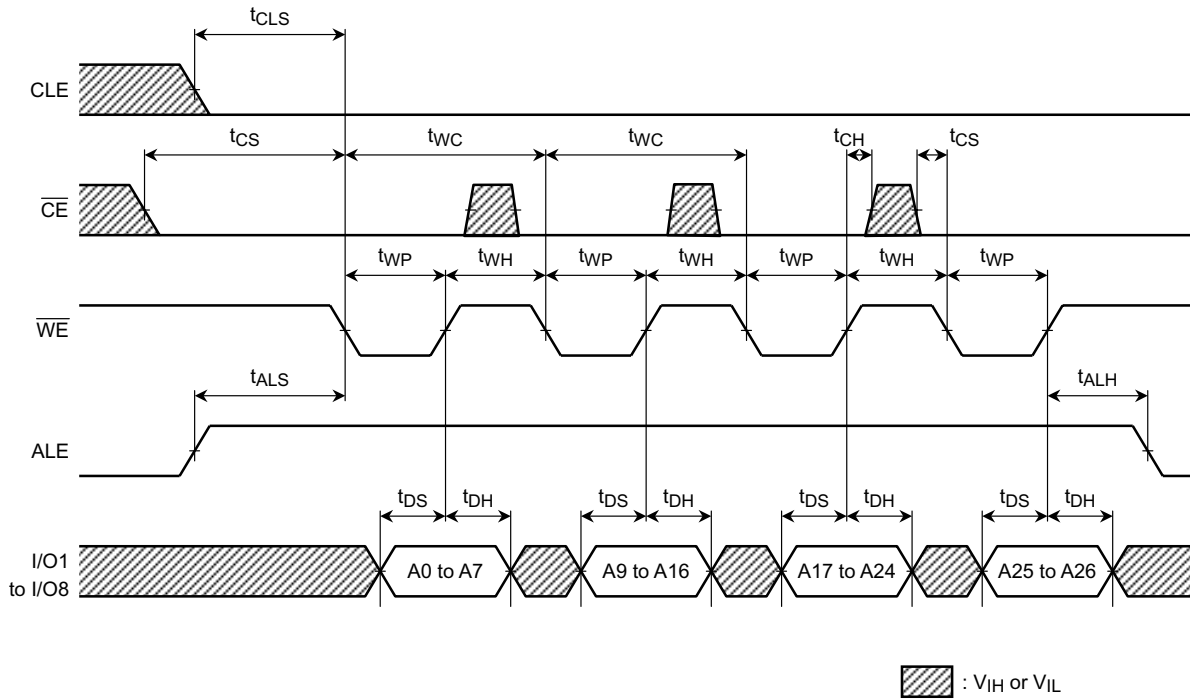(1): Refer to Application Note (12) toward the end of this document.

TIMING DIAGRAMS
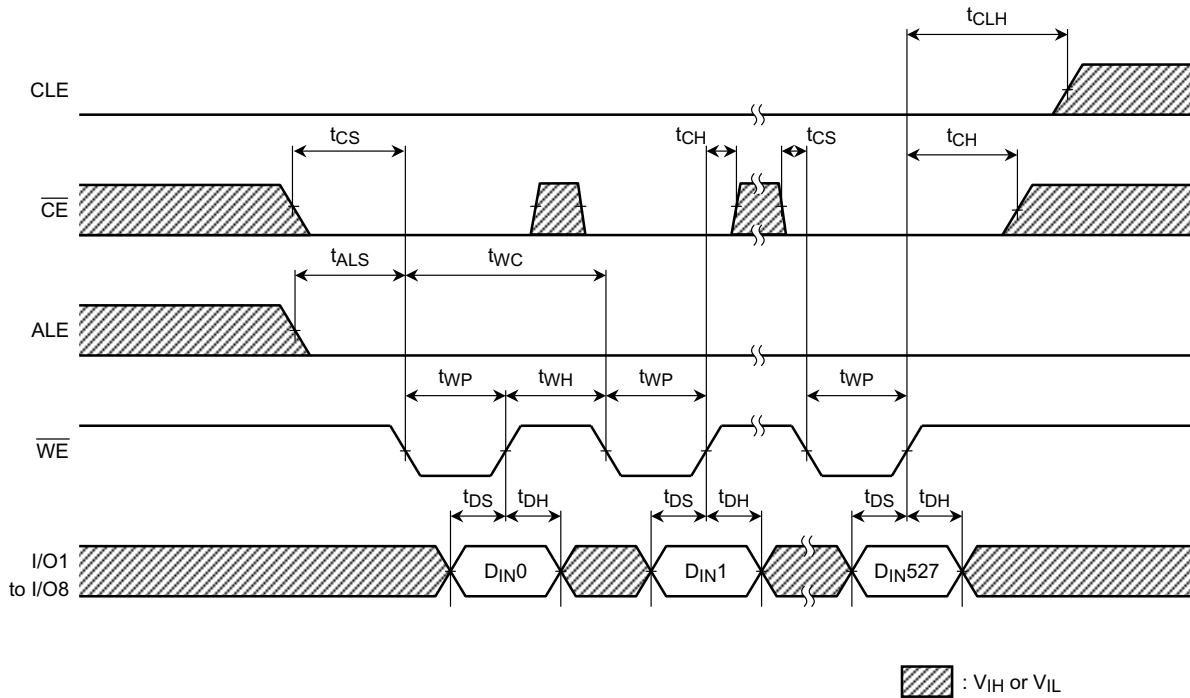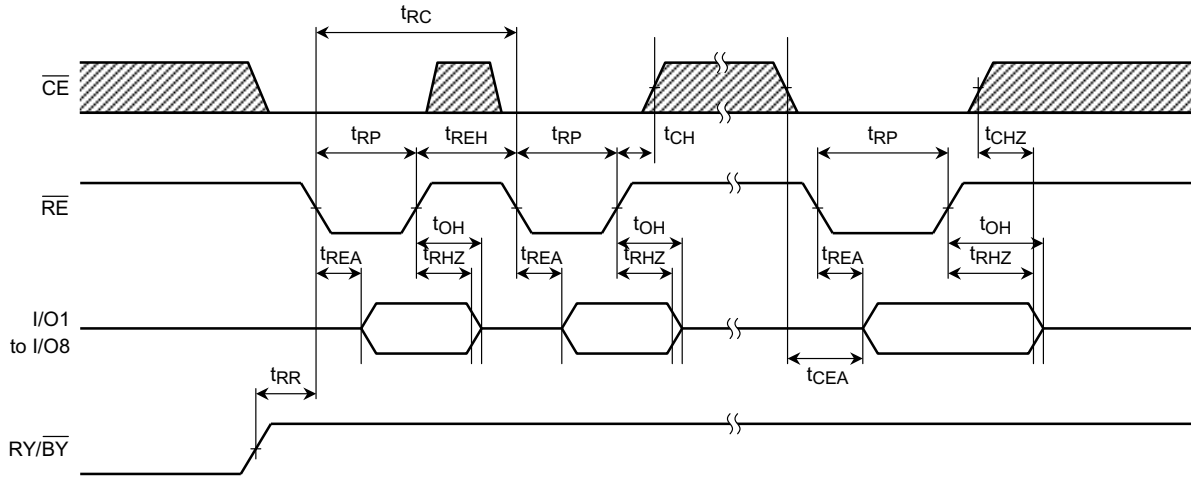
Latch Timing Diagram for Command/Address/Data

Command Input Cycle Timing Diagram

Address Input Cycle Timing Diagram

t_{CLS}

CLE

t_{CS} t_{WC} t_{WC} t_{CH} t_{CS}

$\overline{CE}$

t_{WP} t_{WH} t_{WP} t_{WH} t_{WP} t_{WH} t_{WP}

$\overline{WE}$

t_{ALS} t_{ALH}

ALE

t_{DS} t_{DH} t_{DS} t_{DH} t_{DS} t_{DH} t_{DS} t_{DH}

I/O1 to I/O8   A0 to A7   A9 to A16   A17 to A24   A25 to A26

: V_{IH} or V_{IL}

Data Input Cycle Timing Diagram

t_{CLH}

CLE

t_{CS} t_{CH} t_{CS} t_{CH}

$\overline{CE}$

t_{ALS} t_{WC}

ALE

t_{WP} t_{WH} t_{WP} t_{WP}

$\overline{WE}$

t_{DS} t_{DH} t_{DS} t_{DH} t_{DS} t_{DH}

I/O1 to I/O8 $D_{IN}0$ $D_{IN}1$ $D_{IN}527$
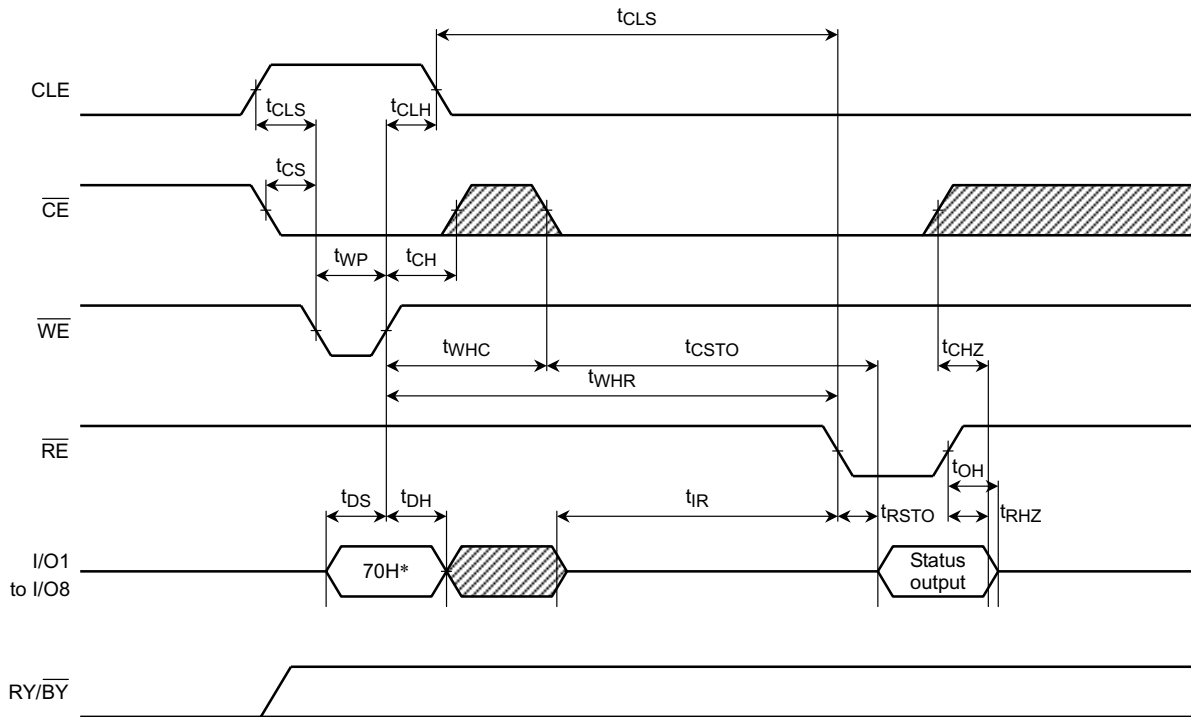
: V_{IH} or V_{IL}

Serial Read Cycle Timing Diagram

Status Read Cycle Timing Diagram

* 70H represents the hexadecimal number

$\boxed{\diagdown}$: V_{IH} or V_{IL}

www.DataSheet4U.com

Read Cycle (1) Timing Diagram
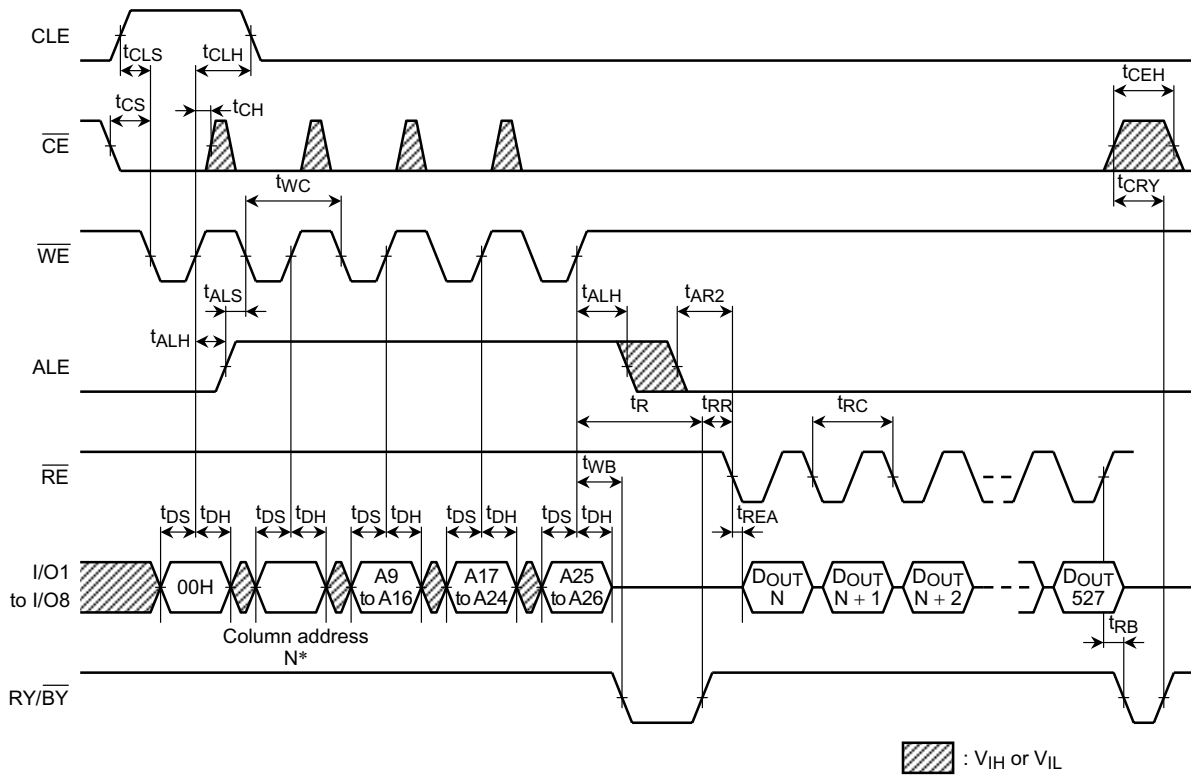
Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$
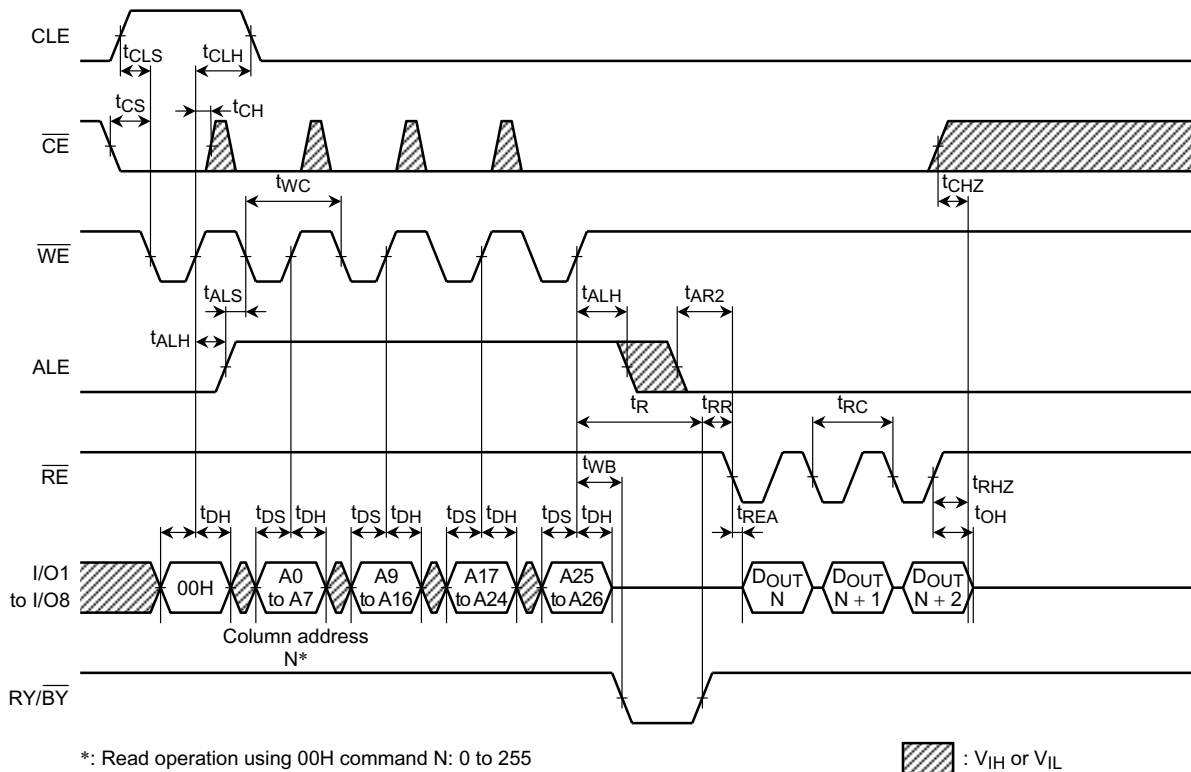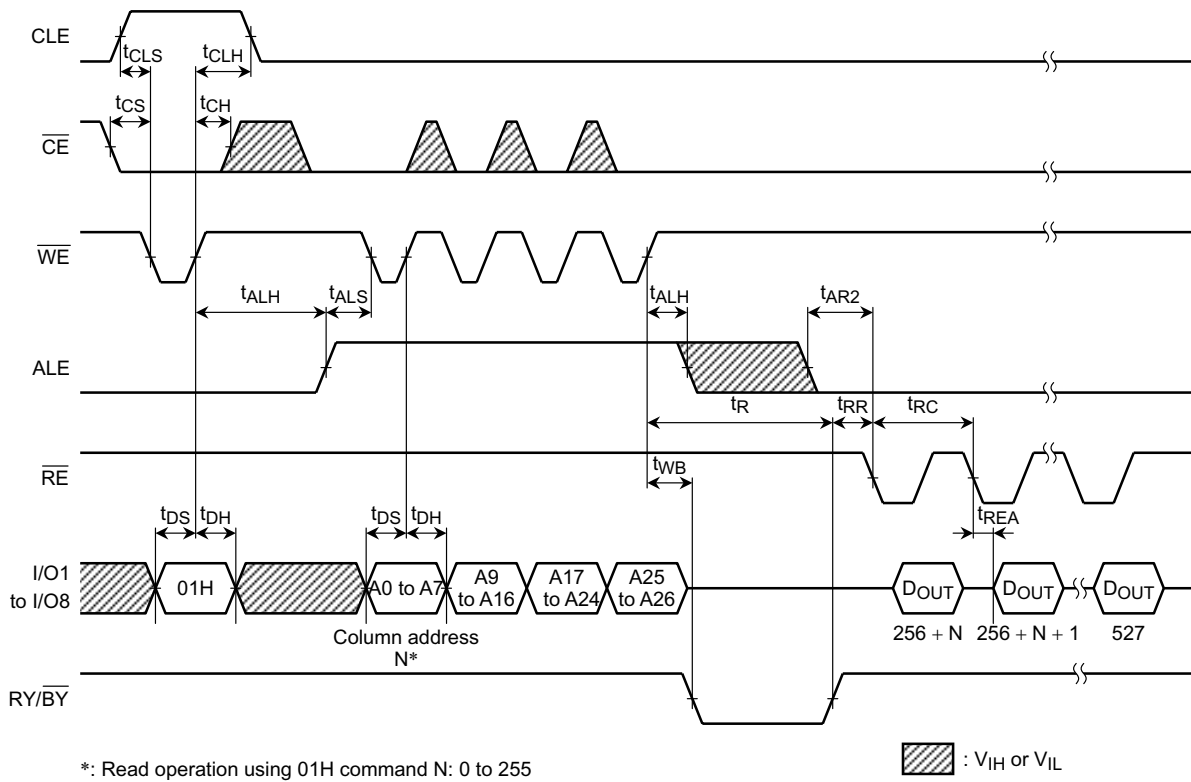

*: Read operation using 00H command N: 0 to 255

Read Cycle (2) Timing Diagram
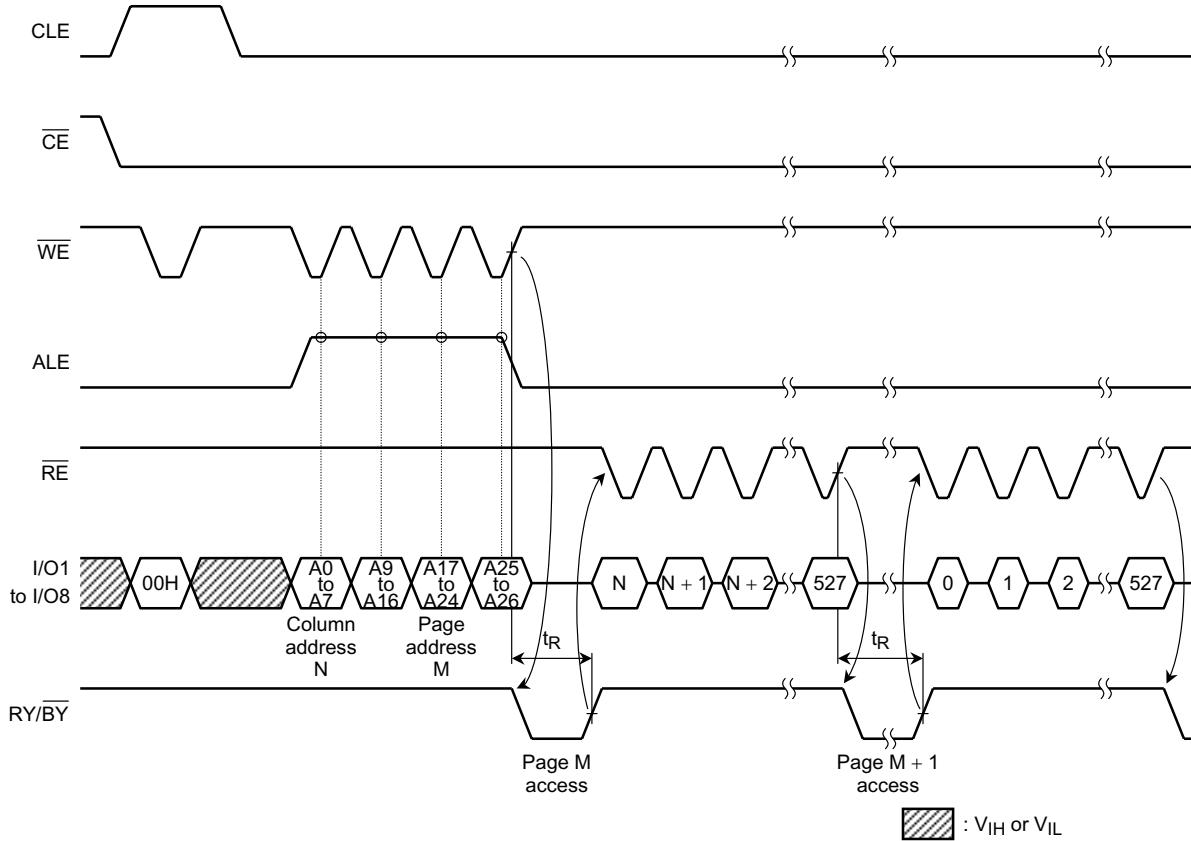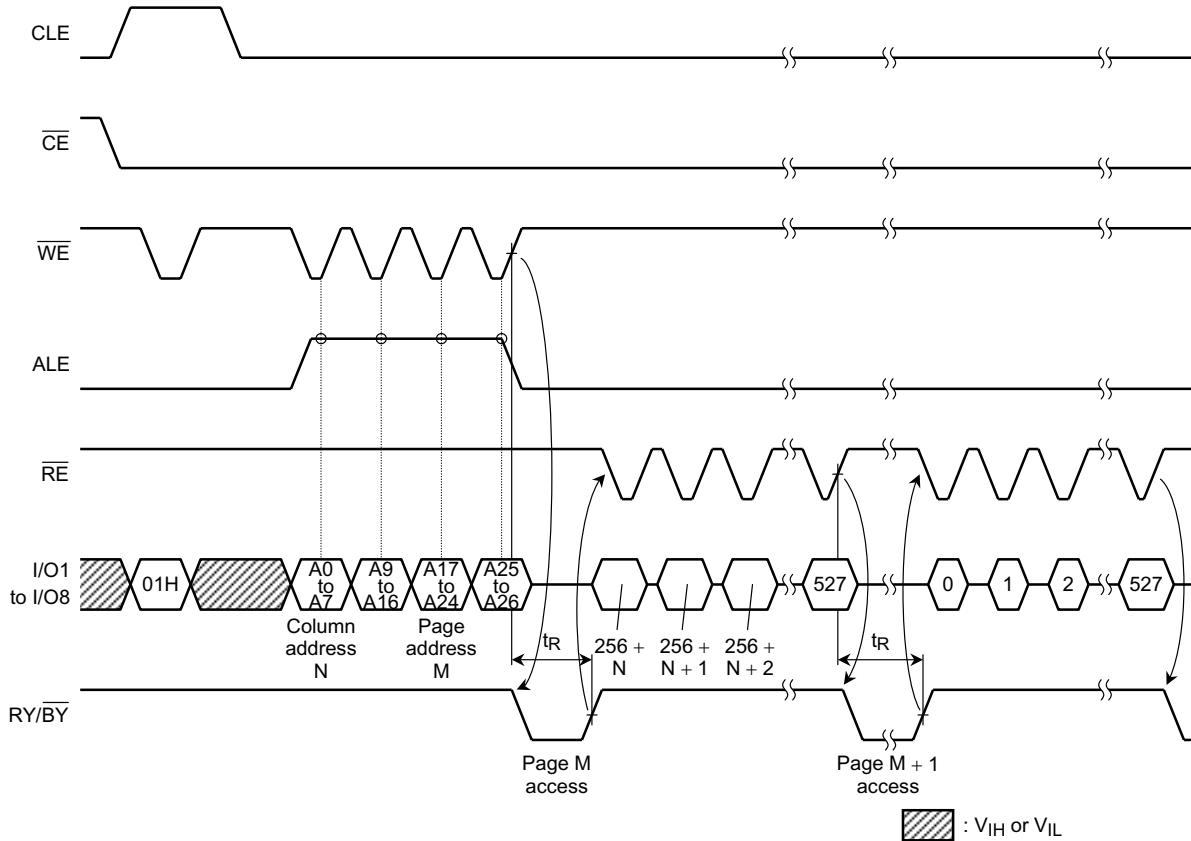

*: Read operation using 01H command N: 0 to 255

⬜ : V$_{IH}$ or V$_{IL}$

Read Cycle (3) Timing Diagram

*: Read operation using 50H command N: 0 to 15

⬜ : V$_{IH}$ or V$_{IL}$
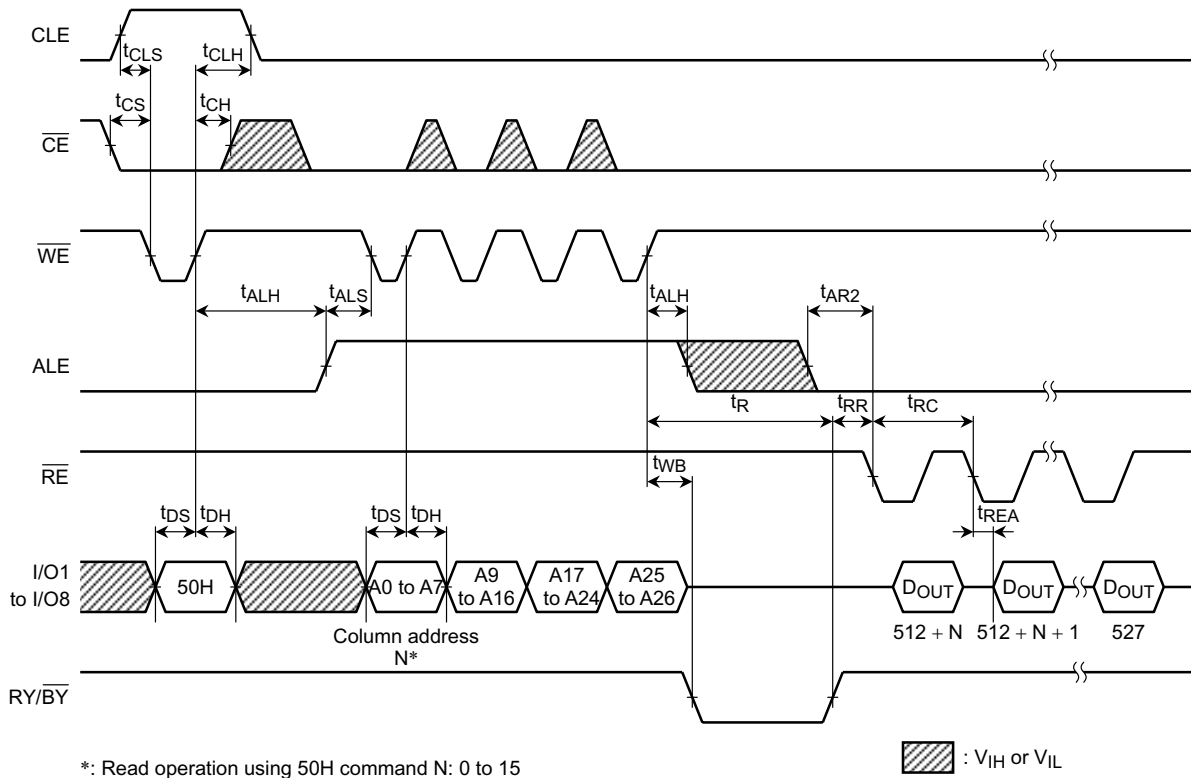
www.DataSheet4U.com

Sequential Read (1) Timing Diagram

CLE
$\overline{CE}$
$\overline{WE}$
ALE
$\overline{RE}$
I/O1 to I/O8

00H | A0 to A7 | A9 to A16 | A17 to A24 | A25 to A26 | N | N + 1 | N + 2 | 527 | 0 | 1 | 2 | 527

Column address N   Page address M

t_R t_R

RY/$\overline{BY}$

Page M access   Page M + 1 access

▨ : V_{IH} or V_{IL}

Sequential Read (2) Timing Diagram

CLE
$\overline{CE}$
$\overline{WE}$
ALE
$\overline{RE}$
I/O1 to I/O8

01H | A0 to A7 | A9 to A16 | A17 to A24 | A25 to A26 | | | | 527 | 0 | 1 | 2 | 527

Column address N   Page address M

t_R 256 + N   256 + N + 1   256 + N + 2 t_R

RY/$\overline{BY}$

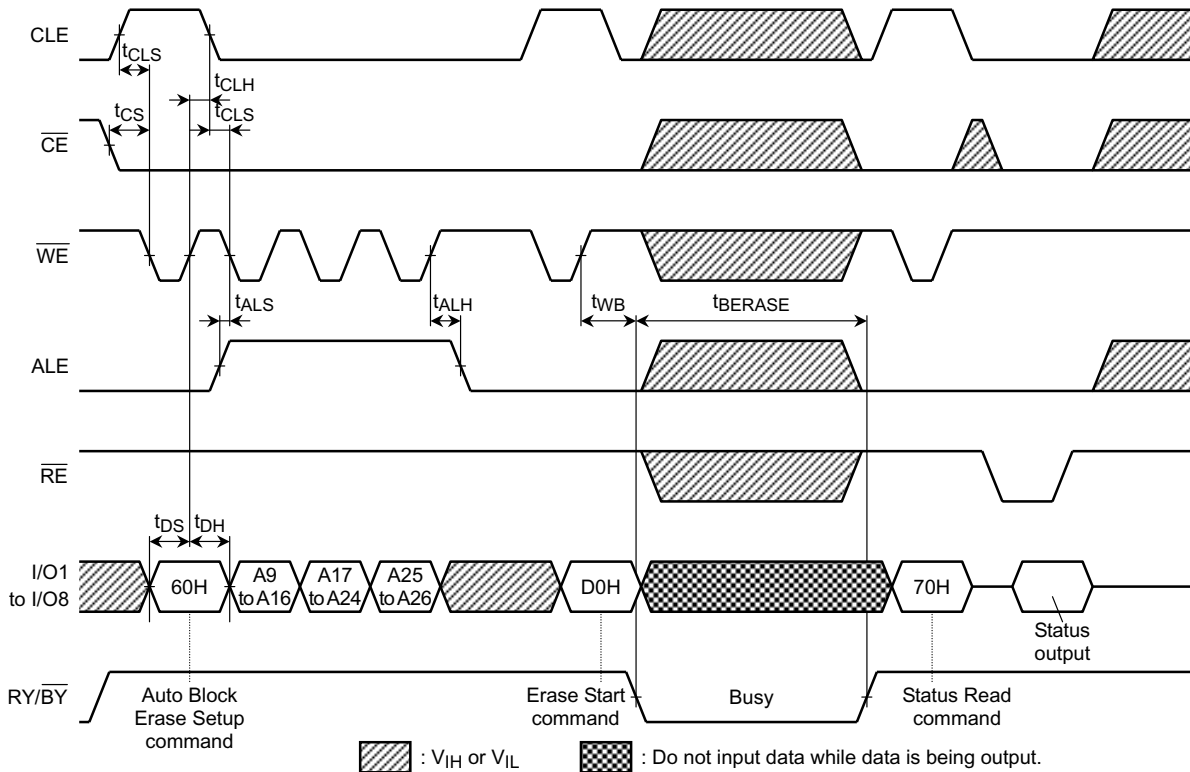Page M access   Page M + 1 access

▨ : V_{IH} or V_{IL}

www.DataSheet4U.com

Sequential Read (3) Timing Diagram
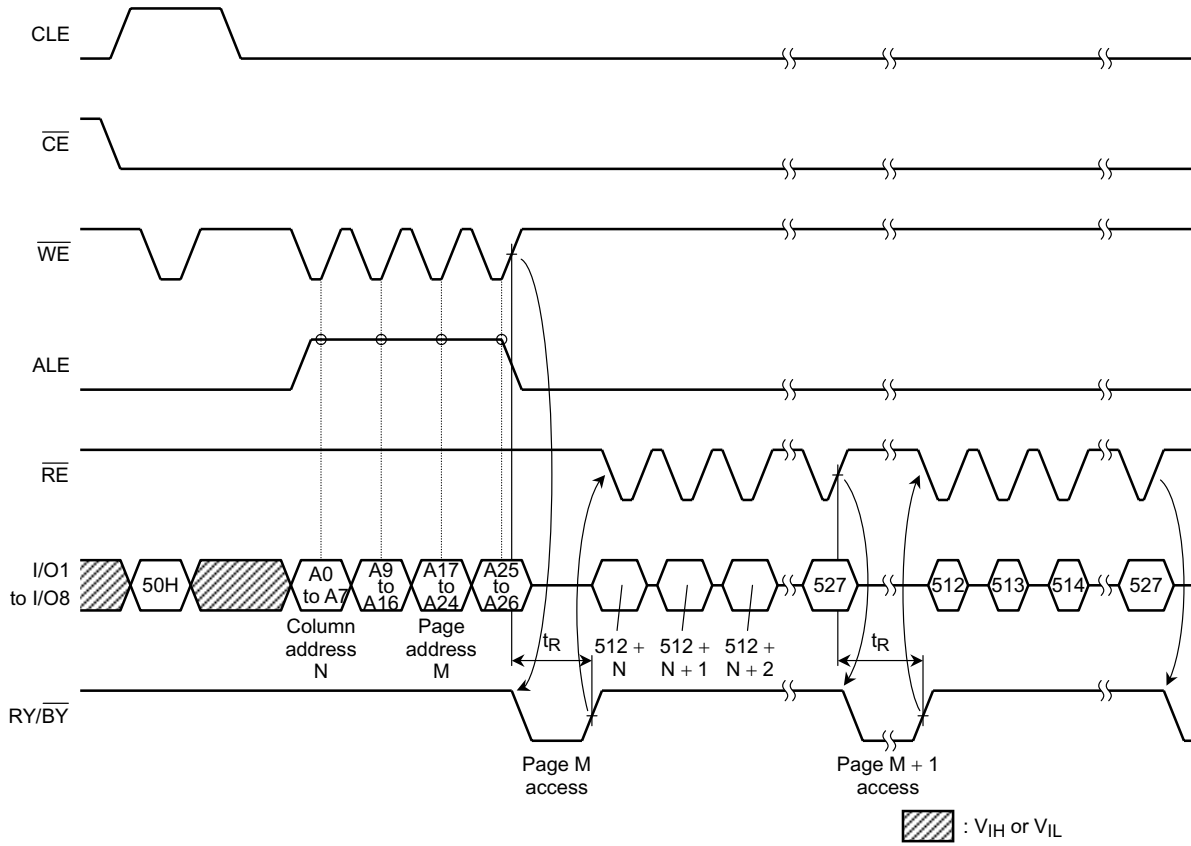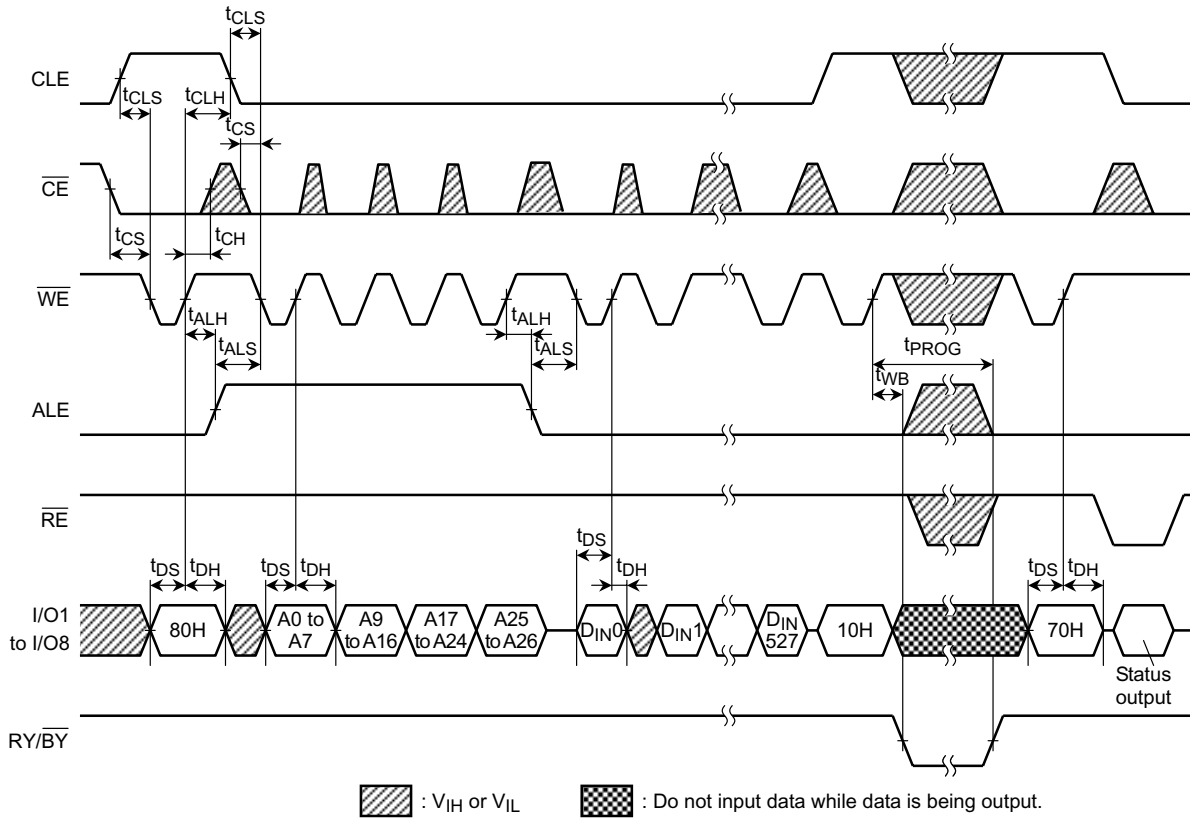
www.DataSheet4U.<u>Auto-Program Operation Timing Diagram</u>

: V_{IH} or V_{IL} : Do not input data while data is being output.

<u>Auto Block Erase Timing Diagram</u>

: V_{IH} or V_{IL} : Do not input data while data is being output.

Multi Block Programming Timing (to be continued)

: V_IH or V_IL

Auto program (dummy)

Max 3 times repeat — Last district input

1 | 2

31 times repeat
(Page 0 to 30 programming in multi block)

Max 4 blocks programming

(continuation 1) Multi Block Programming Timing

: V_{IH} or V_{IL}

: Do not input data while data is being output.

Max 3 times repeat

Last district input

Auto program (multi block program)

2

3

31 times repeat

Max 3 times repeat

(Page 0 to 30 programming in multi block)

Max 4 blocks programming

(continuation 2) Multi Block Programming Timing

: V_{IH} or V_{IL}

: Do not input data while data is being output.

Auto program (dummy)

3

4

Max 3 times repeat

Last district input

(Last pages programming in multi block)

Max 4 blocks programming

(continuation 3) Multi Block Programming Timing

: V_{IH} or V_{IL}

: Do not input data while data is being output.

Auto program (true)

Max 3 times repeat   4

Last district input

(Last pages programming in multi block)
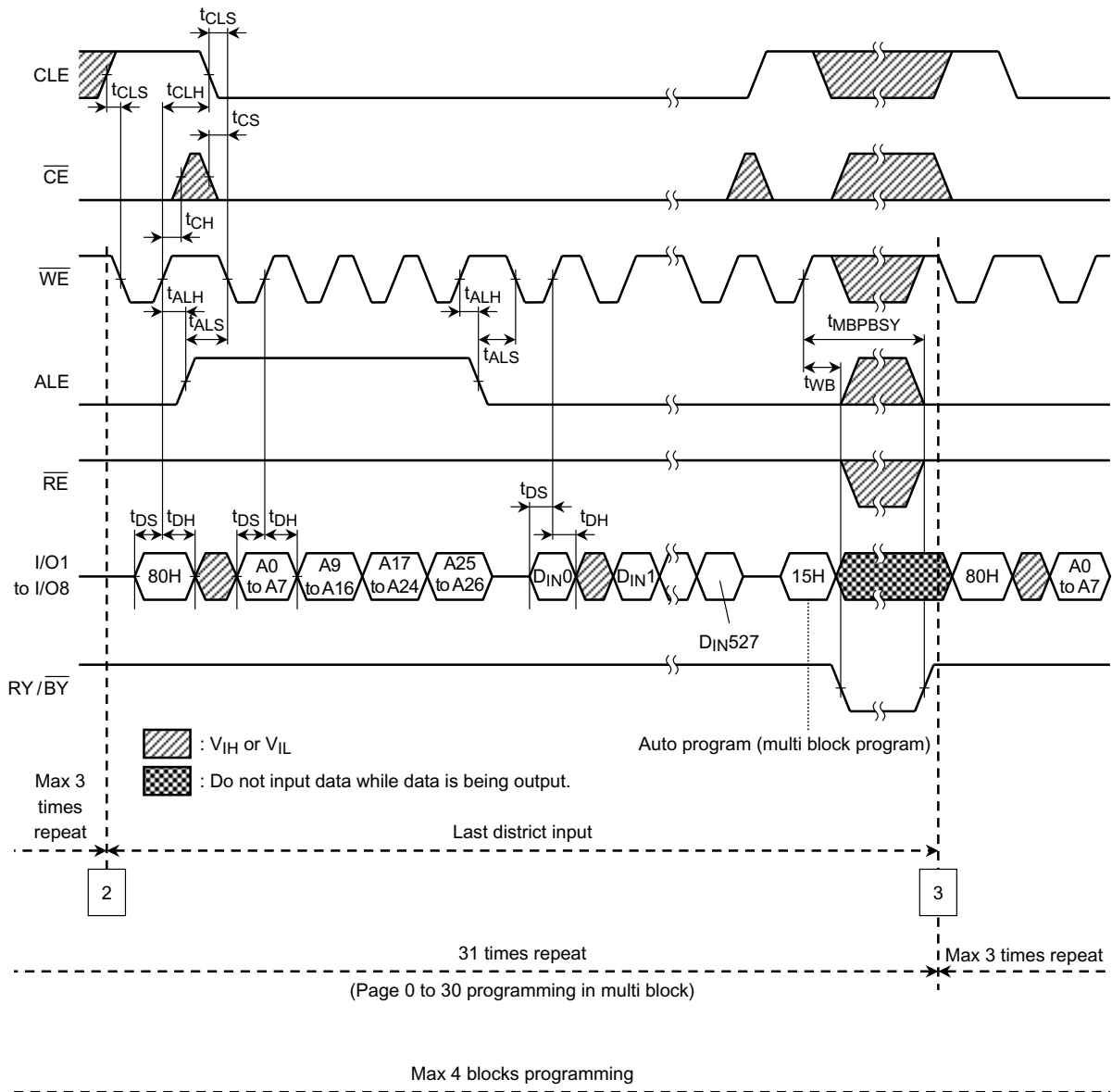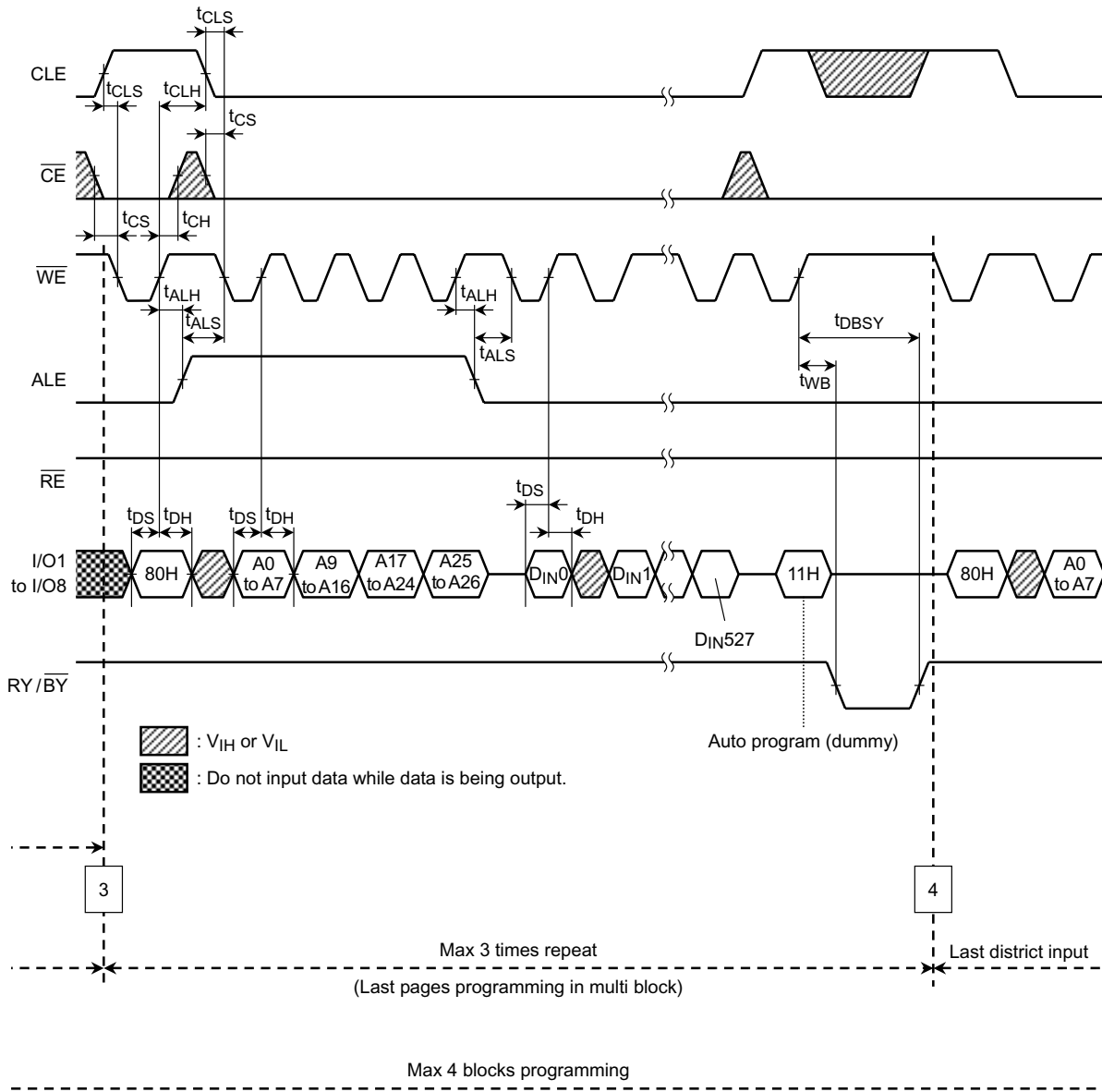
5

Max 4 blocks programming   Status read

Multi Block Erase Timing Diagram

: V_{IH} or V_{IL}

: Do not input data while data is being output.

ID Read (1) Operation Timing Diagram

Address input

Maker code   Device code

: V_{IH} or V_{IL}
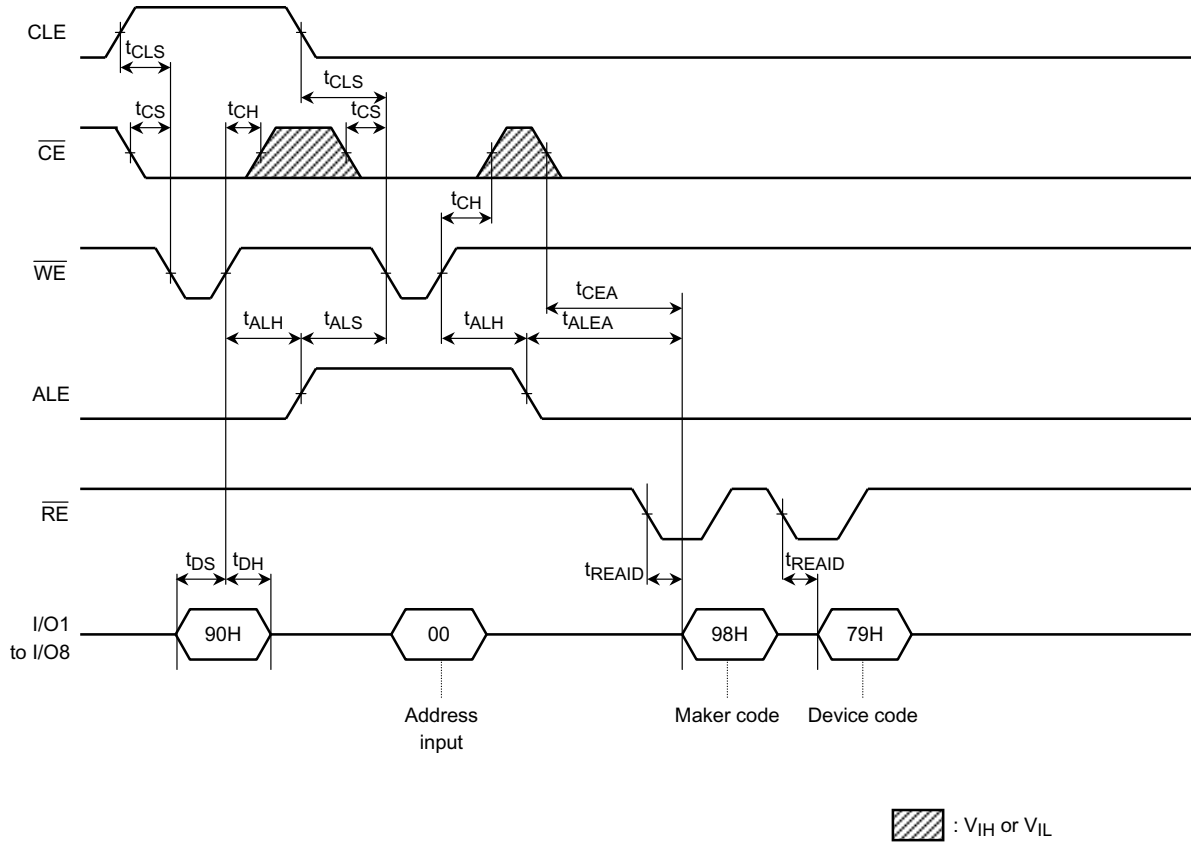
ID Read (2) Operation Timing Diagram

Address input

: V_{IH} or V_{IL}

PIN FUNCTIONS
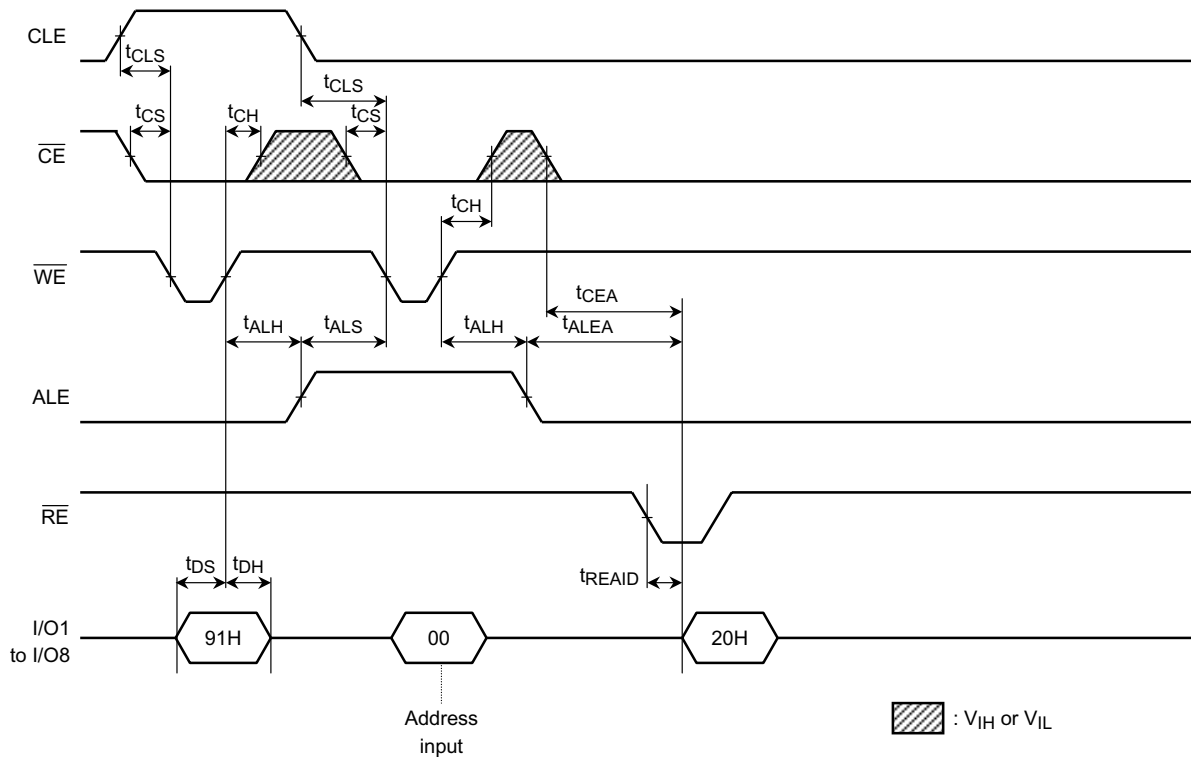
The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of $\overline{WE}$ if ALE is High.

Input data is latched if ALE is Low.

```
           NC  □ 1  ○         48 □ NC
           NC  □ 2            47 □ NC
           NC  □ 3            46 □ NC
           NC  □ 4            45 □ NC
           NC  □ 5            44 □ I/O8
          GND  □ 6            43 □ I/O7
        RY/BY  □ 7            42 □ I/O6
           RE  □ 8            41 □ I/O5
           CE  □ 9            40 □ NC
           NC  □ 10           39 □ NC
           NC  □ 11           38 □ NC
          VCC  □ 12           37 □ VCC
          VSS  □ 13           36 □ VSS
           NC  □ 14           35 □ NC
           NC  □ 15           34 □ NC
          CLE  □ 16           33 □ NC
          ALE  □ 17           32 □ I/O4
           WE  □ 18           31 □ I/O3
           WP  □ 19           30 □ I/O2
           NC  □ 20           29 □ I/O1
           NC  □ 21           28 □ NC
           NC  □ 22           27 □ NC
           NC  □ 23           26 □ NC
           NC  □ 24           25 □ NC
```
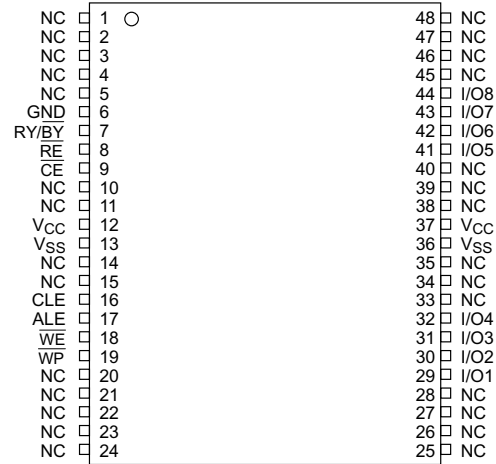
Figure 1. Pinout

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a Read operation. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High. The $\overline{CE}$ signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.

The internal column address counter is also incremented (Address = Address + l) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Schematic Cell Layout and Address Assignment

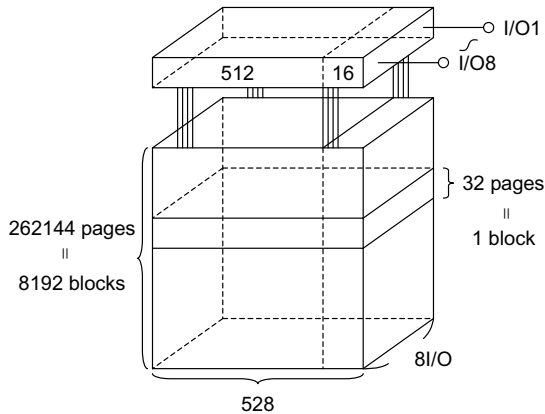The Program operation works on page units while the Erase operation works on block units.

Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

    1 page = 528 bytes

    1 block = 528 bytes × 32 pages = (16K + 512) bytes

Capacity = 528 bytes × 32 pages × 8192 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	A24	A23	A22	A21	A20	A19	A18	A17
Fourth cycle	*L	*L	*L	*L	*L	*L	A26	A25

A0 to A7   : Column address
A9 to A26 : Page address
A14 to A26 : Block address
A9 to A13 : NAND address in block

* : A8 is automatically set to Low or High by a 00H command or a 01H command.

* : I/O3 to I/O8 must be set to Low in the fourth cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the nineteen different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⌐_⌐	H	*
Data Input	L	L	L	⌐_⌐	H	H
Address Input	L	H	L	⌐_⌐	H	*
Serial Data Output	L	L	L	H	⌐_⌐	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0V/Vcc

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	○
Auto Program (True)	10	—	
Auto Program (Dummy)	11	—	
Auto Program (Multi Block Program)	15	—	
Auto Block Erase	60	D0	
Status Read (1)	70	—	○
Status Read (2)	71	—	○
ID Read (1)	90	—	
ID Read (2)	91	—	

HEX data bit assignment

(Example)

Serial Data Input: 80H

1	0	0	0	0	0	0	0
I/O8	7	6	5	4	3	2	I/O1
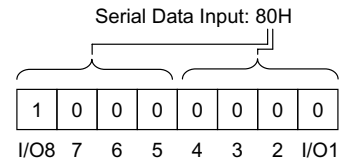
Once the device has been set to Read mode by a 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations.

Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output Select	L	L	L	H	L	Output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

www.DataSheet4U.com

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a "00H" command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.
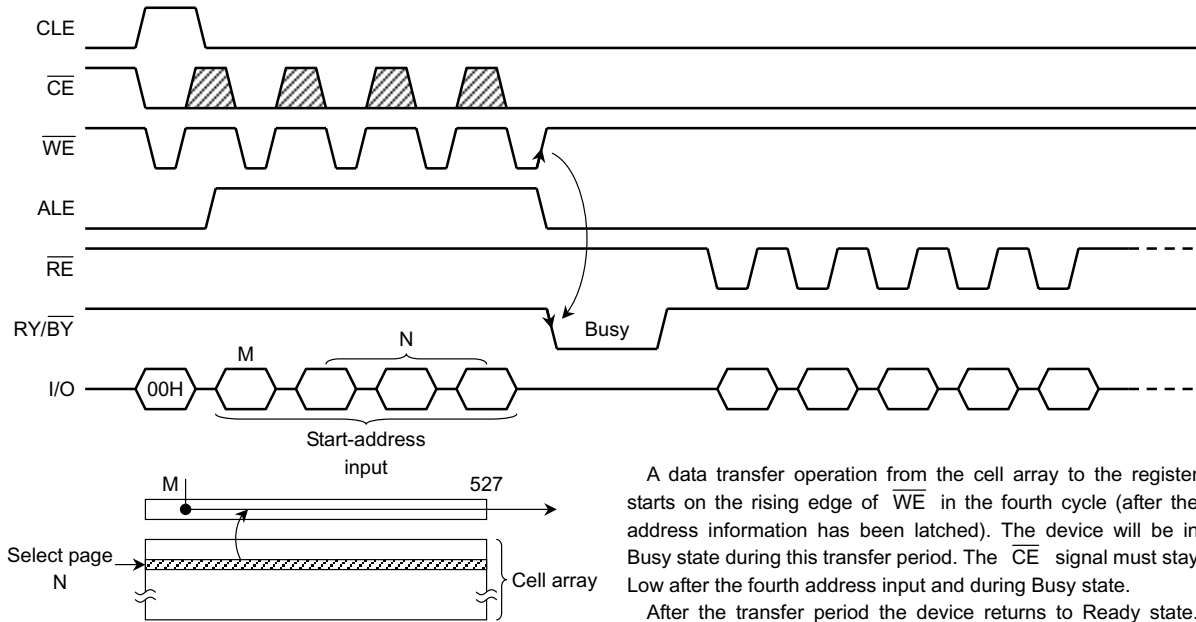

Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the fourth cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay Low after the fourth address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)
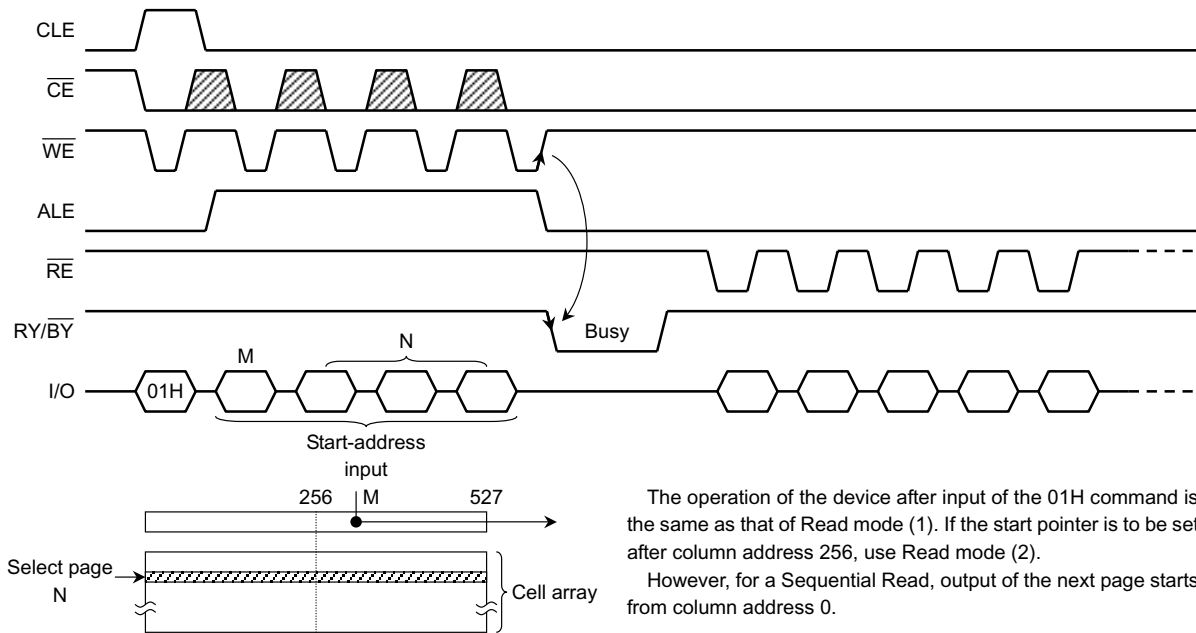
Figure 4. Read mode (2) operation

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

However, for a Sequential Read, output of the next page starts from column address 0.

www.DataSheet4U Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.
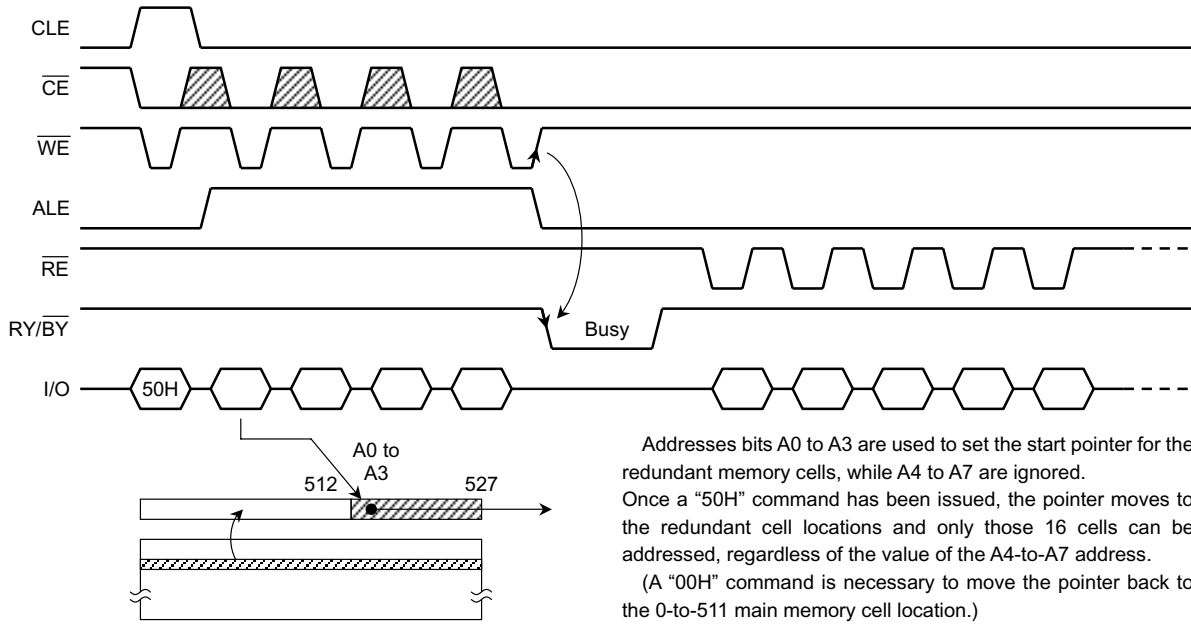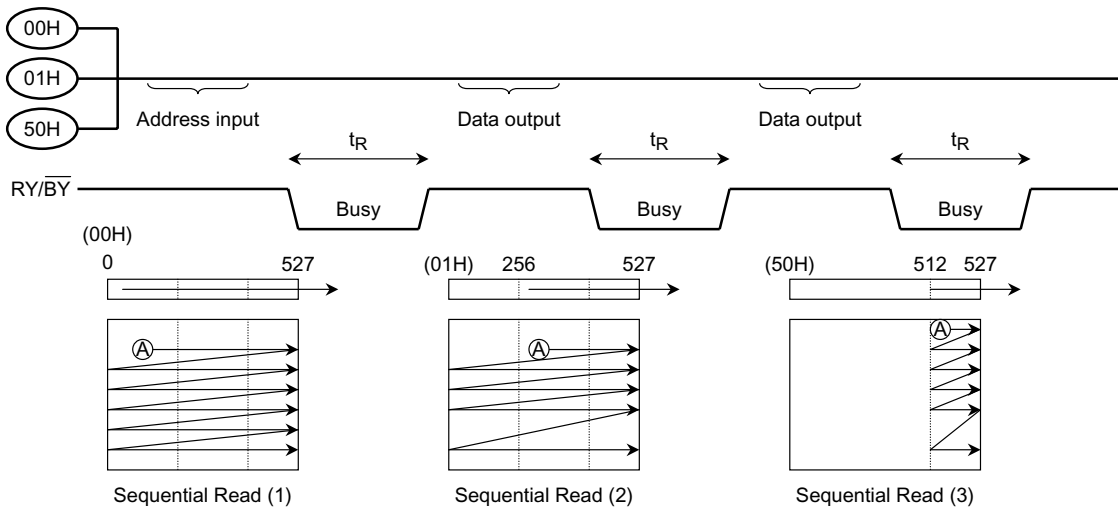
CLE

CE

WE

ALE

RE

RY/BY   Busy

I/O 〈50H〉

A0 to
A3
512   527

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored.
Once a "50H" command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address.
(A "00H" command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Figure 5. Read mode (3) operation

Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.

〈00H〉
〈01H〉   Address input t_R Data output t_R Data output t_R
〈50H〉

RY/BY   Busy   Busy   Busy

(00H)
0   527   (01H) 256   527   (50H)   512 527

Ⓐ   Ⓐ   Ⓐ

Sequential Read (1)   Sequential Read (2)   Sequential Read (3)

Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only.

When the page address reaches the next block address, read command (00H/01H/50H) and address inputs are needed.

Status Read

The device has three Status Read commands. There are Status Read (1) command "70H" and Status Read (2) command "71H".

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a Status Read command "70H" or "71H" input.

The resulting information of Status Read (1) command "70H" is outlined in Table 5 below and the resulting information of Status Read (2) command "71H" are outlined in the explanation for Multi Block Program and Multi Block Erase toward the end of this document.

Table 5. Status output table for Status Read (1) command "70H"

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.
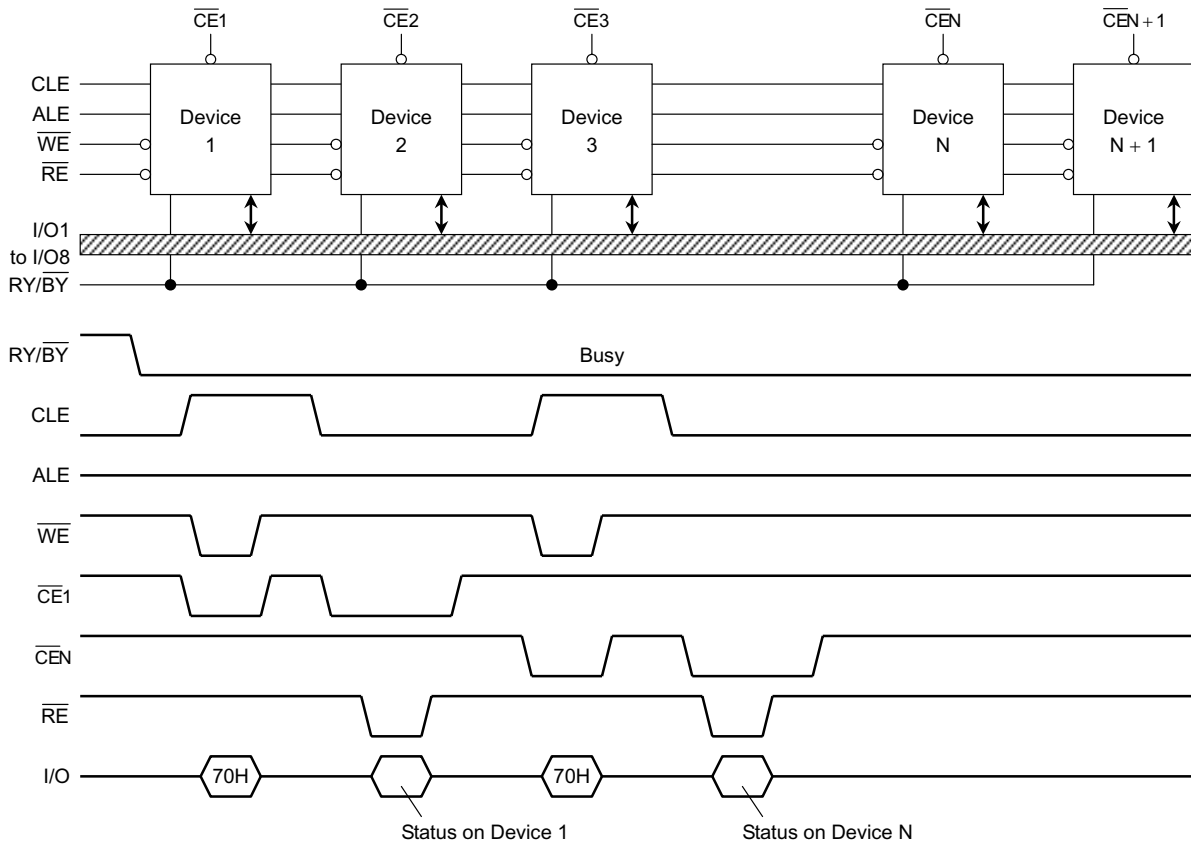
Figure 6. Status Read timing application example

System Design Note: If the $RY/\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)
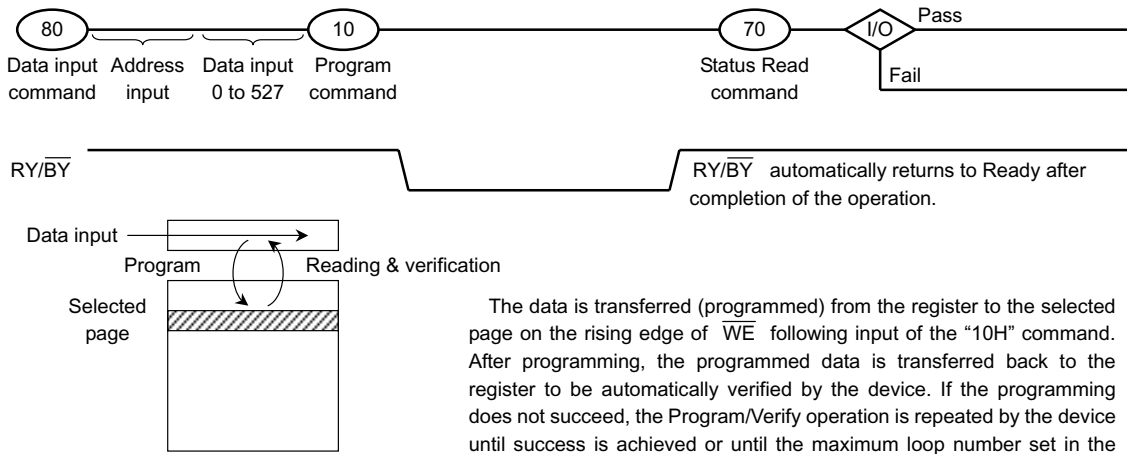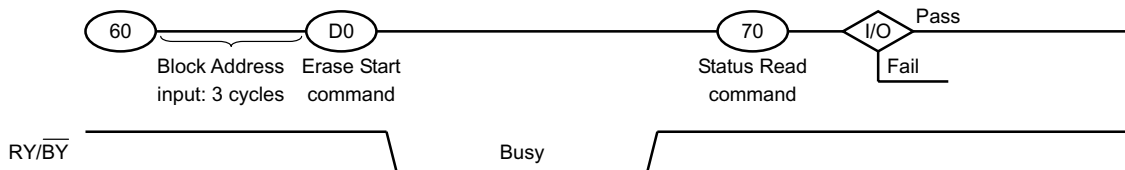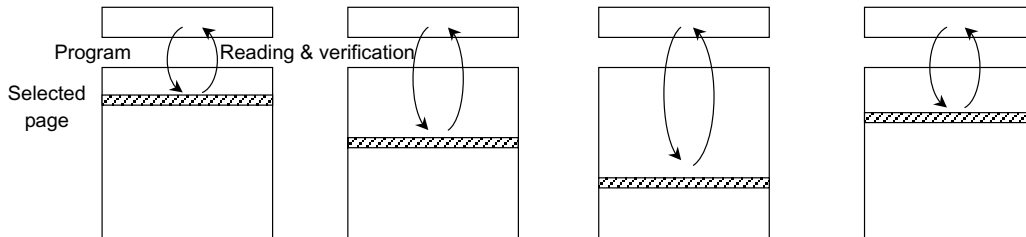

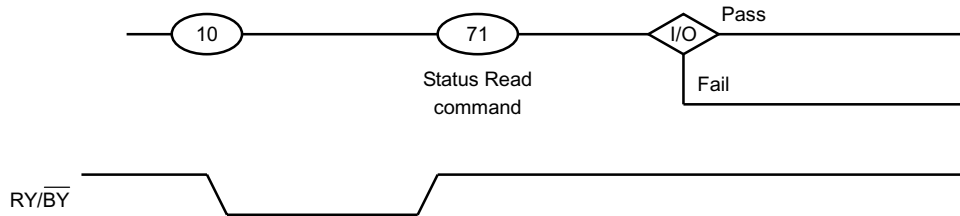The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the "10H" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0H" which follows the Erase Setup command "80H". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

Multi Block Program

The device carries out an Multi Block Program operation when it receives a "15H" or "10H" Program command after some sets of the address and data have been input.

In the interval of the Multi District adress and the (512 + 16 byte) data input, "11H" Dummy Program command is used when it still continues the data input into another District.

The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)
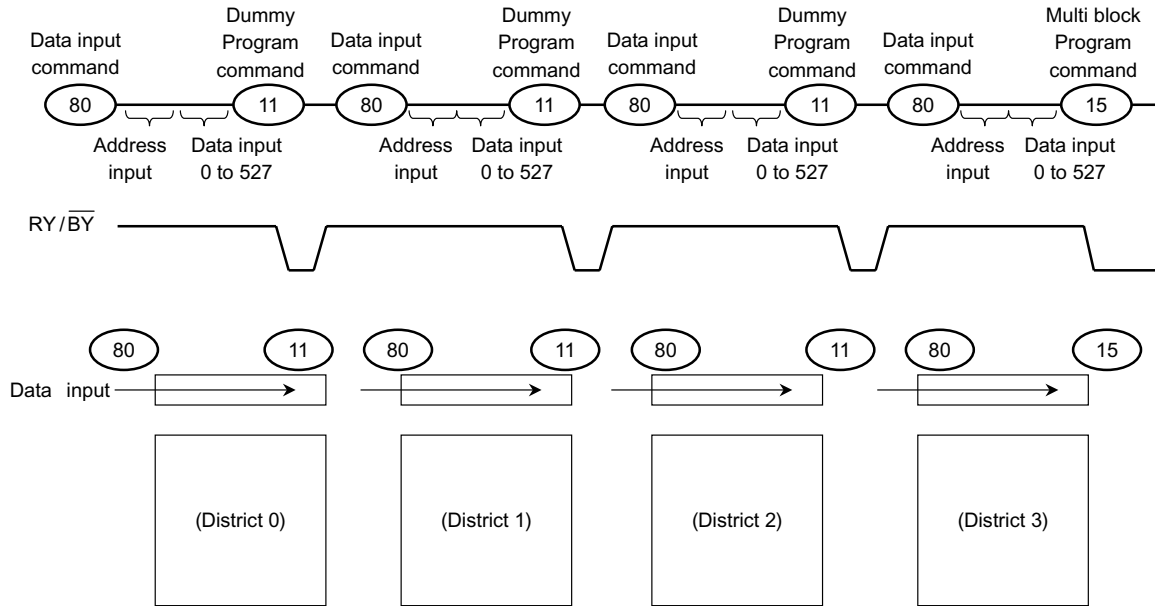
After "15H" Multi Block Program command, physical programing starts as follows.

The data is transferred (programmed) from the register to the selected page on the rising edge of -WE following input of the "15H" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 31 times with incrementing the page address in the blocks, and then input the last page data of the blocks, "10H" command executes final programming.

In this full sequence, the command sequence is following.
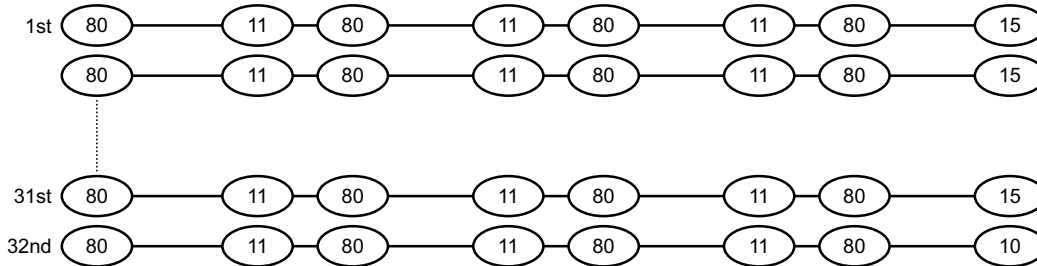
After the "10H" command, the total results of the above operation is shown through the Status Read command.

The Status discription of 71H command is following.

	STATUS	OUTPUT	
I/O1	Total Pass/Fail	Pass: 0	Fail: 1
I/O2	District 0 Pass/Fail	Pass: 0	Fail: 1
I/O3	District 1 Pass/Fail	Pass: 0	Fail: 1
I/O4	District 2 Pass/Fail	Pass: 0	Fail: 1
I/O5	District 3 Pass/Fail	Pass: 0	Fail: 1
I/O6	Not Used	Do not care	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes total Pass/Fail condition. If at least one fail occurred in 32 times × 4 (512 + 16 byte) page write operation, it shows "Fail" condition.

I/O2 describes Pass/Fail condition. If more than one fail occurred in 32 times (512 + 16 byte) page write operation in District 0 area, it shows "Fail" condition.

I/O3, I/O4 and I/O5 are as same manner as I/O2.

Internal addressing in relation with the Districts

To use Multi Block Program operation, the internal addressing should be conscious in relation with the District.

- The device consists of 4 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 4, Block 8, Block 12,   ⋯:.., Block 8188
District 1: Block 1, Block 5, Block 9, Block 13,   ⋯:.., Block 8189
District 2: Block 2, Block 6, Block 10, Block 14,   ⋯:.., Block 8190
District 3: Block 3, Block 7, Block 11, Block 15,   ⋯:.., Block 8191

Address input restriction for the Multi Block Program operation

In selecting the blocks for the Multi Block Program operation, following is the restriction and acceptance.

(Restriction)
Maximum one block should be selected from each District.
The data input operation should be started from the same number page of the each selected block and then, the page number in the blocks should be same number at the same time programming.

(Acceptance)
There is no order limitation of the District for the address input.
Any number of the District can be select for the programming.
So, for example, following operations are in acceptance.
Example 1 : (80) [District 2] (11)　(80) [District 0] (11)　(80) [District 1] (15)
Example 2 : (80) [District 0] (11)　(80) [District 1] (11)　(80) [District 2] (11)　(80) [District 3] (15)

It requires no mutual address relation between the selected blocks from each District.

Operating restriction during the Multi Block Program operation

(Restriction)
Starting from 1st page data input, until issuing "10H" command, any other command out of defined sequence can not be issued except Status Read command and Reset command.

(Acceptance)
The data input operation can be terminated with "10H" command instead of "15H" command in the middle of the page number in the block.
In this case the Status represents the reflected value accumulated from 1st page programming of this sequence and up to the last page programming terminated by "10H" command.
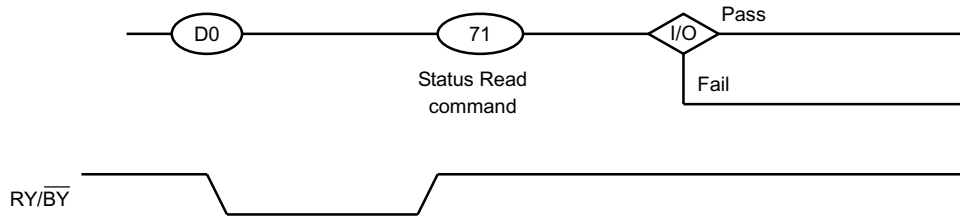
Status Read operation

Untill the Ready condition after the programming terminated by "10H" command, effective bit in the Status data is limited on Ready/Busy bit.
In other words, Pass/Fail condition can be checked only in the Ready condition after "10H" command.

Multi Block Erase

The device carries out a Multi Block Erase operation when it receives a "D0H" command after some sets of the address have been input.

After the "D0H" command, the total results of Erase operation is shown through the Status Read command "71H".

The Status discription of 71H command is following.

	STATUS	OUTPUT	
I/O1	Total Pass/Fail	Pass: 0	Fail: 1
I/O2	District 0 Pass/Fail	Pass: 0	Fail: 1
I/O3	District 1 Pass/Fail	Pass: 0	Fail: 1
I/O4	District 2 Pass/Fail	Pass: 0	Fail: 1
I/O5	District 3 Pass/Fail	Pass: 0	Fail: 1
I/O6	Not Used	Do not care	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes total Pass/Fail condition. If at least one fail occurred in Max 4 Blocks erase operation, it shows "Fail" condition.

I/O2 describes Pass/Fail condition. If fail occurred in District 0 area, it shows "Fail" condition.

I/O3, I/O4 and I/O5 are as same manner as I/O2.

Internal addressing in relation with the Districts

To use Multi Block Erase operation, the internal addressing should be conscious in relation with the Districts.

- The device consists of 4 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 4, Block 8, Block 12,   ⋯.., Block 8188
District 1: Block 1, Block 5, Block 9, Block 13,   ⋯.., Block 8189
District 2: Block 2, Block 6, Block 10, Block 14, ⋯.., Block 8190
District 3: Block 3, Block 7, Block 11, Block 15, ⋯.., Block 8191

Address input restriction for the Multi Block Erase operation

In selecting the blocks for the Multi Block Erase operation, following is the restriction and acceptance.

(Restriction)
Maximum one block should be selected from each District.

(Acceptance)
There is no order limitation of the District for the address input.
Any number of the Districts can be select for the erase operation.
So, for example, following operation are in acceptance.
Example 1 : (60) [District 2]   (60) [District 0]   (60) [District 1]   (D0)
Example 2 : (60) [District 0]   (60) [District 1]   (60) [District 2]   (60) [District 3]   (D0)

It requires no mutual address relation between the selected blocks from each District.

Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFH" Reset command input during the various device operations is as follows:

<u>When a Reset (FFH) command is input during programming</u>

Figure 8.

80 — 10 — FF — 00

Internal V_{PP}

RY/$\overline{BY}$

t_{RST} (max 10 μs)
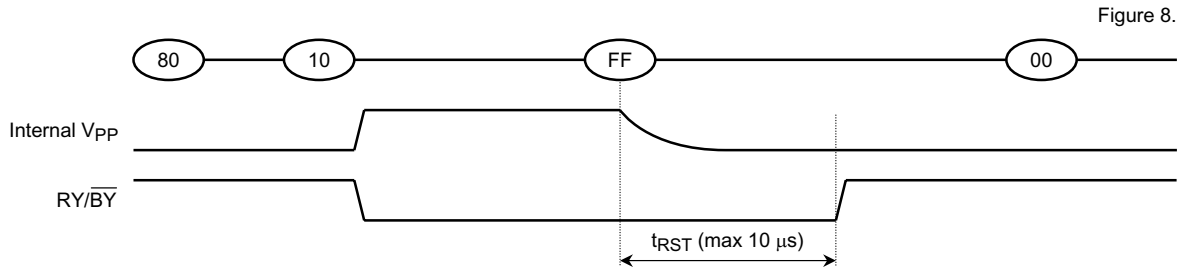
<u>When a Reset (FFH) command is input during erasing</u>

Figure 9.

D0 — FF — 00

Internal erase voltage

RY/$\overline{BY}$

t_{RST} (max 500 μs)
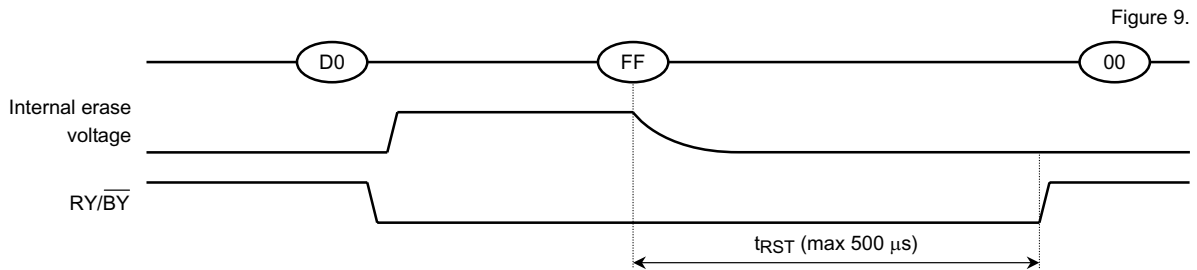
<u>When a Reset (FFH) command is input during Read operation</u>

Figure 10.

00 — FF — 00

RY/$\overline{BY}$

t_{RST} (max 6 μs)
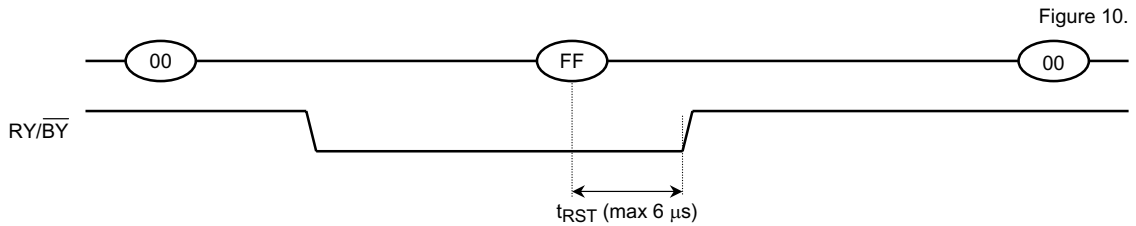
<u>When a Status Read command (70H) is input after a Reset</u>

Figure 11.

FF — 70

RY/$\overline{BY}$

I/O status: Pass/Fail → Pass
Ready/Busy → Ready

FF — 70

RY/$\overline{BY}$

I/O status: Ready/Busy → Busy
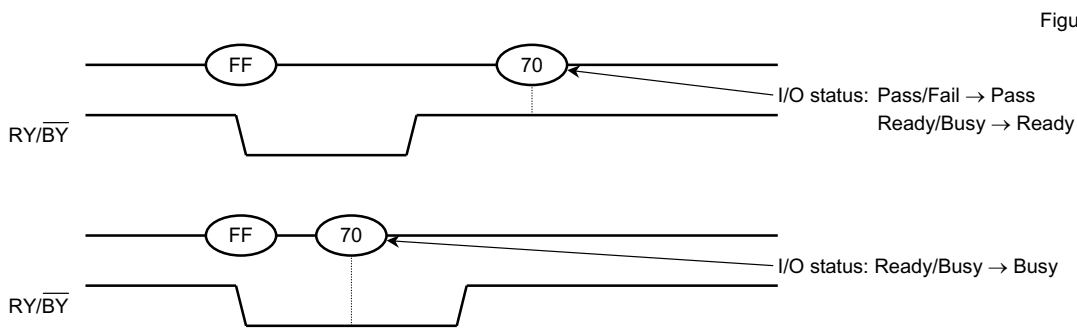
<u>When two or more Reset commands are input in succession</u>

Figure 12.

(1)   (2)   (3)
FF   FF   FF

RY/$\overline{BY}$

The second (FF) command is invalid, but the third (FF) command is valid.
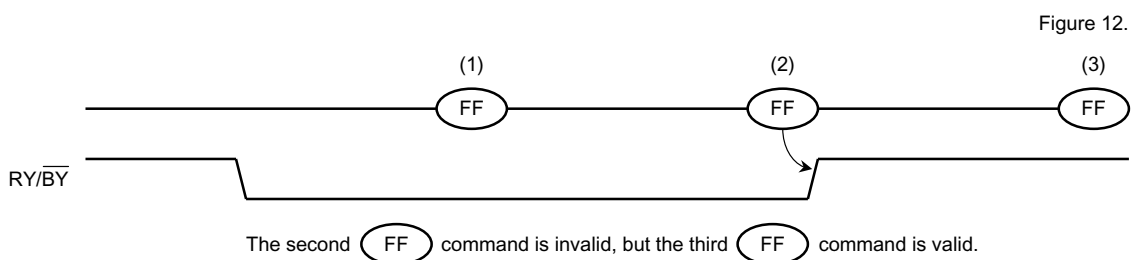
ID Read (1)

The device contains ID codes which identify the device type and the manufacturer.

The device has 2 types of ID read command, i.e. ID Read (1) command 90H and ID Read (2) command 91H.

ID Read (1) command 90H provides maker code and device code. The ID codes can be read out under the following timing conditions:
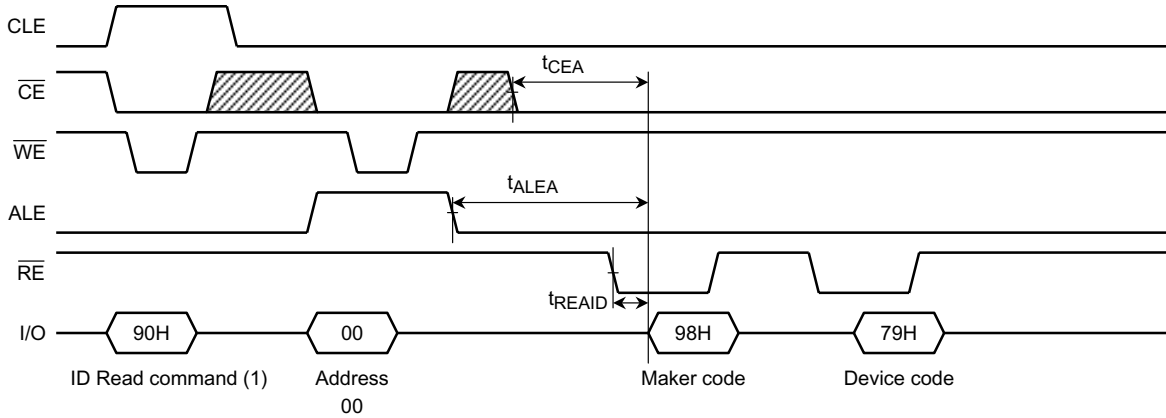
For the specifications of the access times t_{REAID}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.
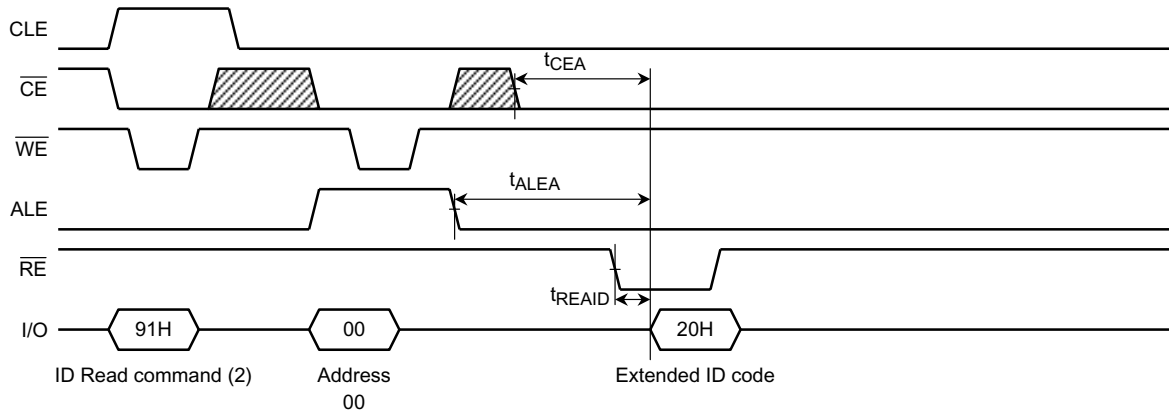
Figure 13. ID Read timing

Table 6. ID Codes read out by ID read command (1) 90H

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	1	1	0	0	1	79H

ID Read (2)

ID Read (2) command 91H provides ×4-block mode availability. If ID code read out by 91H is B0H, it indicates the device has ×4-block mode.

For the specifications of the access times t_{REAID}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.

Figure 14. ID Read timing

Table 7. ID Codes read out by command 91H

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Extended ID code	0	0	1	0	0	0	0	0	20H

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The $\overline{WP}$ signal may be negated any time after the V_{CC} reaches 2.5 V and $\overline{CE}$ signal is kept high in power up sequence.
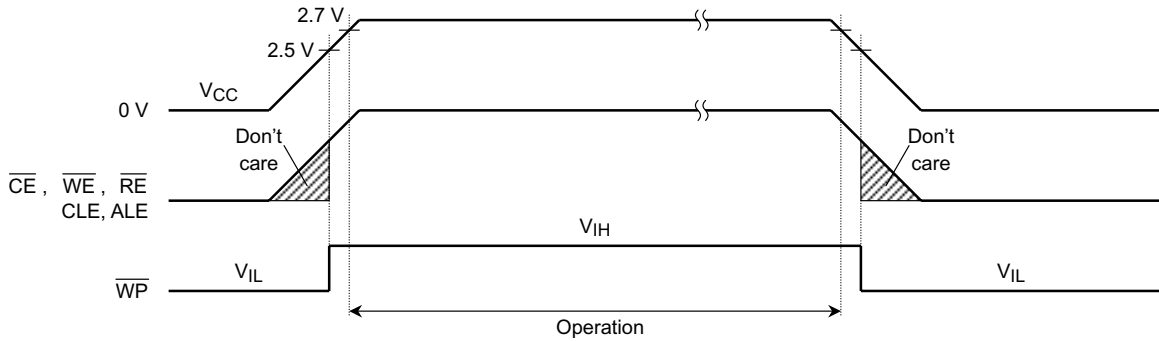
Figure 15. Power-on/off Sequence

In order to operate this device stably, after V_{CC} becomes 2.5 V, it recommends starting access after about 200 μs.

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

Power on — FF
Reset
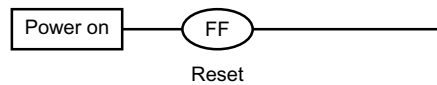
Figure 16.

(3) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of command while Busy state

During Busy state, do not input any command except 70H, 71H and FFH.

(5) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Program Execution command "10H", "11H" or "15H" or the Reset command "FFH".

If a command other than "10H", "11H", "15H" or "FFH" is input, the Program operation is not performed.

80 — XX — 10   } For this operation the "FFH" command is needed.
Command other than   Programming cannot be executed.
"10H", "11H", "15H" or "FFH"
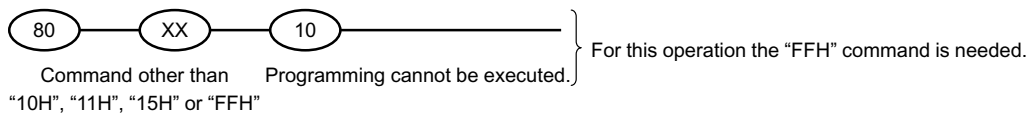
(6)   Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.
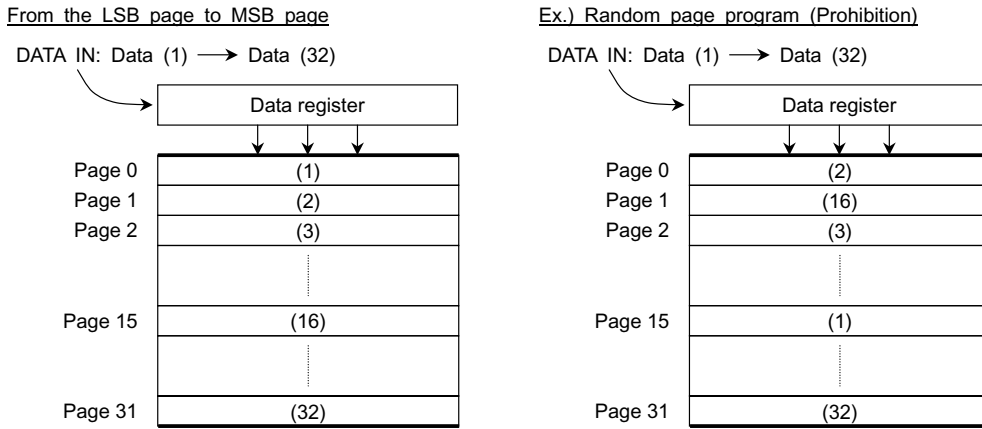
From the LSB page to MSB page   Ex.) Random page program (Prohibition)

DATA IN: Data (1) ⟶ Data (32)   DATA IN: Data (1) ⟶ Data (32)

Data register
(1)	(2)		(3)	

Page 0	(1)
Page 1	(2)
Page 2	(3)
Page 15	(16)
Page 31	(32)

Data register

Page 0	(2)
Page 1	(16)
Page 2	(3)
Page 15	(1)
Page 31	(32)

Figure 17. page programming within a block

(7)   Status Read during a Read operation
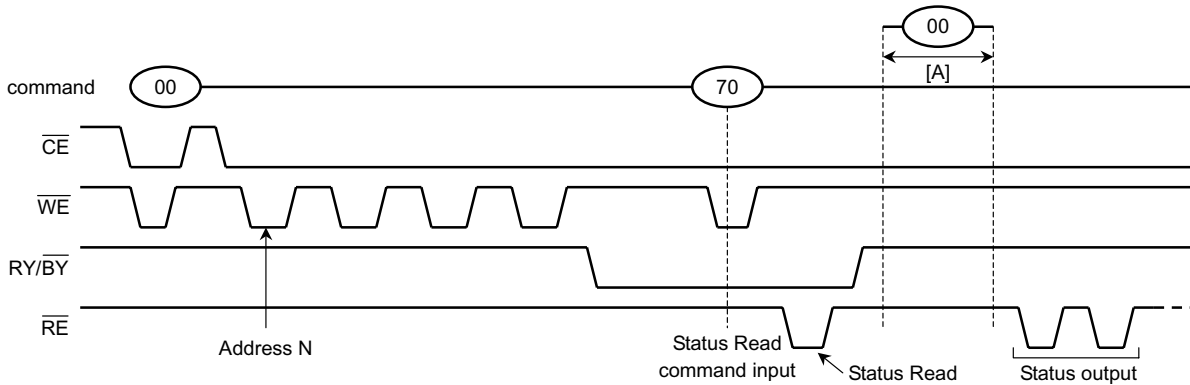
Figure 18.

The device status can be read out by inputting the Status Read command "70H" in Read mode.

Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Pointer control for "00H", "01H" and "50H"

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 8. Pointer Destination

Read Mode	Command	Pointer
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527
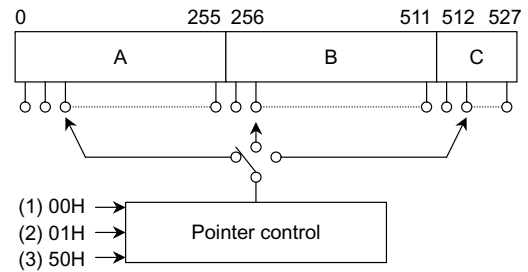
Figure 19. Pointer control

The pointer is set to region A by the "00H" command, to region B by the "01H" command, and to region C by the "50H" command.

(Example)

The "00H" command must be input to set the pointer back to region A when the pointer is pointing to region C.
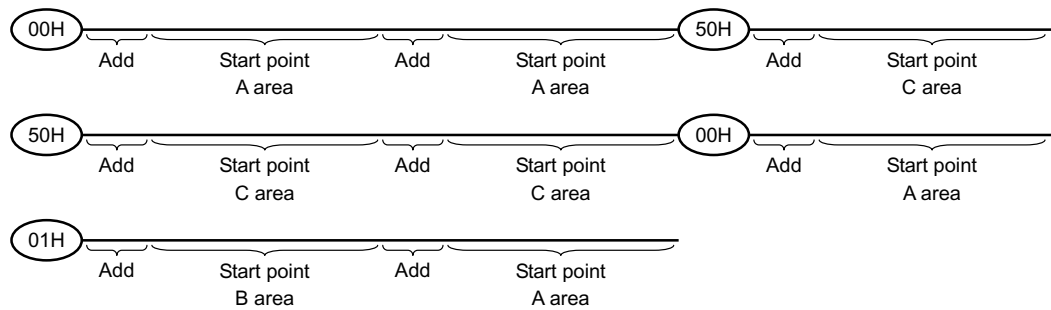
To program region C only, set the start point to region C using the 50H command.
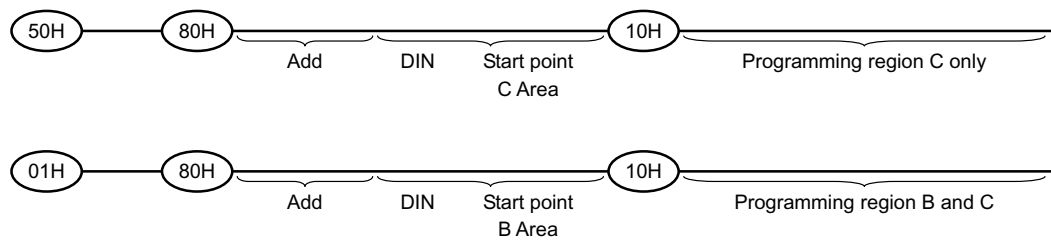
Figure 20. Example of How to Set the Pointer

(9)   RY/$\overline{BY}$: termination for the Ready/Busy pin ($RY/\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.
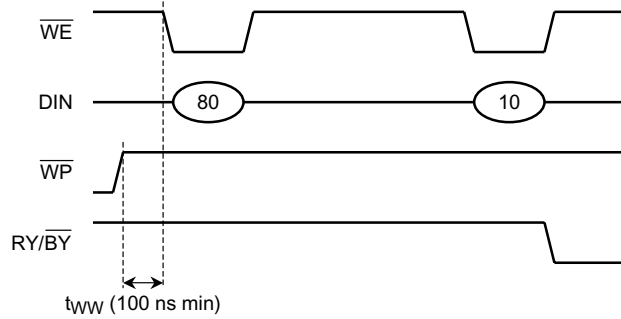

Figure 21.
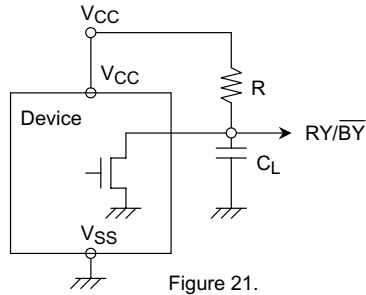
This data may vary from device to device.
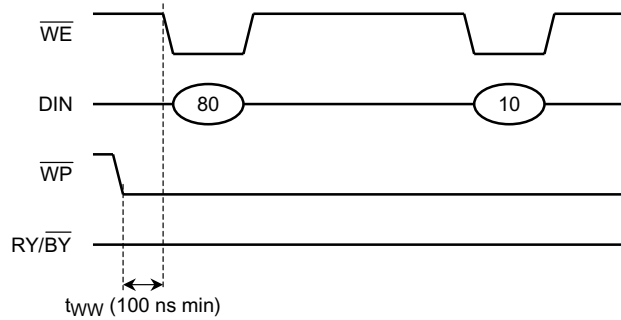We recommend that you use this data as a reference when selecting a resistor value.
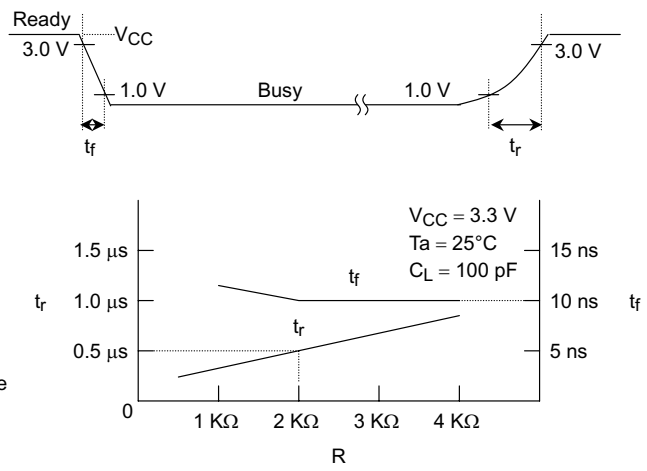
(10)   Note regarding the $\overline{\text{WP}}$ signal

The Erase and Program operations are automatically reset when $\overline{\text{WP}}$ goes Low. The operations are enabled and disabled as follows:
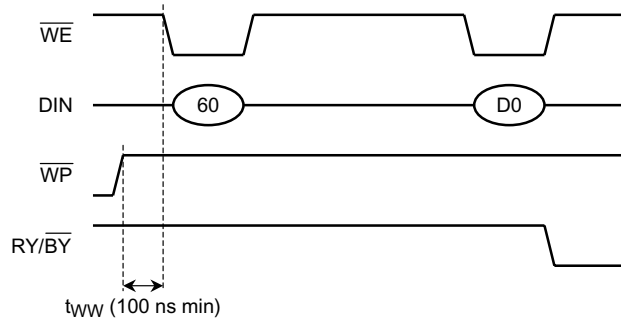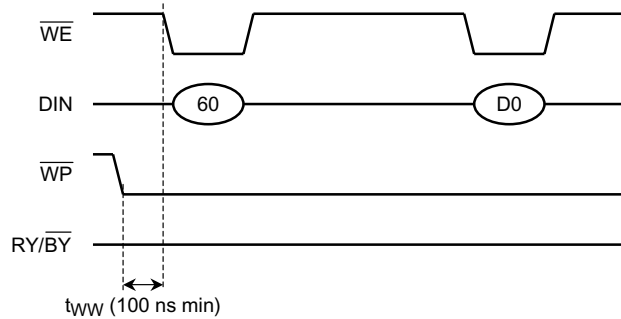
Enable Programming

t_{WW} (100 ns min)

Disable Programming

t_{WW} (100 ns min)

Enable Erasing

t_{WW} (100 ns min)

Disable Erasing

t_{WW} (100 ns min)
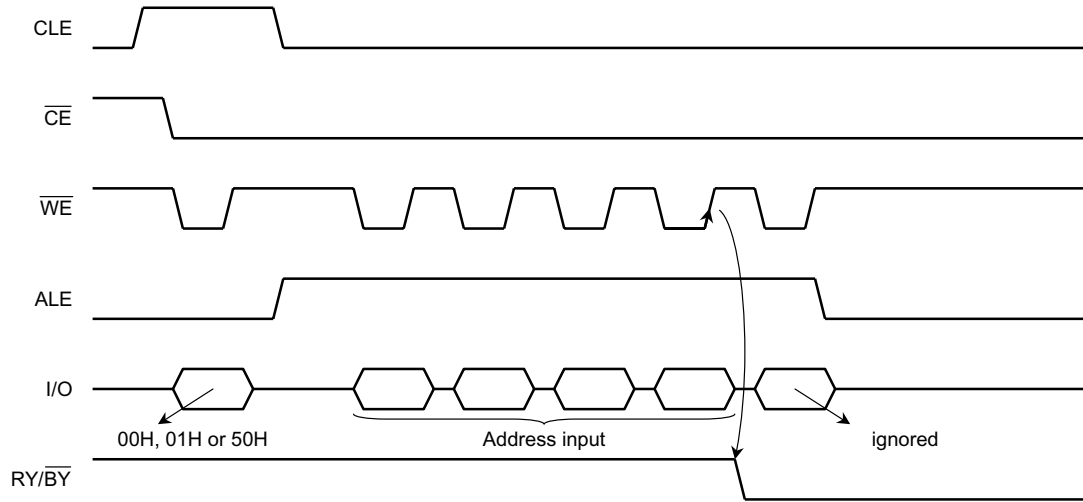
(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation

WE Internal read operation starts when WE goes High in the fourth cycle.
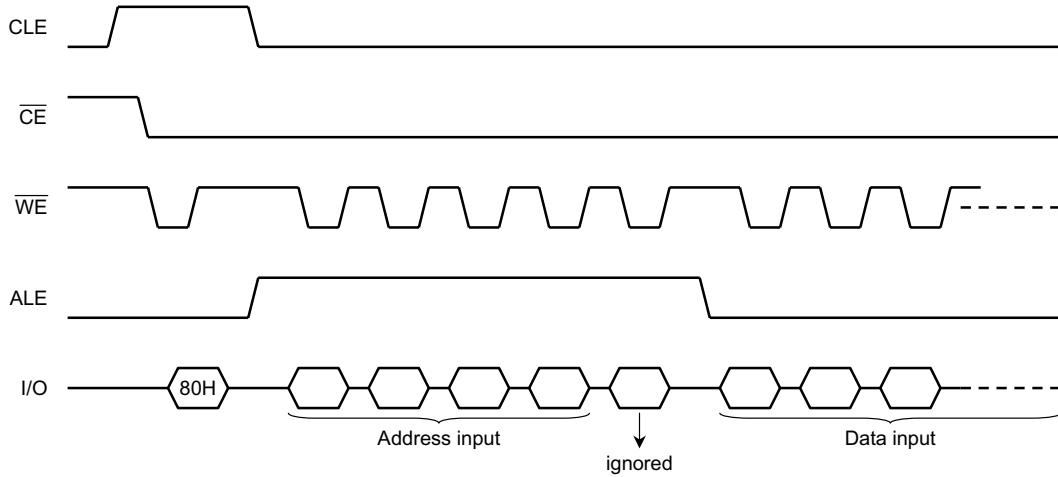
Figure 22.

Program operation

Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

1st programming	Data Pattern 1	All 1s	

2nd programming	All 1s	Data Pattern 2	All 1s

3rd programming	All 1s		Data Pattern 3

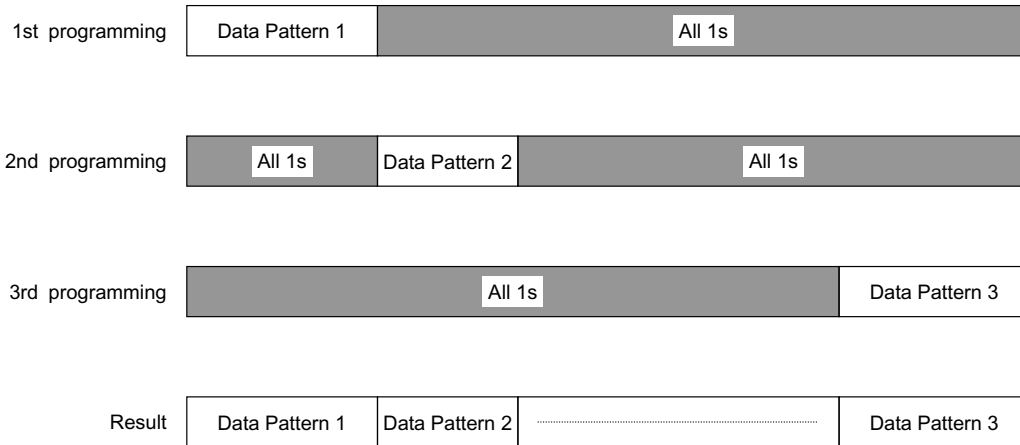| Result	Data Pattern 1	Data Pattern 2	....	Data Pattern 3

Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1"
(i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all "1").

(13) Note regarding the $\overline{RE}$ signal

$\overline{RE}$ The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a "00H", "01H" or "50H" command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing, If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 25.)
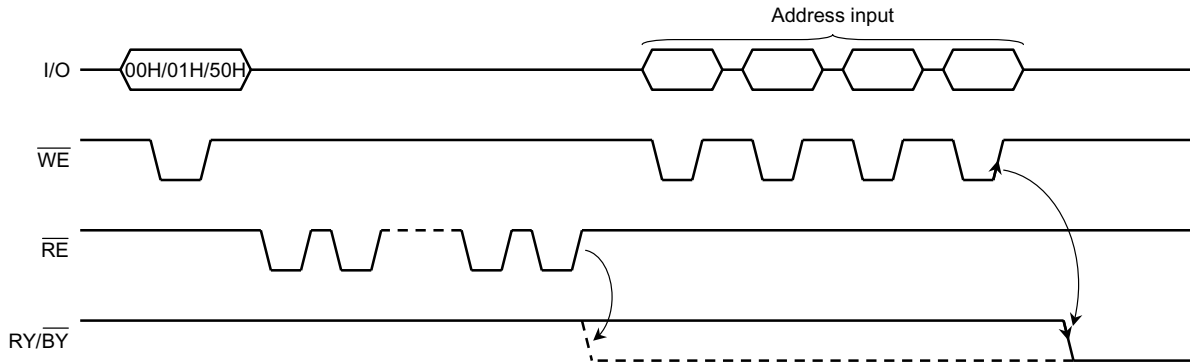
Figure 25.

Hence the $\overline{RE}$ clock input must start after the address input.

(14)   Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.
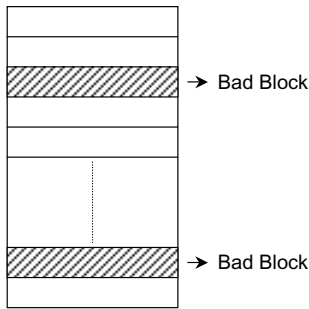

→ Bad Block

→ Bad Block

Figure 26.

At the time of shipment, all data bytes in a Valid Block are FFH. For Bad Block, all bytes are not in the FFH state. Please don't perform erase operation to Bad Block.
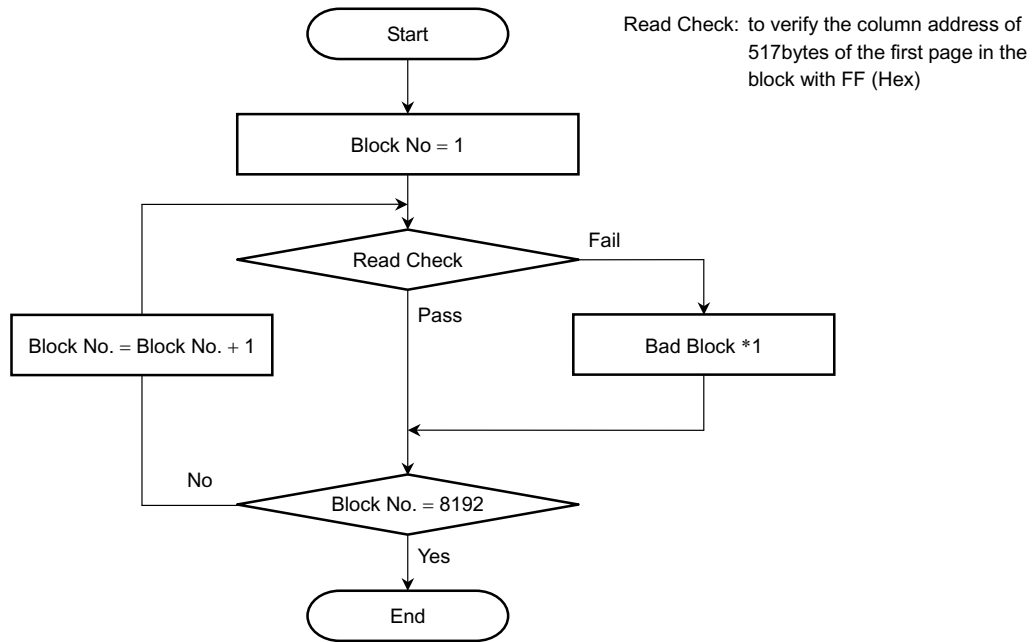
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	8032	—	8192	Block

Bad Block Test Flow

Read Check: to verify the column address of 517bytes of the first page in the block with FF (Hex)

*1: No erase operation is allowed to detected bad blocks

Figure 27

(15)   Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

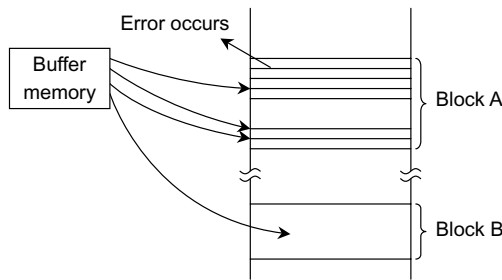| FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	(1) Block Verify after Program → Retry
		(2) ECC

- ECC: Error Correction Code

- Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Figure 28.

Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16)   Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

Package Dimensions

TSOPI48-P-1220-0.50   Unit: mm