TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

512-MBIT (64M × 8 BITS) CMOS NAND E^2PROM

DESCRIPTION

The device is a single 3.3 V 512Mbit (553,648,128 bit) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as 528 bytes × 32 pages × 4096 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages).

The device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization
  - Memory cell allay 528 × 128K × 8
  - Register 528 × 8
  - Page size 528 bytes
  - Block size (16K + 512) bytes

- Modes
  - Read, Reset, Auto Page Program, Auto Block Erase, Status Read

- Mode control
  - Serial input/output
  - Command control

- Power supply
  - V_{CC} = 2.7 V to 3.6 V

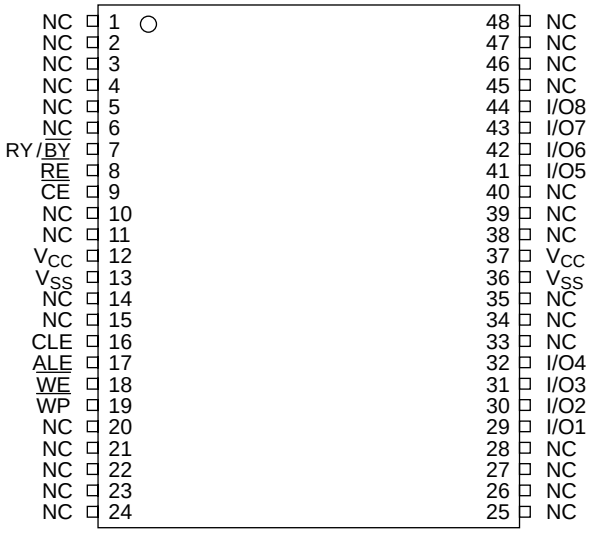
- Access time
  - Cell array to register 25 μs max
  - Serial Read Cycle 40 ns min

- Program/Erase time
  - Auto Page Program 300 μs/page typ.
  - Auto Block Erase 2.5 ms/block typ.

- Operating current
  - Read (40 ns cycle) 20 mA max.
  - Program (avg.) 20 mA max.
  - Erase (avg.) 20 mA max.
  - Standby 50 μA max

- Package
  - TSOPI48-P-1220-0.50 (Weight: 0.53g typ.)

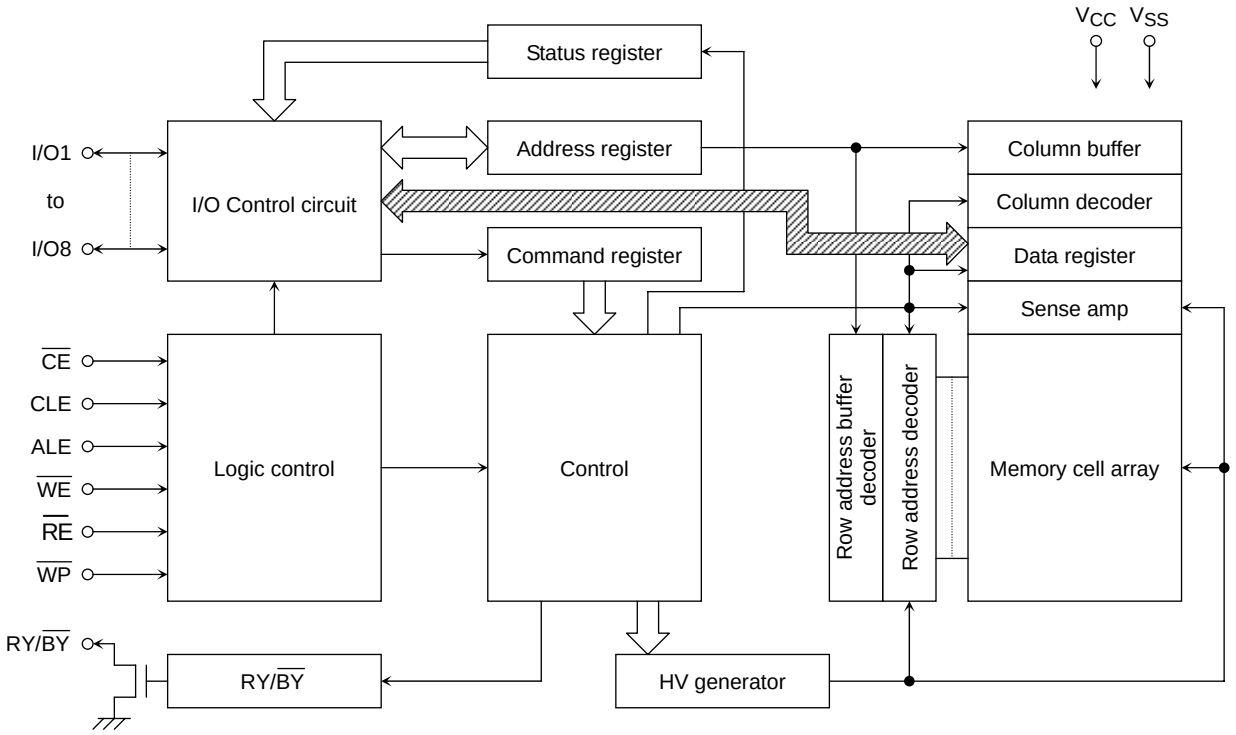
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input/Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55 to 125	°C
T_{opr}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	4016	—	4096	Blocks

(1) The device occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

(2) The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	—	3.6	V
V_{IH}	High Level input Voltage	$V_{CC} \times 0.78$	—	$V_{CC} + 0.3$	V
V_{IL}	Low Level Input Voltage	−0.3*	—	$V_{CC} \times 0.22$	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 40 ns	—	—	20	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 40 ns	—	—	20	mA
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 40 ns	—	—	20	mA
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 40 ns	—	—	20	mA
I_{CCO7}	Programming Current	—	—	—	20	mA
I_{CCO8}	Erasing Current	—	—	—	20	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V	—	8	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

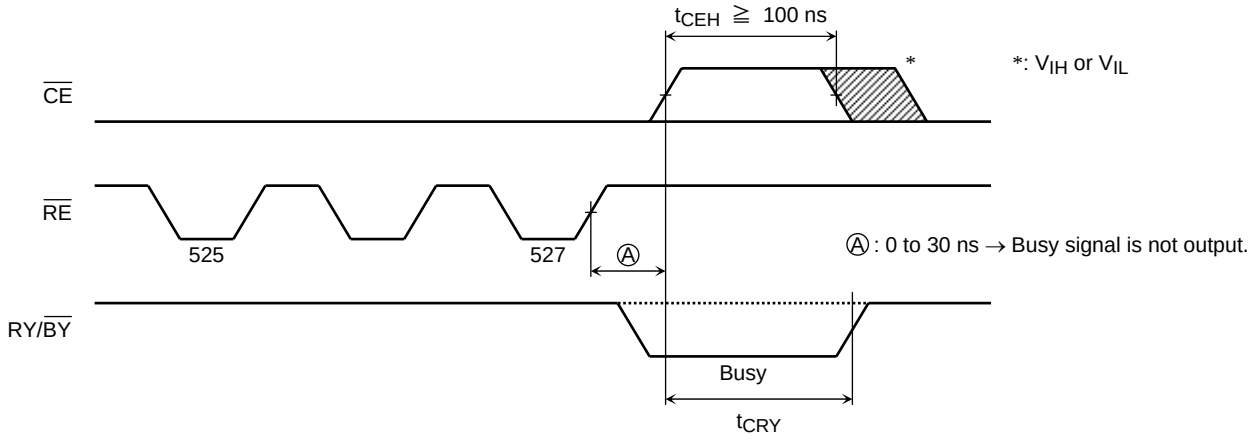
(Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time (*1)	20	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time (*2)	30	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	20	—	ns	
t_{ALS}	ALE Setup Time (*1)	20	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	5	—	ns	
t_{WC}	Write Cycle Time	40	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	20	—	ns	
t_{RC}	Read Cycle Time	40	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	—	30	ns	
t_{CEA}	$\overline{CE}$ Access Time (Serial Data Access)	—	35	ns	
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns	
t_{ALEA}	ALE Access Time (ID Read)	—	40	ns	
t_{CEH}	$\overline{CE}$ High Time for Last Address in Serial Read Cycle	100	—	ns	(2)
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_R	Memory Cell Array to Starting Address	—	25	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	10	—	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	—	130	ns	
t_{CRY}	$\overline{CE}$ High to Ready (When interrupted by $\overline{CE}$ in Read Mode)	—	5	μs	(1) (2)
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5 / 5 / 10 / 500	μs	

*1: tCLS and tALS can not be shorter than tWP

*2: tCS should be longer than tWP + 10ns.

Note: (1) $\overline{CE}$ High to Ready time depends on the pull-up resister tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)
(2) Sequential Read is terminated when t_{CEH} is greater than or equal to 100 ns. If the $\overline{RE}$ to $\overline{CE}$ delay is less than 30 ns, RY/$\overline{BY}$ signal stays Ready.



AC TEST CONDITIONS

PARAMETER	CONDITION
Vcc	2.7V to 3.6V
Input level	V_{CC} − 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	V_{CC} / 2
Output data comparison level	V_{CC} / 2
Output load	C_L (100 pF) + 1 TTL

PROGRAMMING AND ERASING CHARACTERISTICS

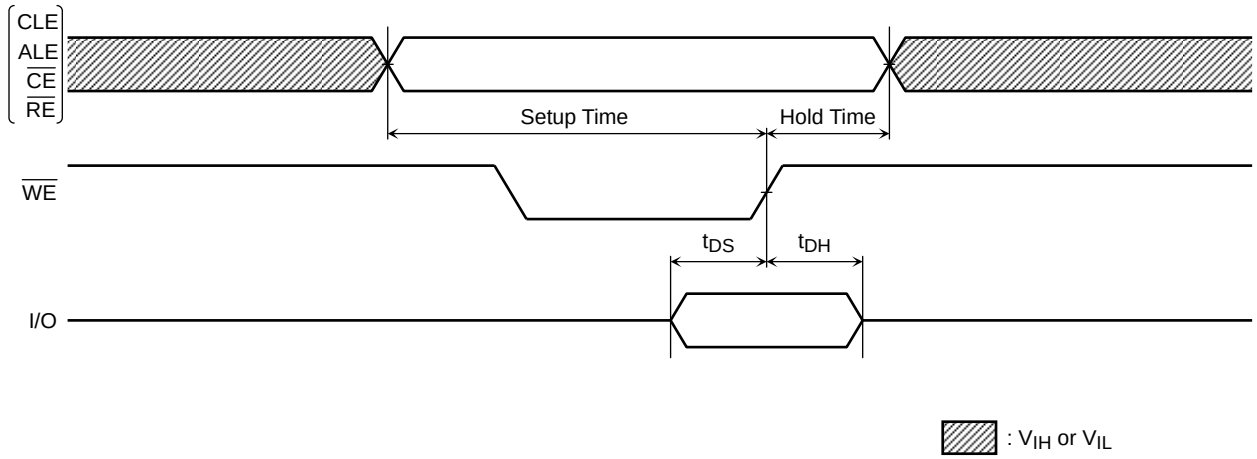
(Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	300	700	μs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t_{BERASE}	Block Erasing Time	—	2.5	7	ms	

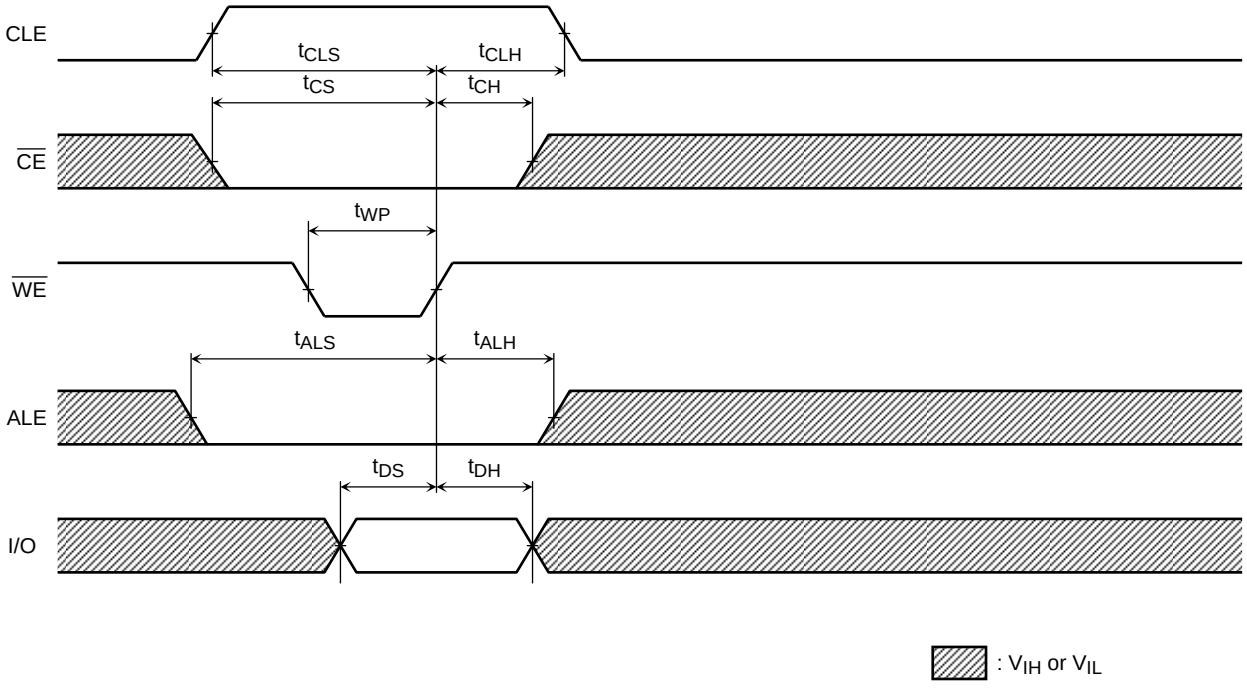
(1): Refer to Application Note (12) toward the end of this document.

TIMING DIAGRAMS

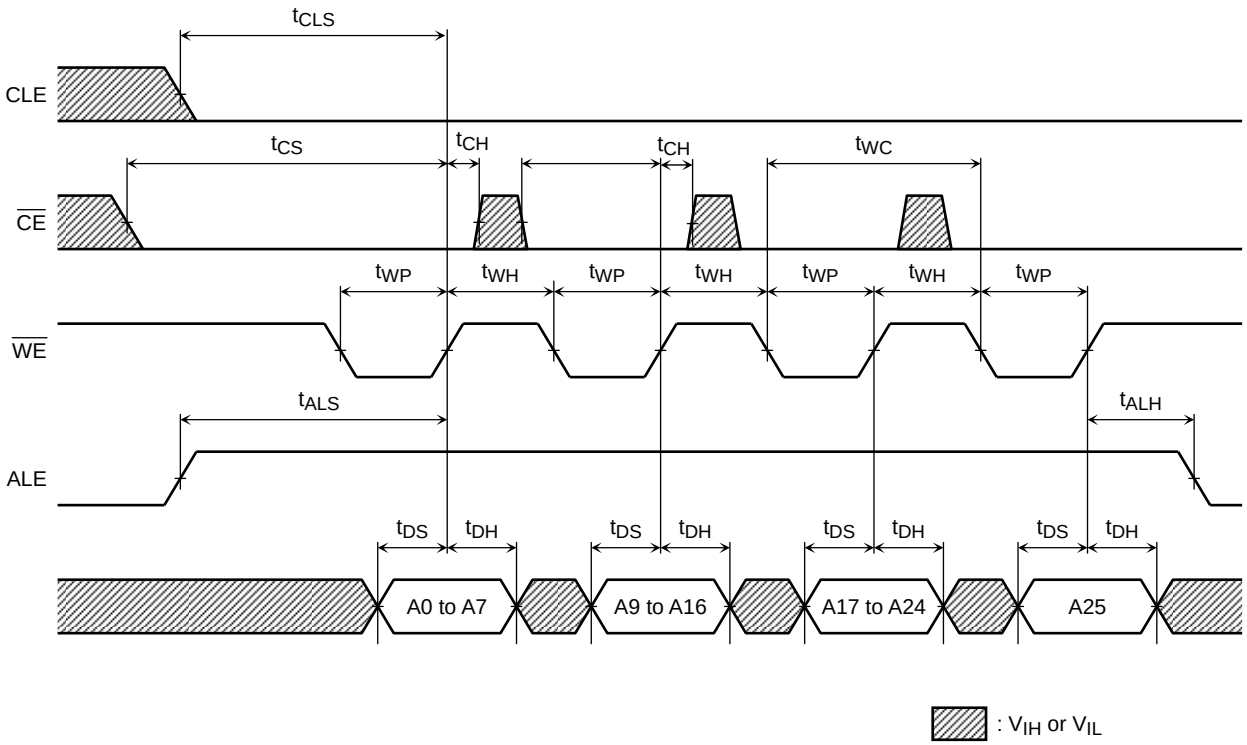
Latch Timing Diagram for Command/Address/Data



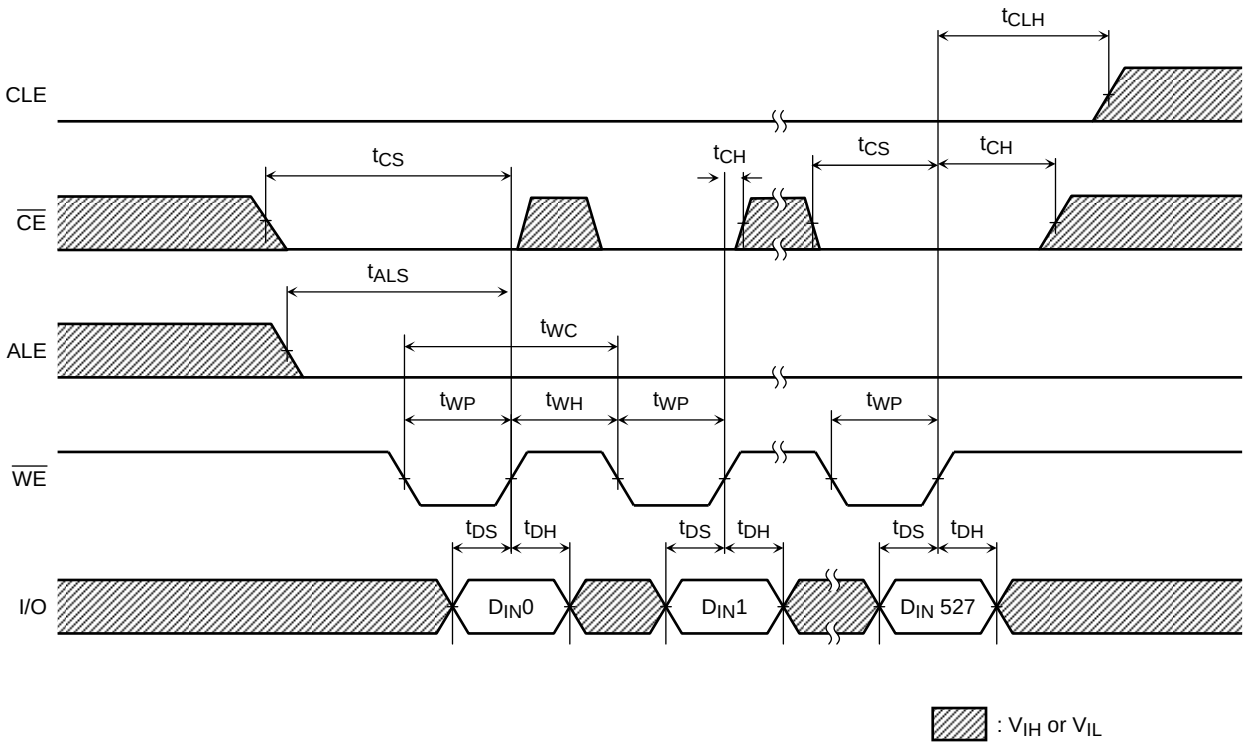
Command Input Cycle Timing Diagram



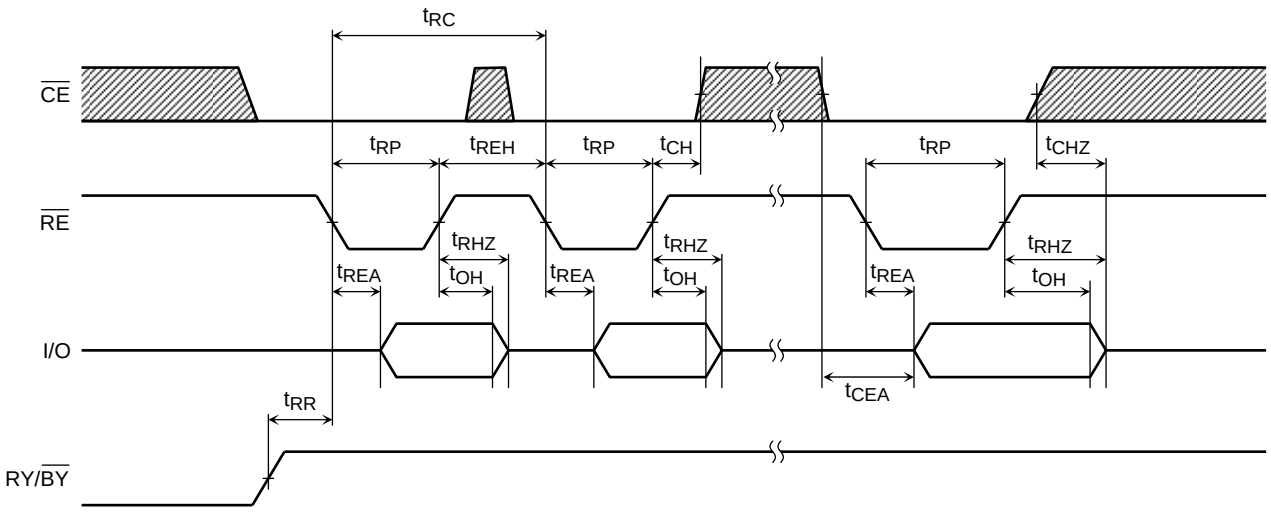
Address Input Cycle Timing Diagram



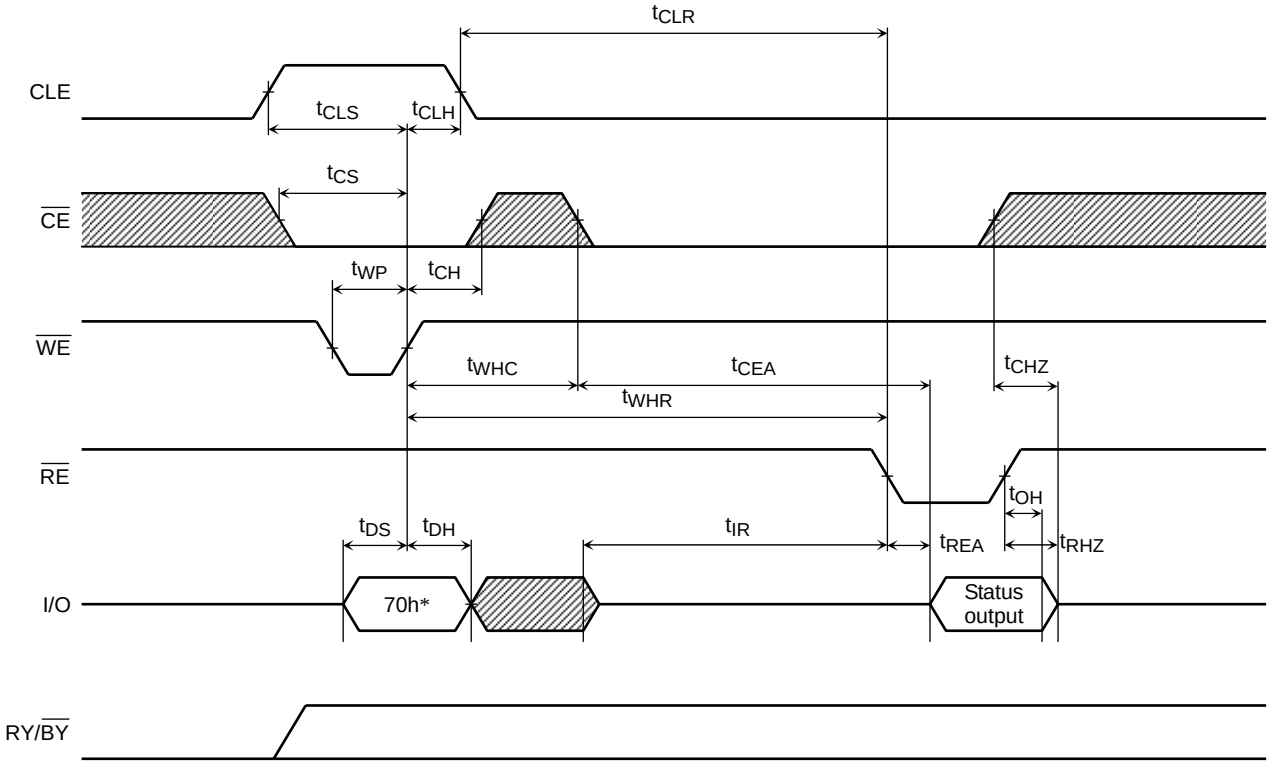
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



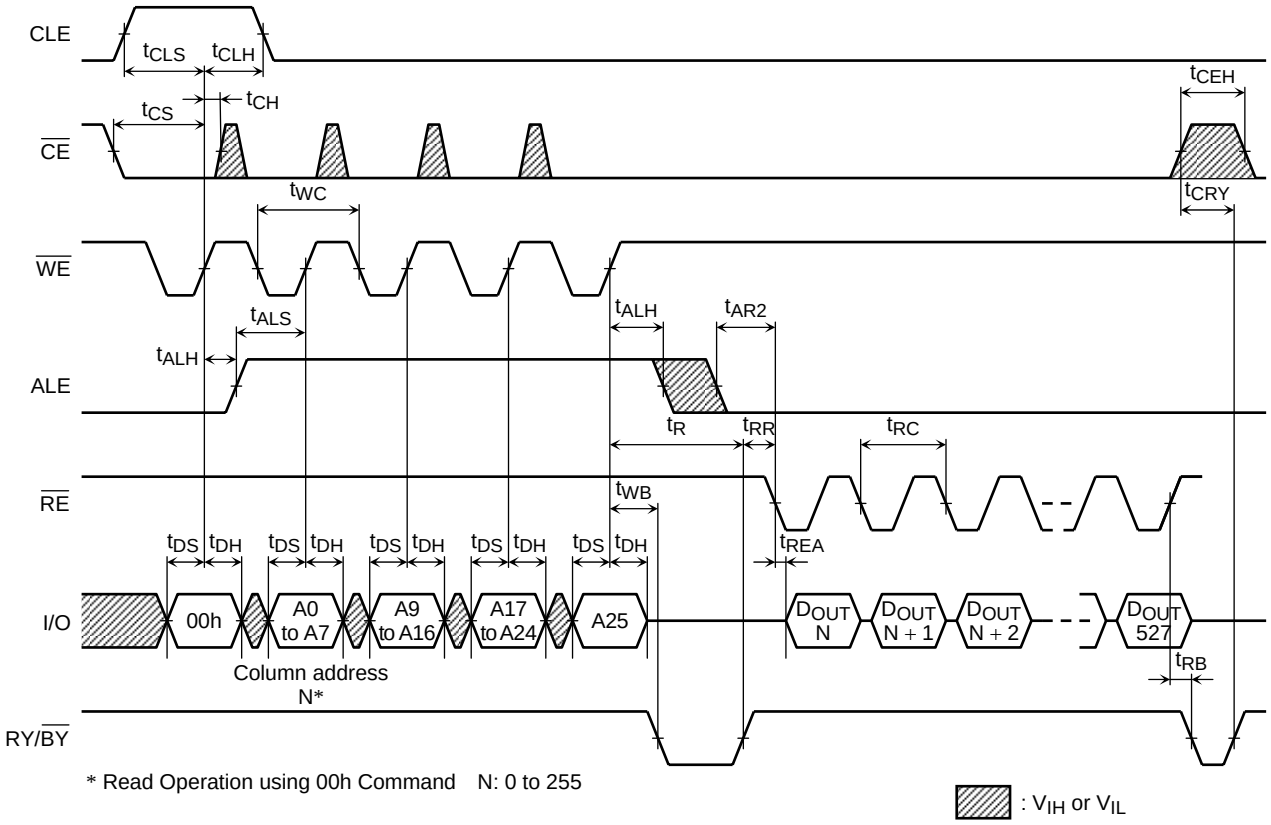
Status Read Cycle Timing Diagram



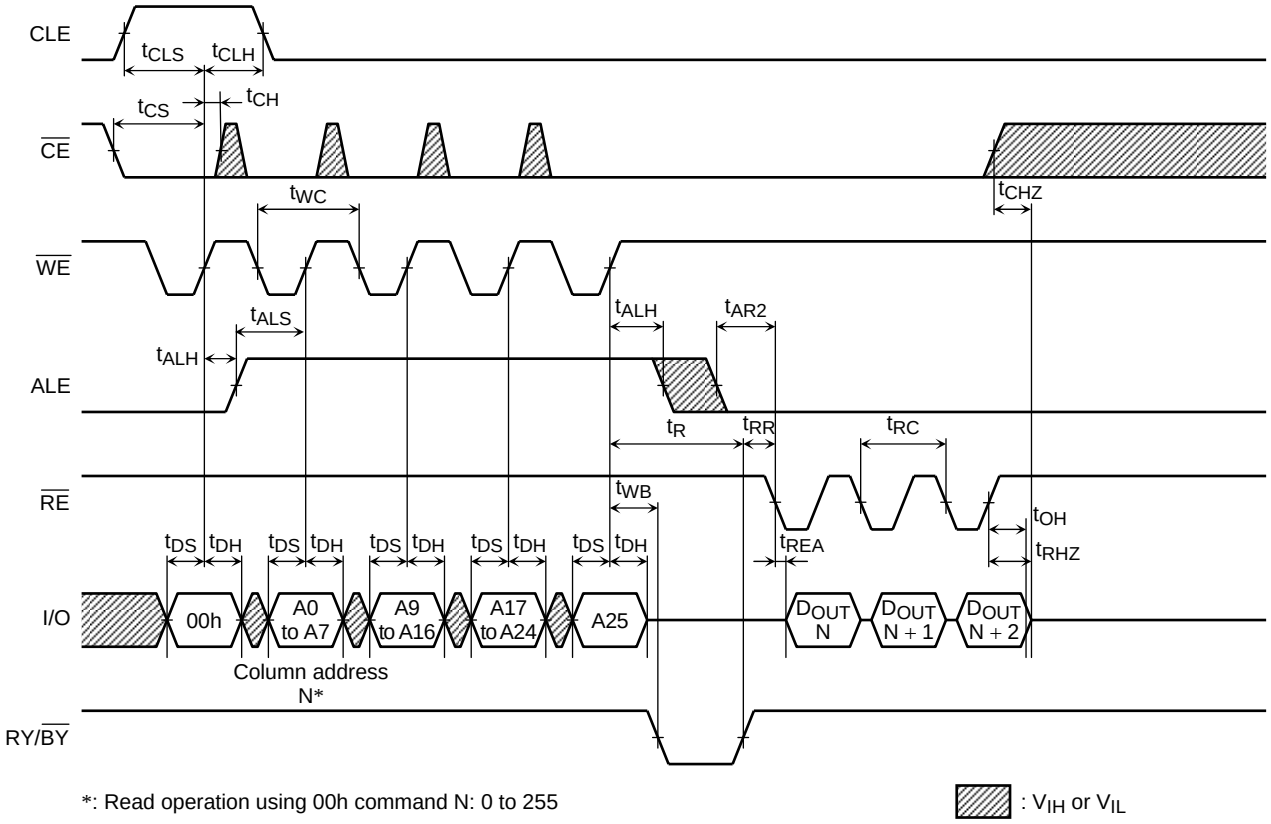
* 70h represents the hexadecimal number

: V_{IH} or V_{IL}

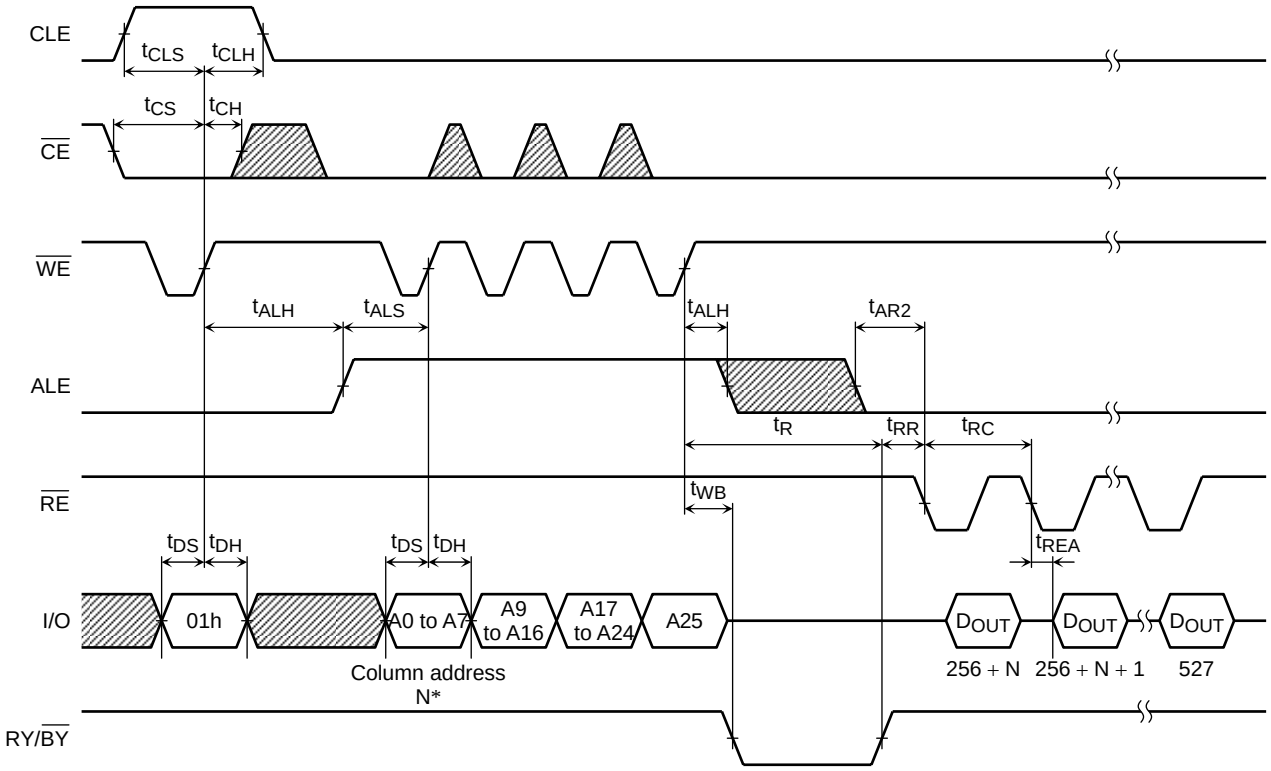
Read Cycle (1) Timing Diagram



Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$

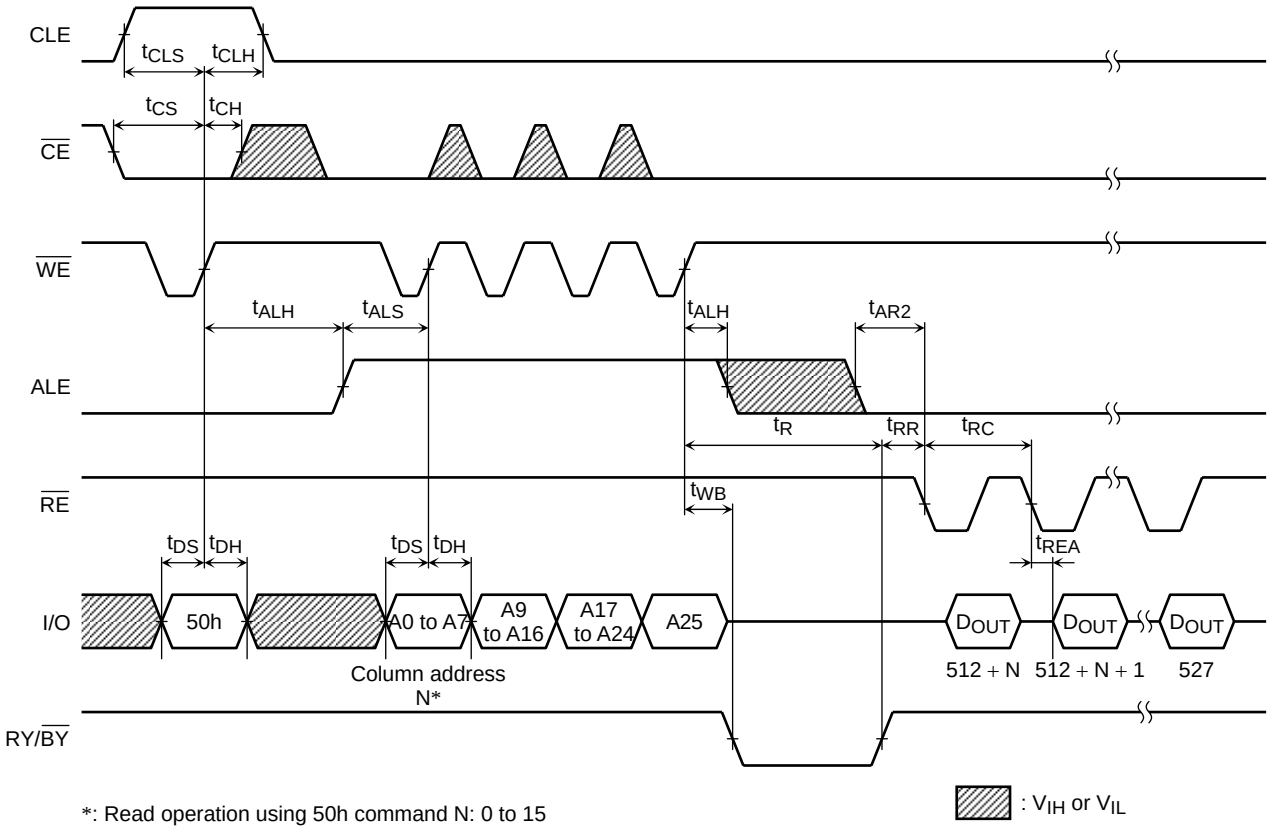


Read Cycle (2) Timing Diagram



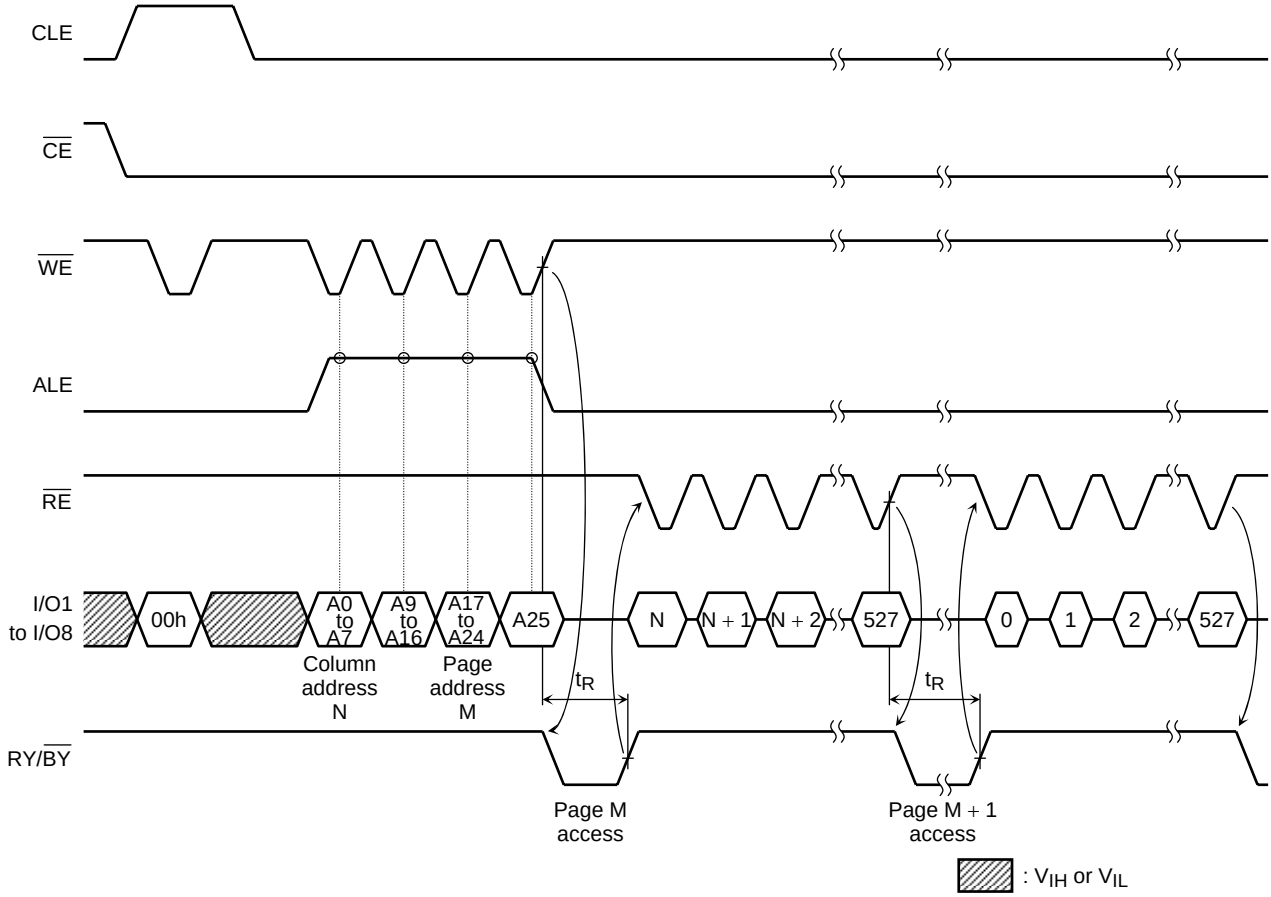
*: Read operation using 01h command N: 0 to 255

Read Cycle (3) Timing Diagram

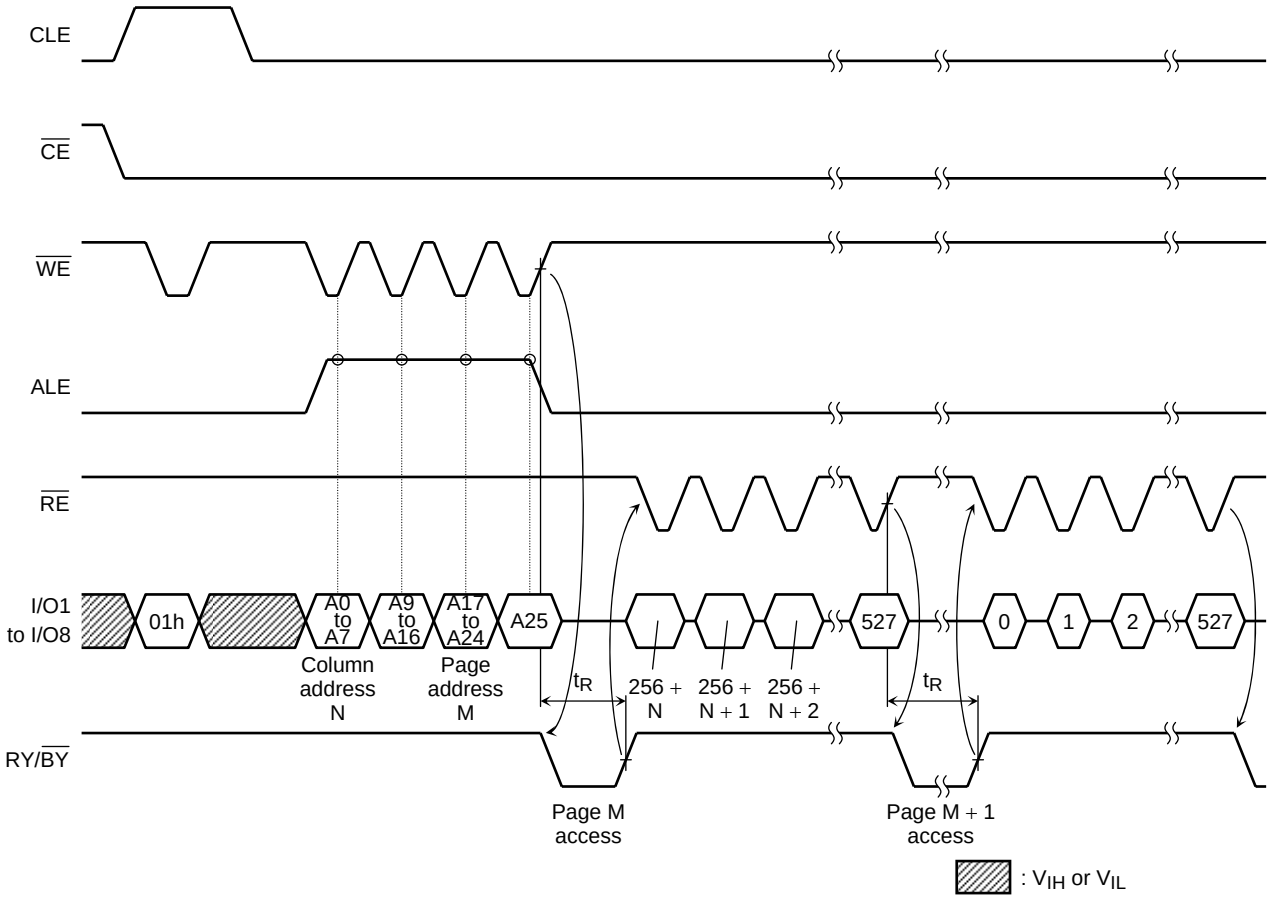


*: Read operation using 50h command N: 0 to 15

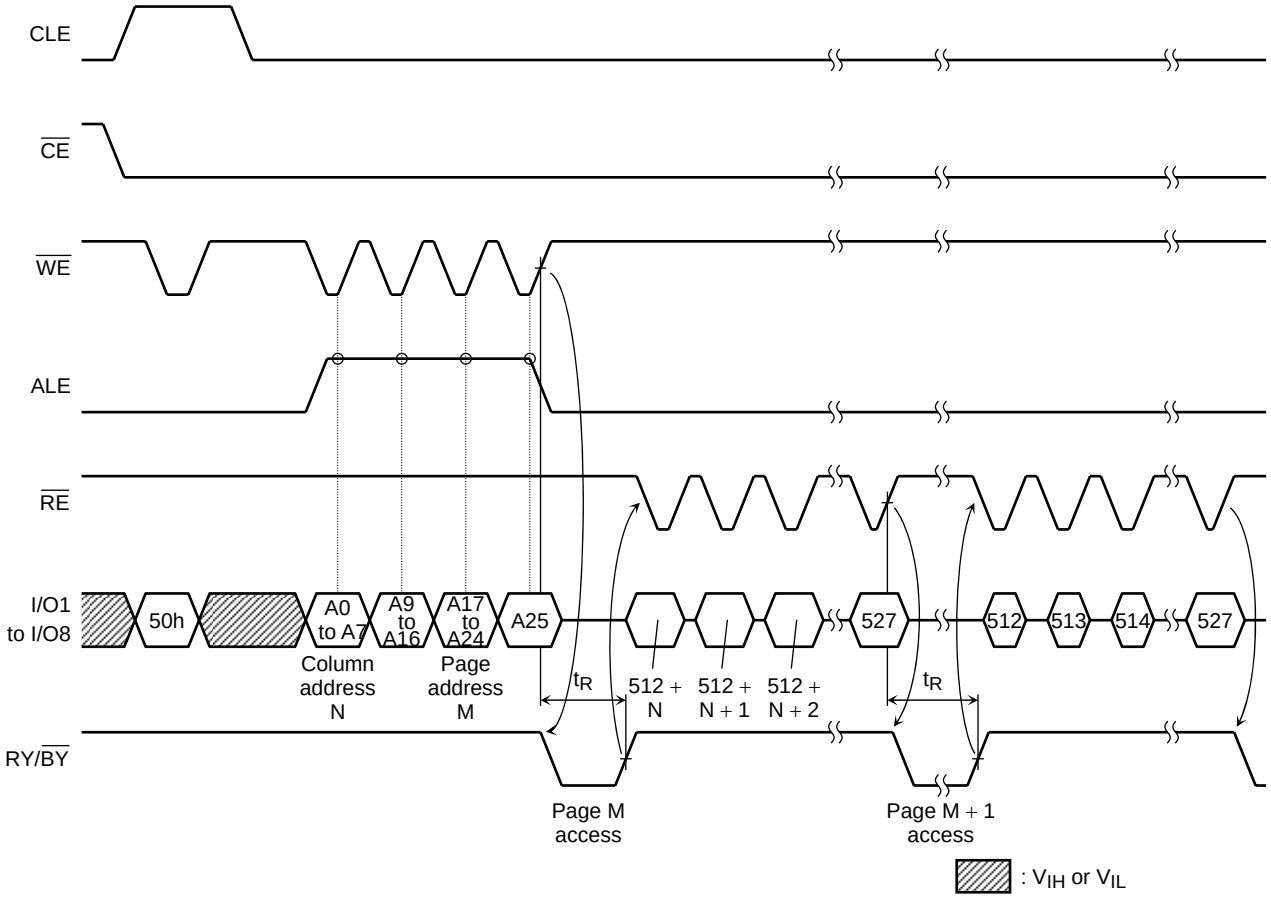
Sequential Read (1) Timing Diagram



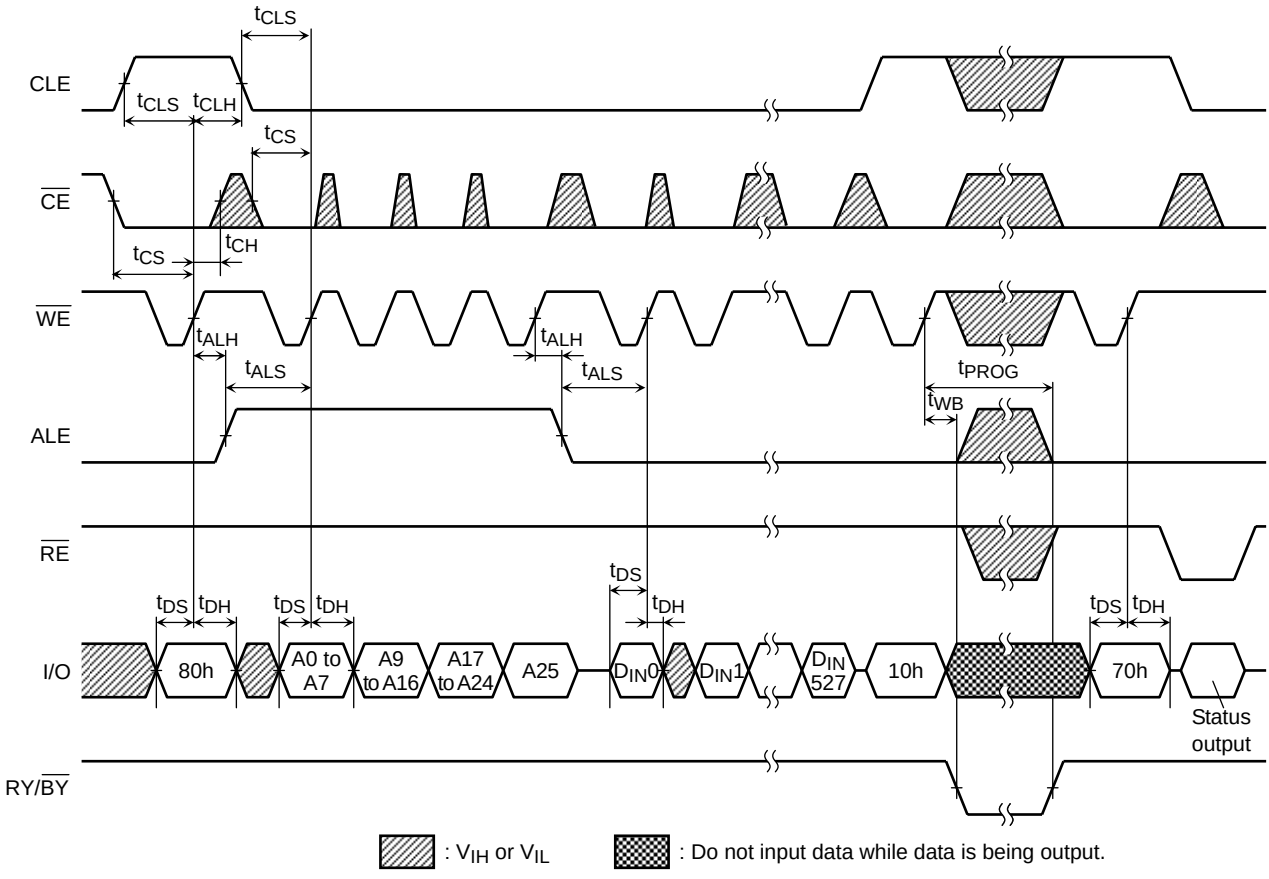
Sequential Read (2) Timing Diagram



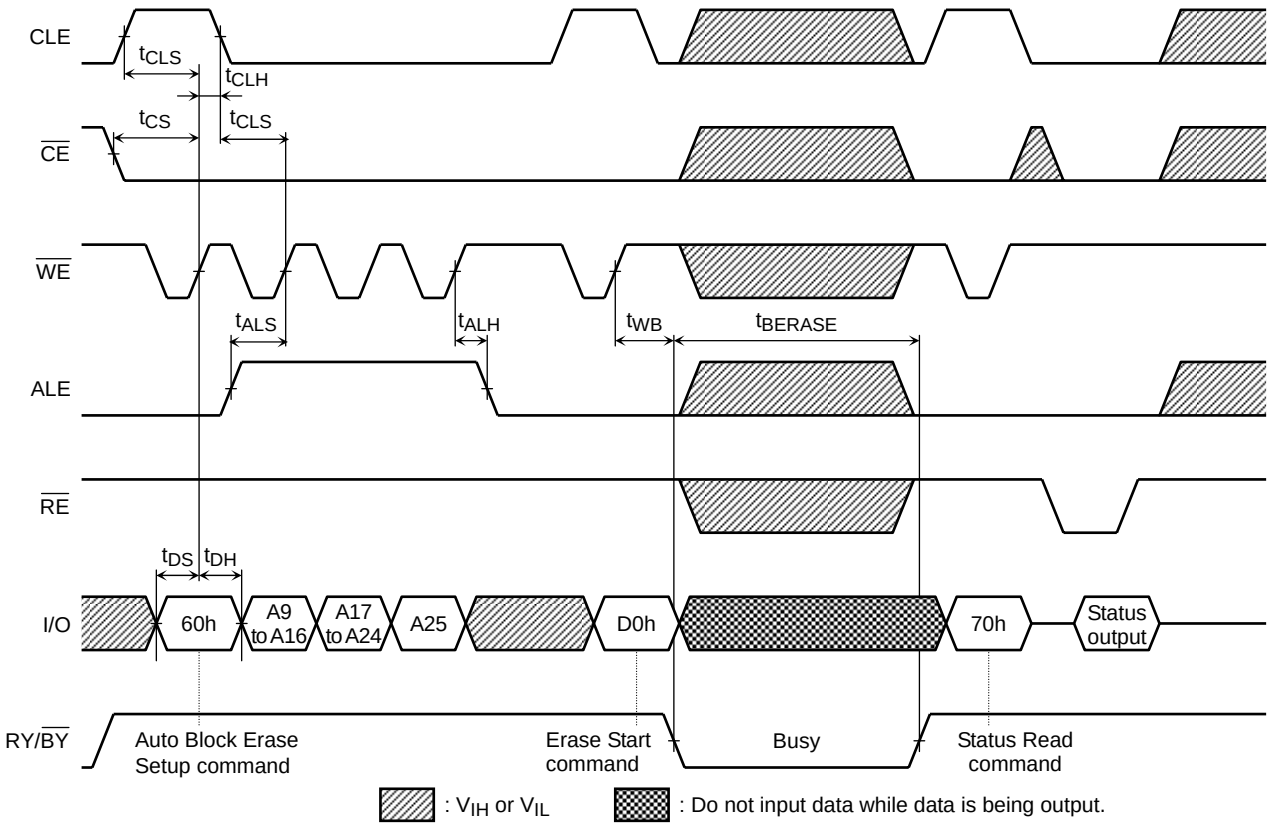
Sequential Read (3) Timing Diagram



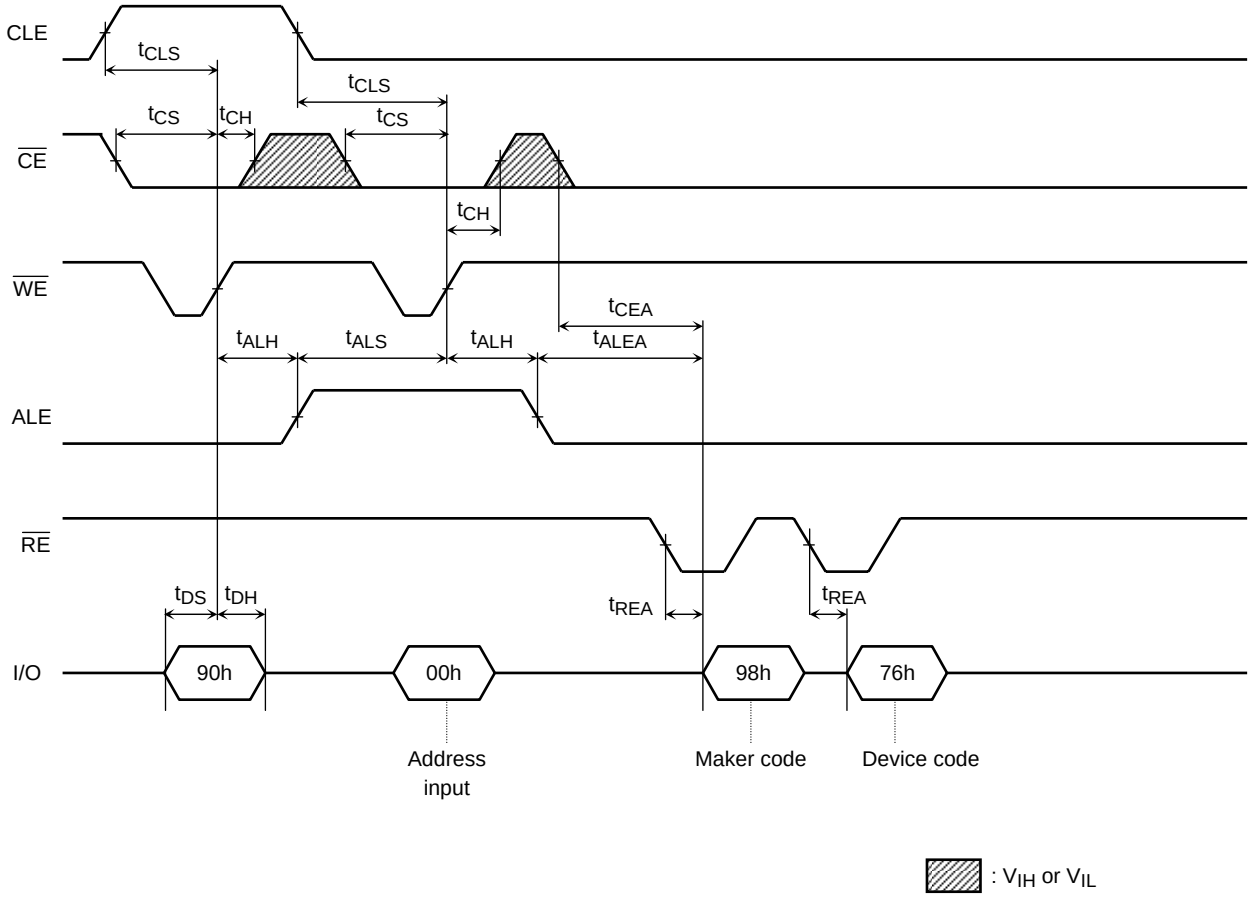
Auto-Program Operation Timing Diagram



Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of $\overline{WE}$ if ALE is High. Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a wait state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY/$\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY/ $\overline{BY}$

The RY/$\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY/$\overline{BY}$ signal is in Busy state (RY/$\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state (RY/$\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

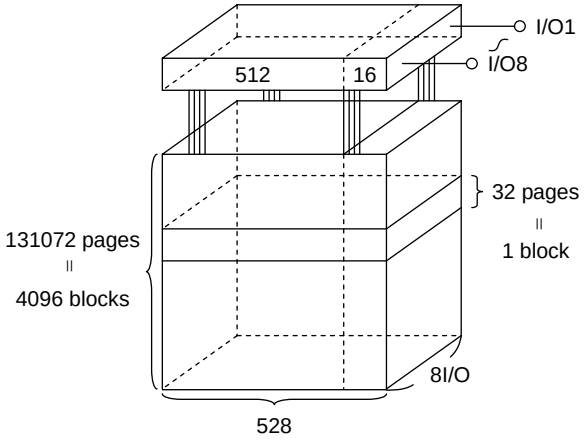


Figure 1. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 32 pages = (16K + 512) bytes
Capacity = 528 bytes × 32 pages × 4096 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	A24	A23	A22	A21	A20	A19	A18	A17
Fourth cycle	*L	*L	*L	*L	*L	*L	*L	A25

A0 to A7: Column address
A9 to A25: Page address
A14 to A25: Block address
A9 to A13: NAND address in block

* : A8 is automatically set to Low or High by a 00h command or a 01h command.
I/O2-8 must be set to Low in the fourth cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 4. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L		H	*
Address Input	L	H	L		H	*
Data Input	L	L	L		H	H
Serial Data Output	L	L	L	H		*
During Programming (Busy)*2	*	*	*	*	*	H
During Erasing (Busy)*2	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: The $\overline{CE}$ signal is ignored when device is in Busy state ($R/\overline{B}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Table 3 shows the operation states for Read mode.

Table 3. Read mode operation states

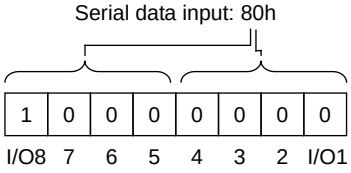
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL}

Table 4. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	○
Auto Program	10	—	
Auto Block Erase	60	D0	
Status Read	70	—	○
ID Read	90	—	

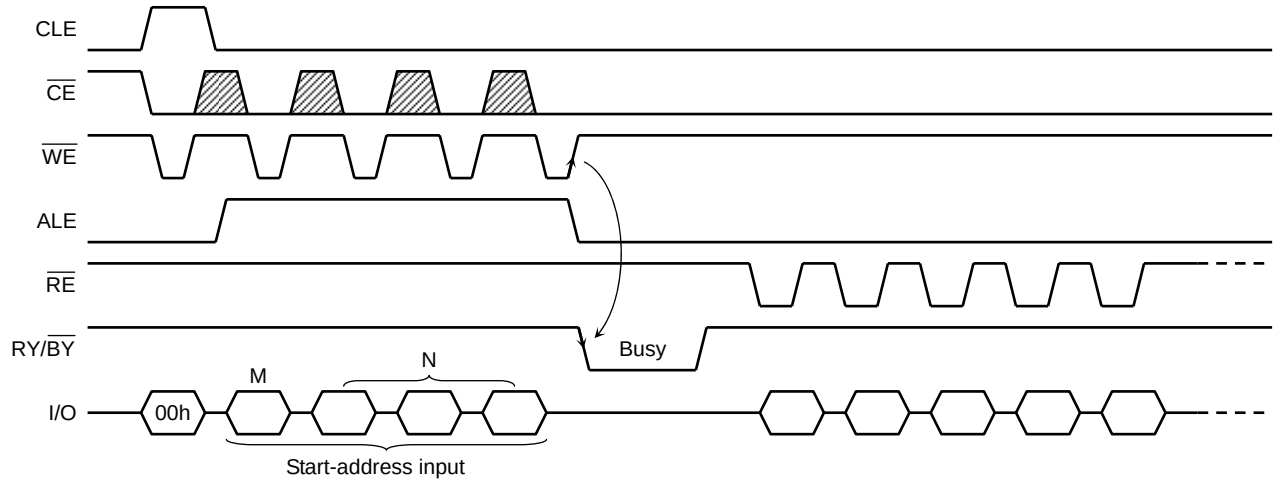
HEX data bit assignment
(Example)



DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00h command is issued to the Command register. Refer to Figure 2 below for timing details and the block diagram.



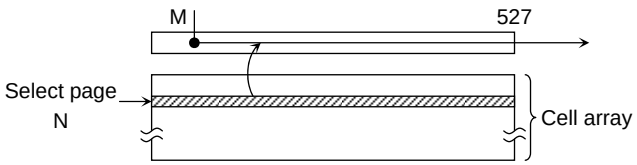
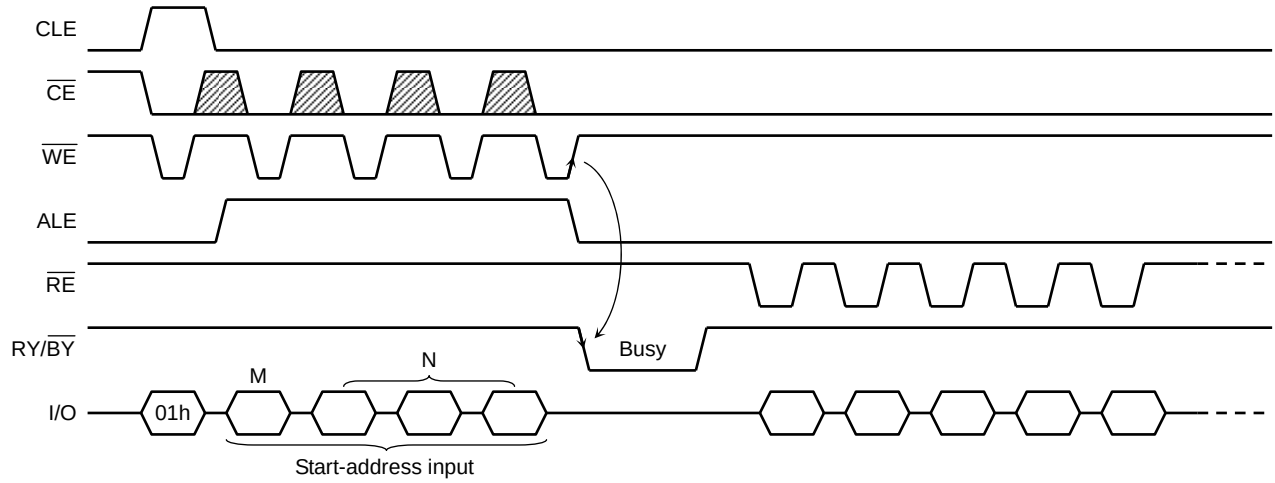


Figure 2. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the fourth cycle (after the address information has been latched). The device will be in Busy state during this transfer period.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)



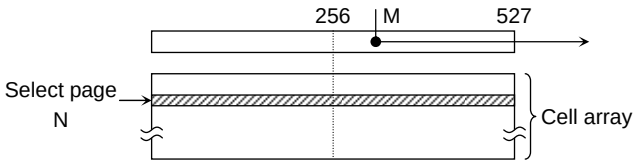


Figure 3. Read mode (2) operation

The operation of the device after input of the 01h command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2), but it is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

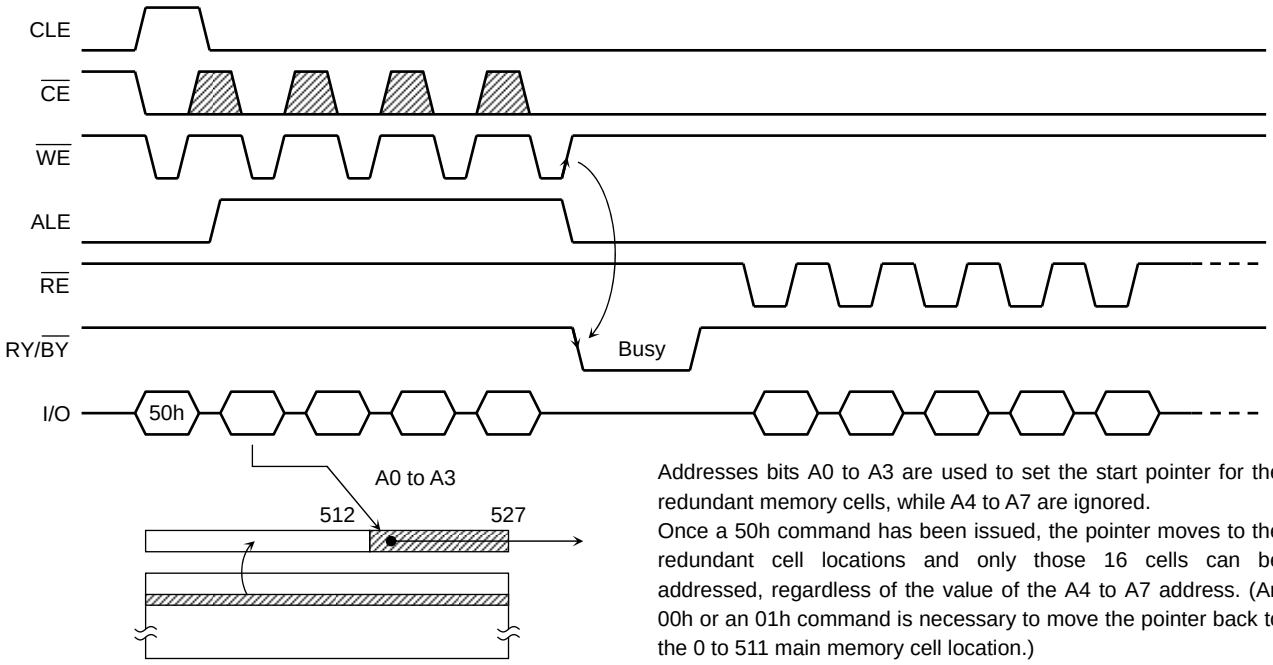
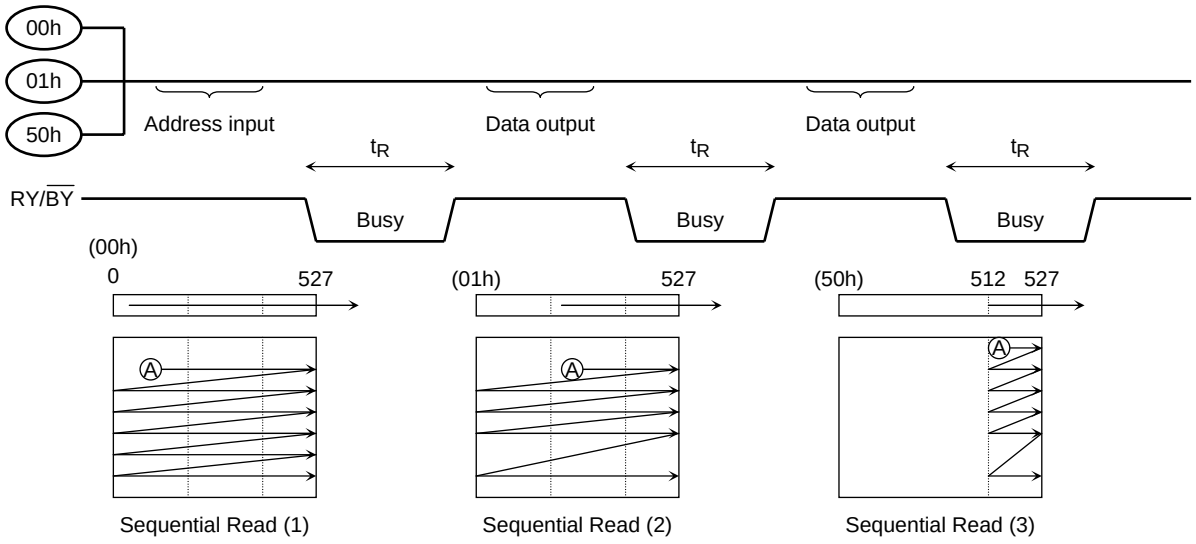


Figure 4. Read mode (3) operation

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored.
Once a 50h command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4 to A7 address. (An 00h or an 01h command is necessary to move the pointer back to the 0 to 511 main memory cell location.)

Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only.

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a Status Read command "70h" input. The resulting information is outlined in Table 5 .

Table 5. Status output table for Status Read command "70h"

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 5.

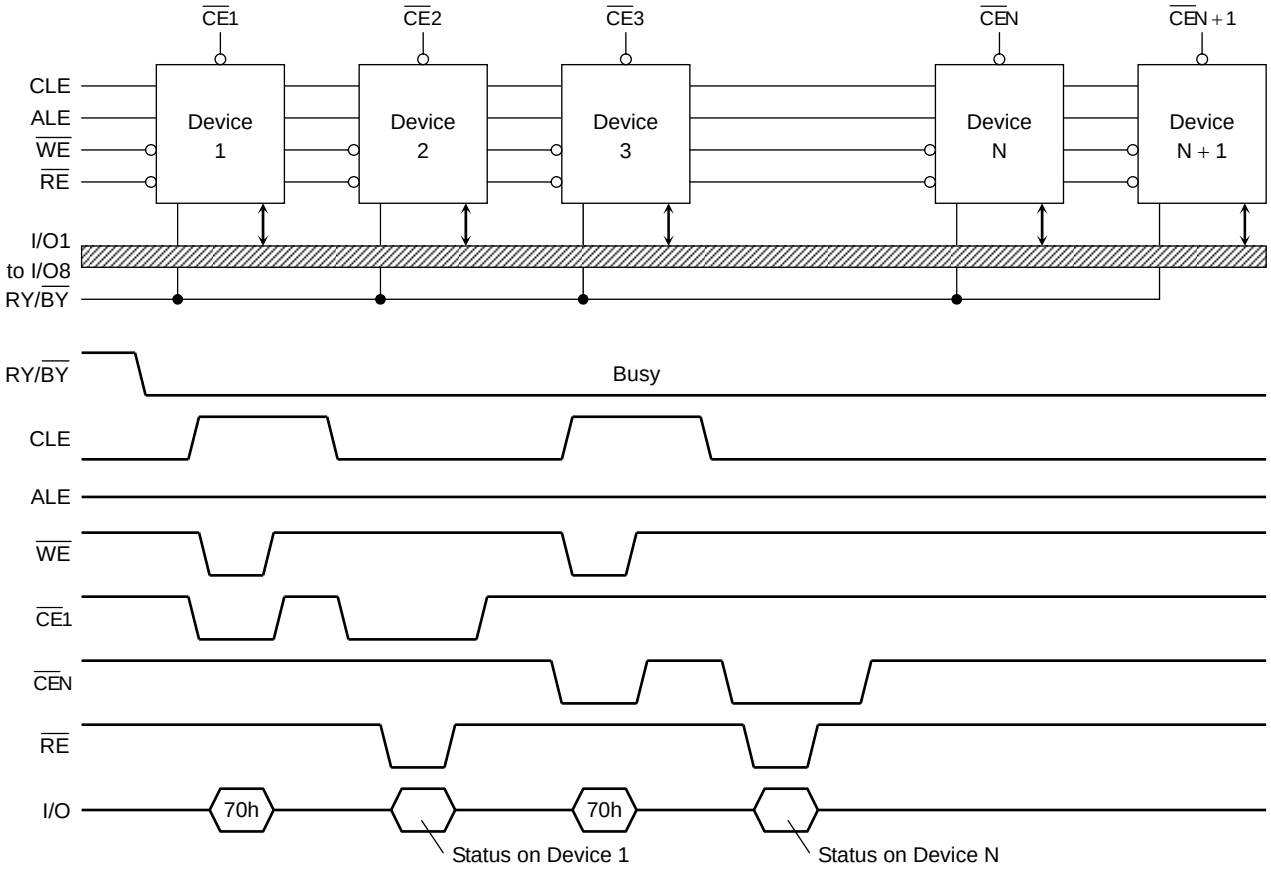


Figure 5. Status Read timing application example

System Design Note: If the RY/$\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

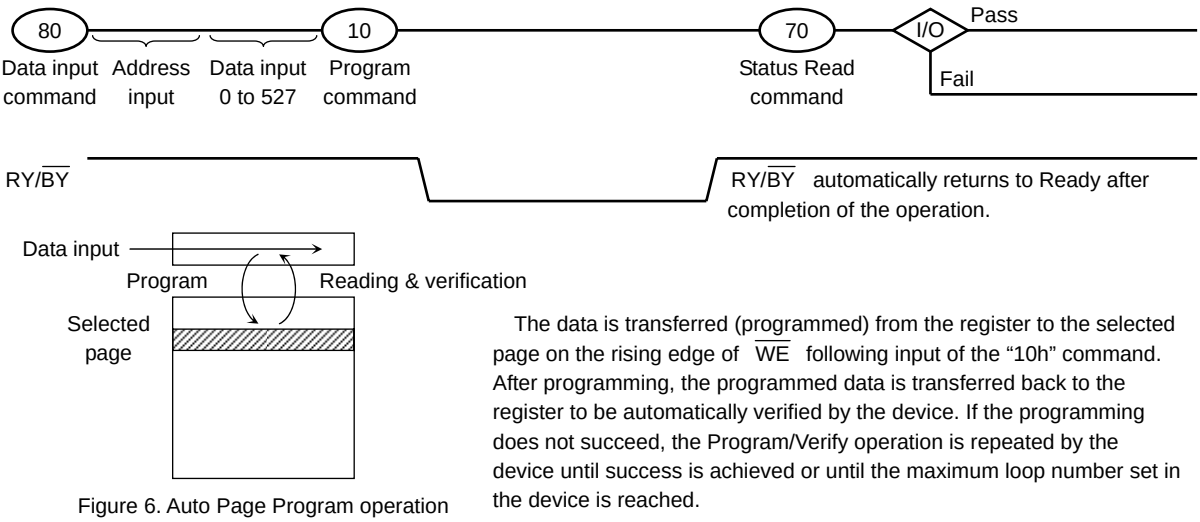
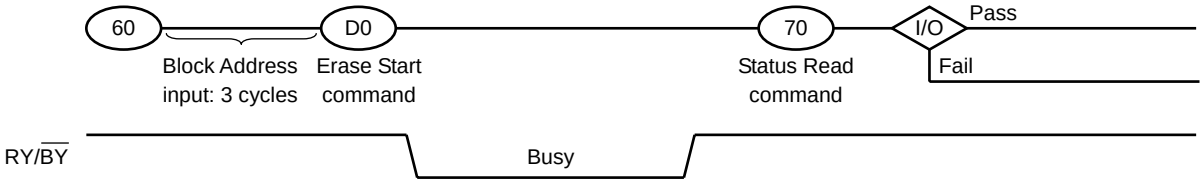


Figure 6. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the "10h" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an ertra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



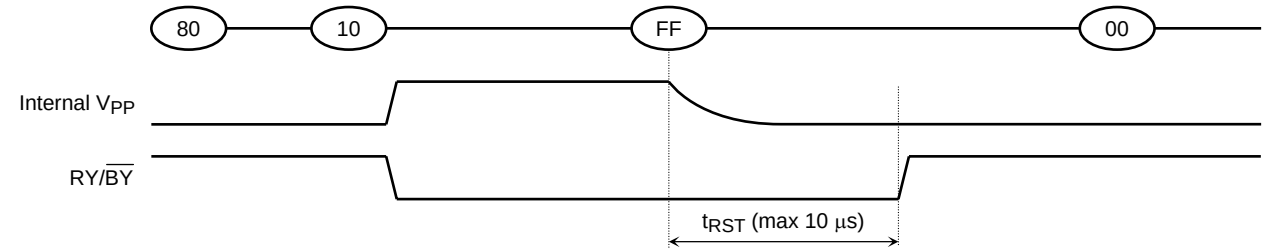
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFh" Reset command input during the various device operations is as follows:

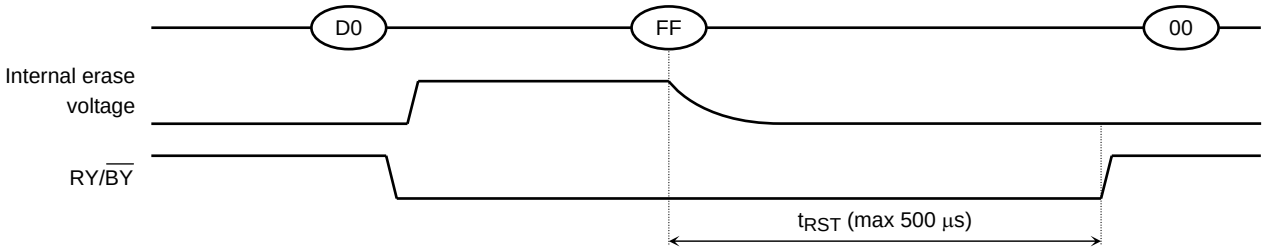
When a Reset (FFh) command is input during programming

Figure 7.



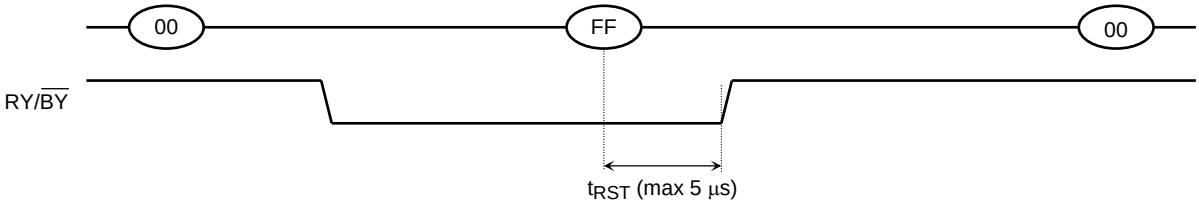
When a Reset (FFh) command is input during erasing

Figure 8.



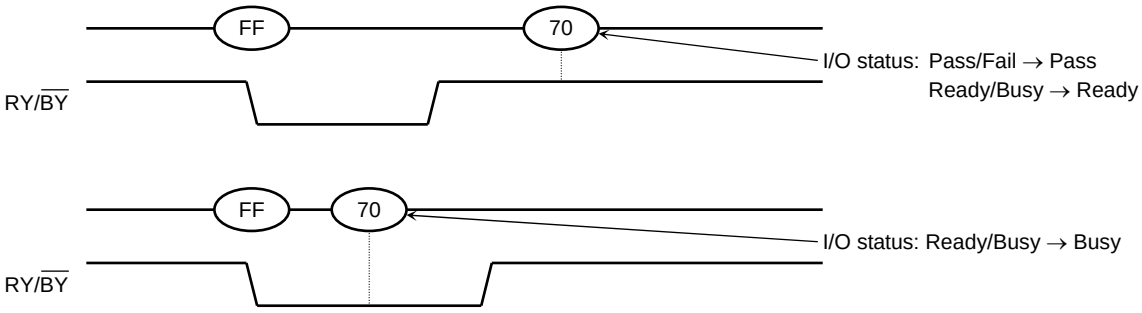
When a Reset (FFh) command is input during Read operation

Figure 9.



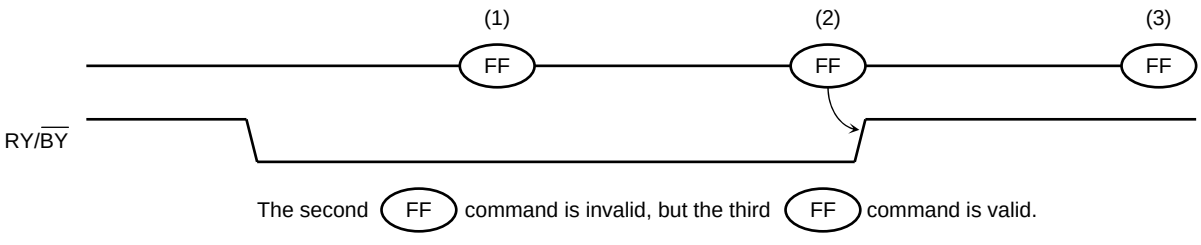
When a Status Read command (70h) is input after a Reset

Figure 10.



When two or more Reset commands are input in succession

Figure 11.



ID Read

ID Read command 90h provides maker code and device code. The ID codes can be read out under the following timing conditions:

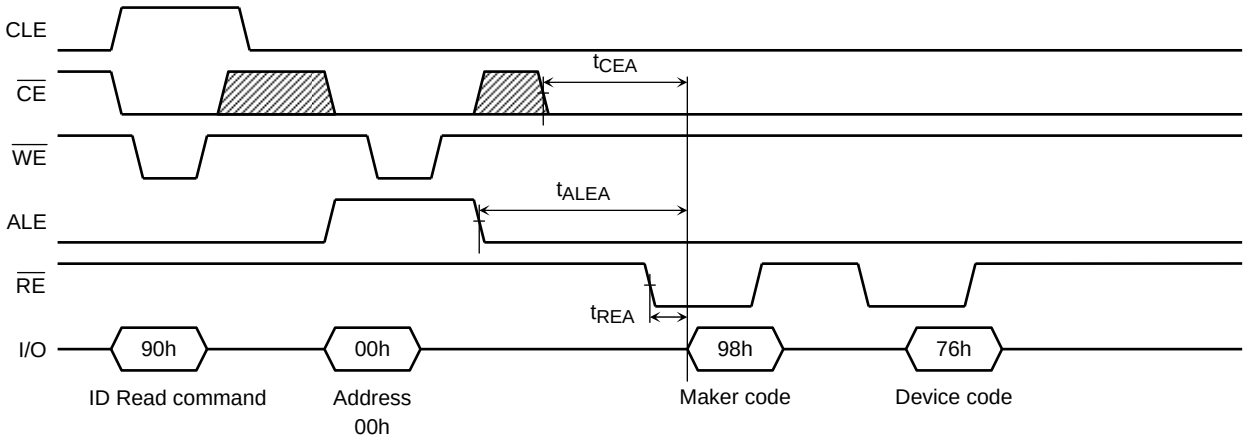


Figure 12. ID Read timing

Table 6. ID Codes read out by ID read command 90h

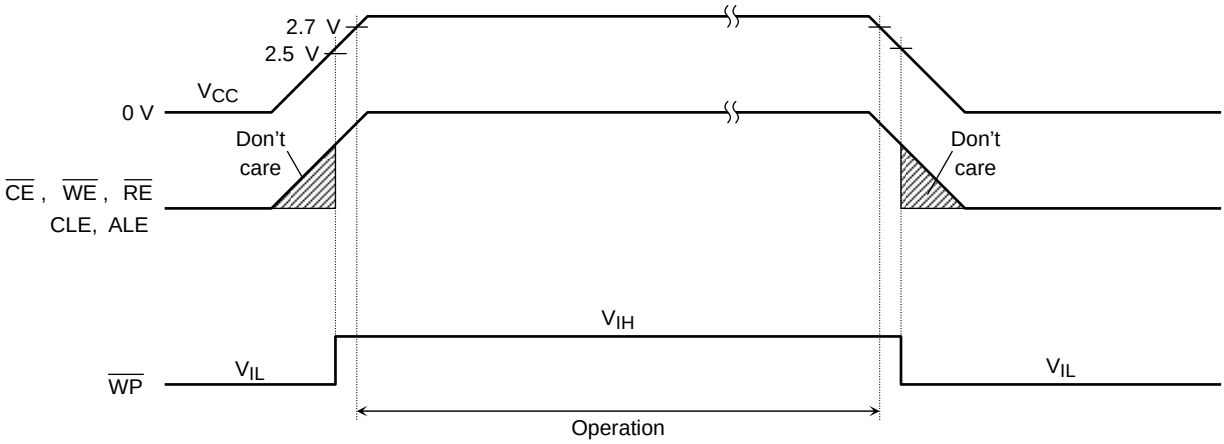
	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98h
Device code	0	1	1	1	0	1	1	0	76h

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The $\overline{WP}$ signal may be negated any time after the V_{CC} reaches 2.5 V and $\overline{CE}$ signal is kept high in power up sequence.



In order to operate this device stably, after V_{CC} becomes 2.5V, it should begin access after about 1ms.

Figure 13. Power-on/off Sequence

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

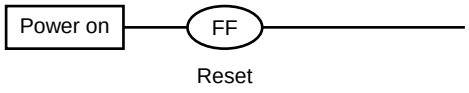


Figure 14.

(3) Prohibition of unspecified commands

The operation commands are listed in Table 4. Input of a command other than those specified in Table 4 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

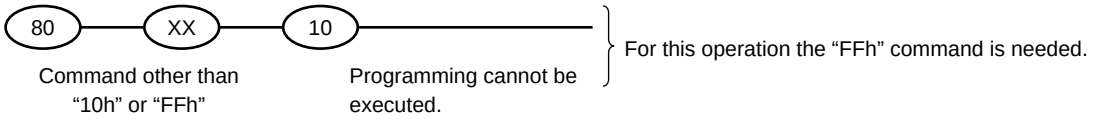
(4) Restriction of command while Busy state

During Busy state, do not input any command except 70h and FFh.

(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Program Execution command “10h” or the Reset command “FFh”.

If a command other than “10h” or “FFh” is input, the Program operation is not performed.



(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

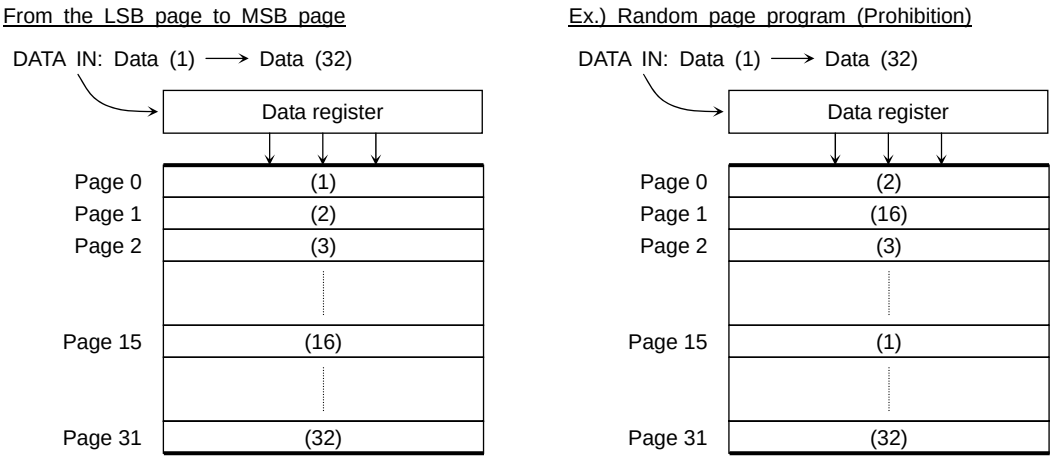


Figure 15. page programming within a block

(7) Status Read during a Read operation

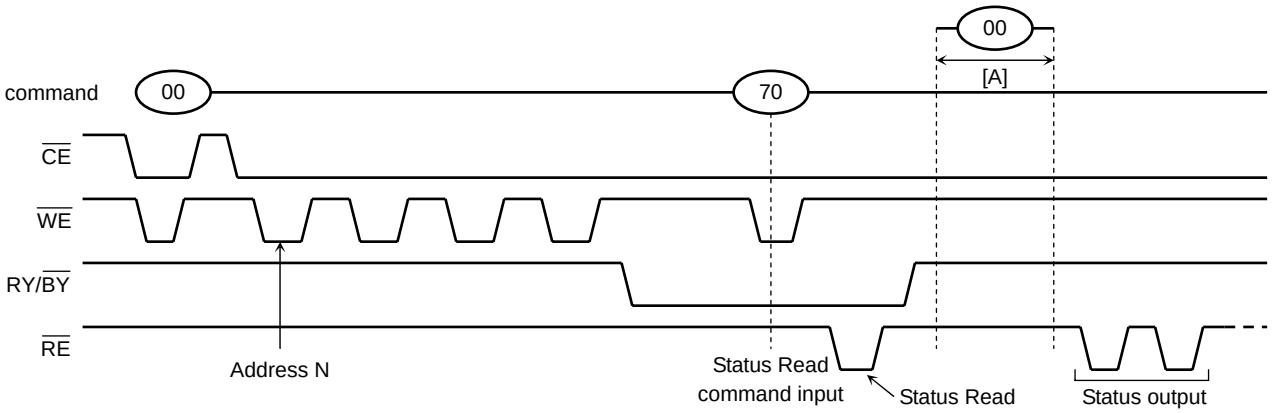


Figure 16.

The device status can be read out by inputting the Status Read command “70h” in Read mode.

Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command “00h” is inputted during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(8) Pointer control for “00h”, “01h” and “50h”

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 17 is a block diagram of their operations.

Table 7. Pointer Destination

Read Mode	Command	Pointer
(1)	00h	0 to 255
(2)	01h	256 to 511
(3)	50h	512 to 527

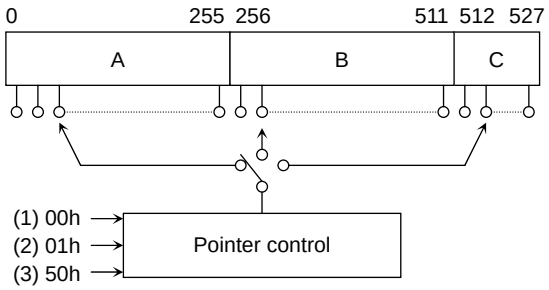
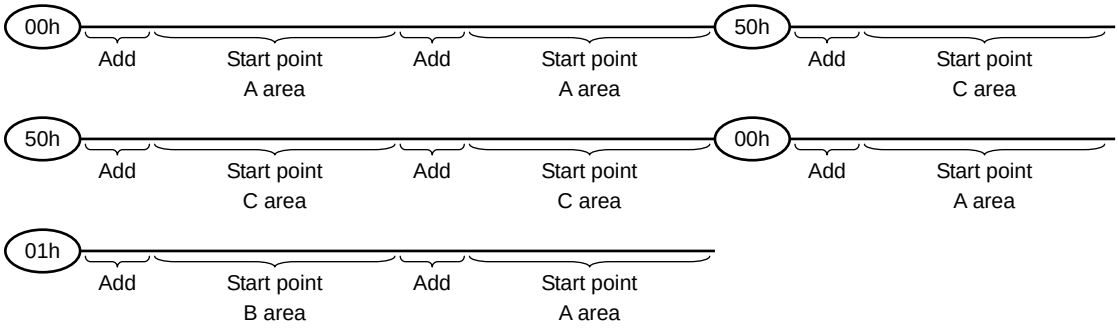


Figure 17 Pointer control

The pointer is set to region A by the “00h” command, to region B by the “01h” command, and to region C by the “50h” command.

(Example)

The “00h” command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50h command.

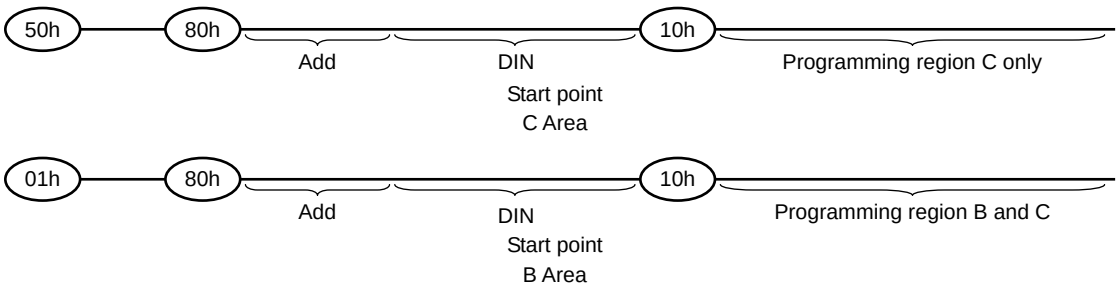


Figure 18. Example of How to Set the Pointer

(9) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.

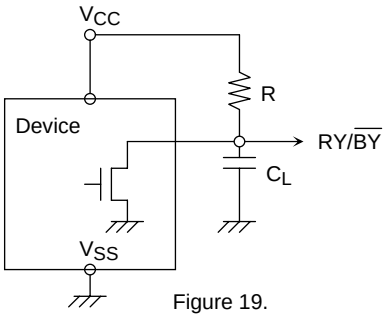
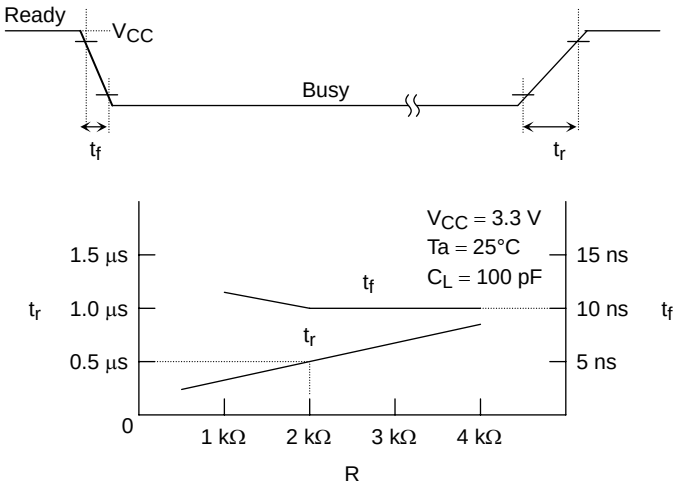


Figure 19.

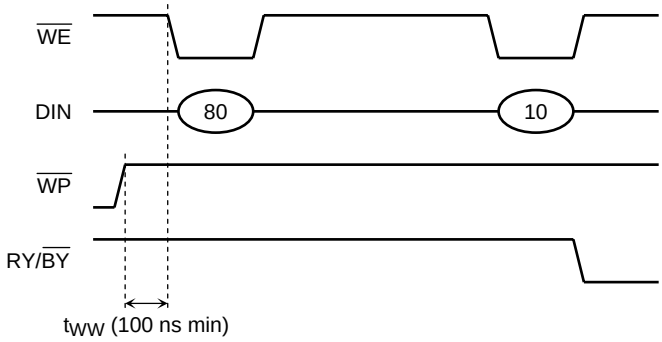


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

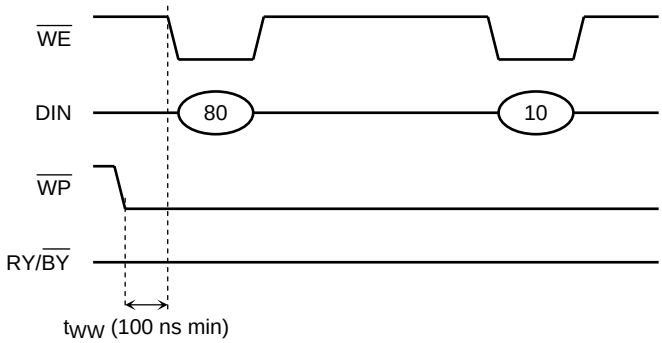
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

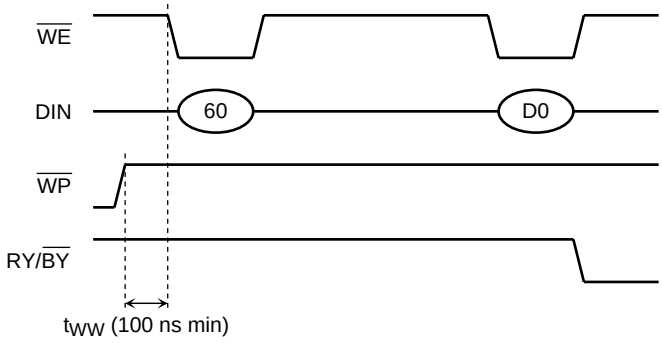
Enable Programming



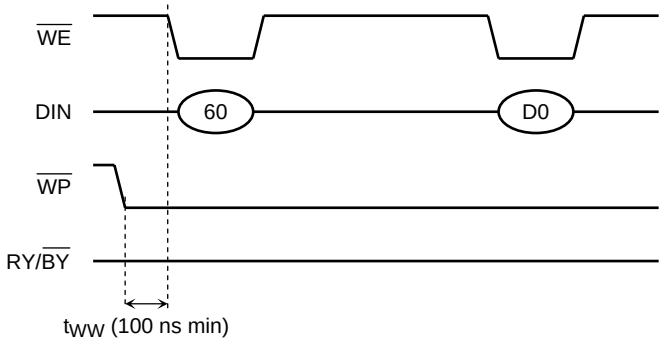
Disable Programming



Enable Erasing



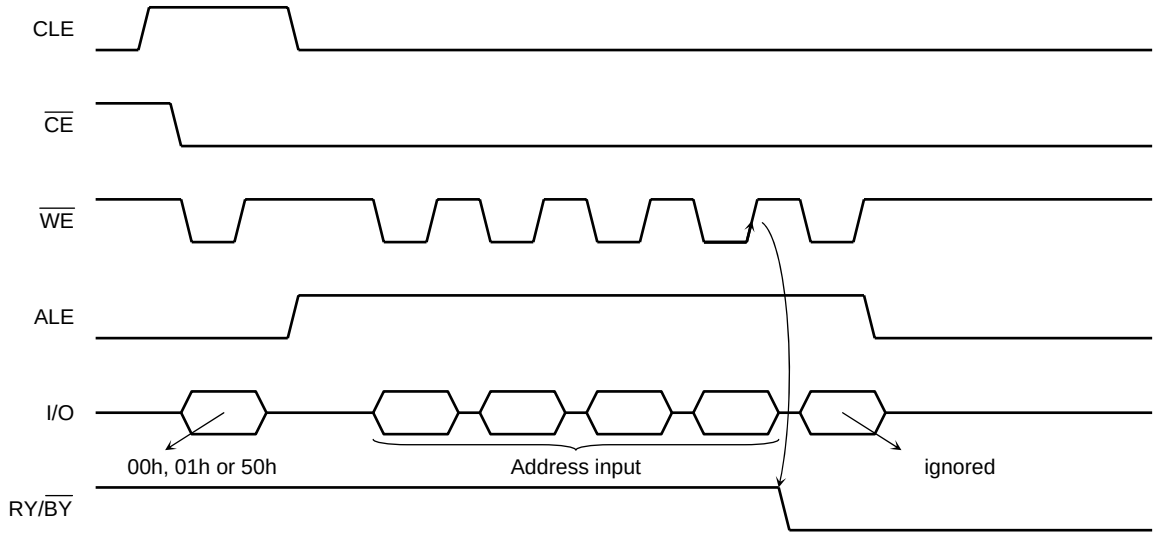
Disable Erasing



(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation



Internal read operation starts when $\overline{WE}$ goes High in the fourth cycle.

Figure 20.

Program operation

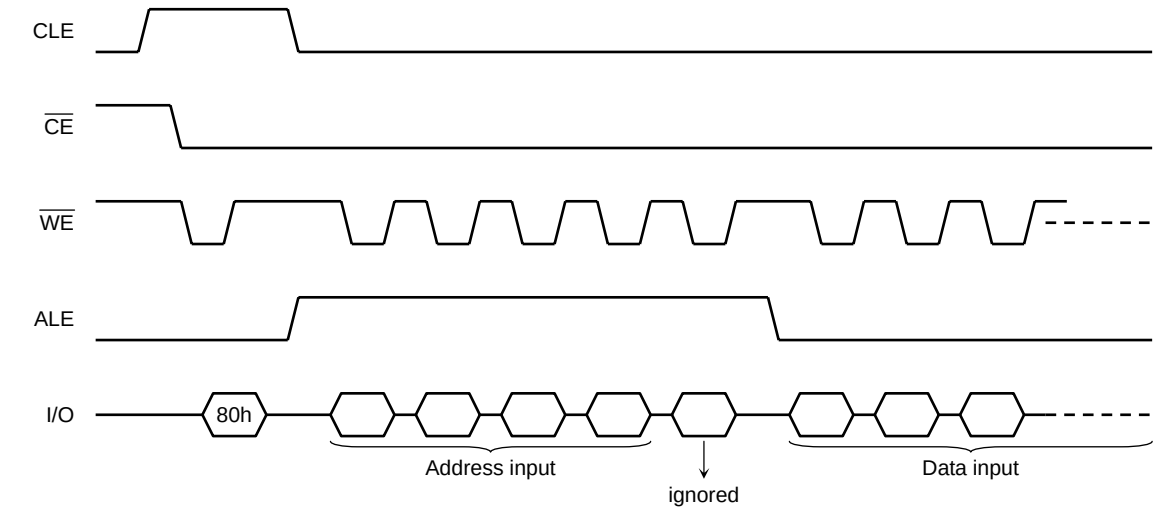


Figure 21.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

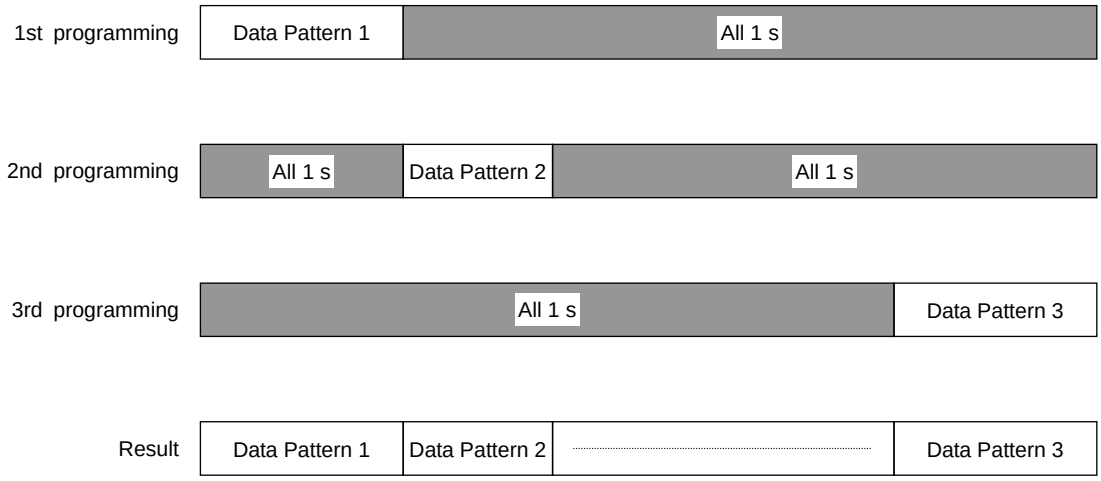


Figure 22

Note: The input data for unprogrammed or previously programmed page segments must be "1"

(13) Note regarding the $\overline{RE}$ signal

$\overline{RE}$ The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a "00h", "01h" or "50h" command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing, If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 23.)

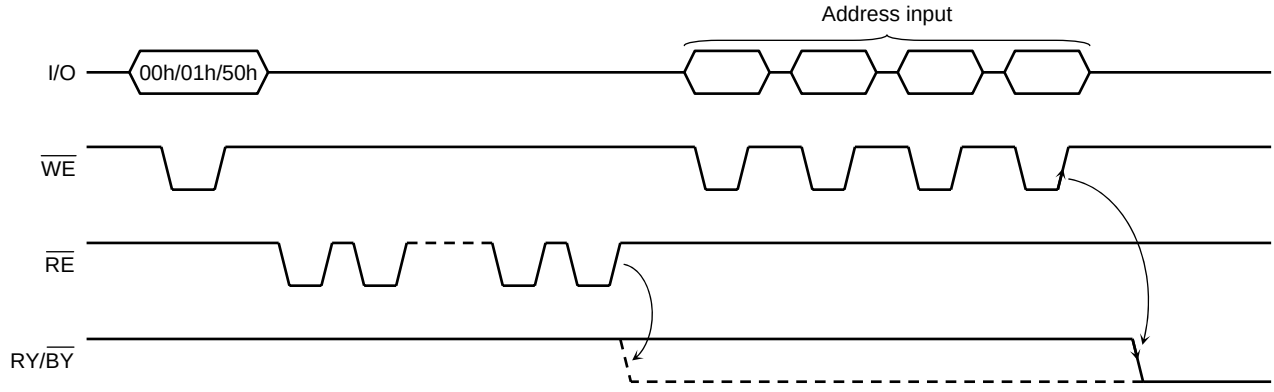


Figure 23.

Hence the $\overline{RE}$ clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

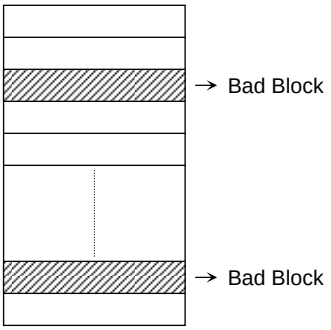


Figure 24

At the time of shipment, all data bytes in a Valid Block are FFh. For Bad Block, all bytes are not in the FFh state. Please don't perform erase operation to Bad Block.

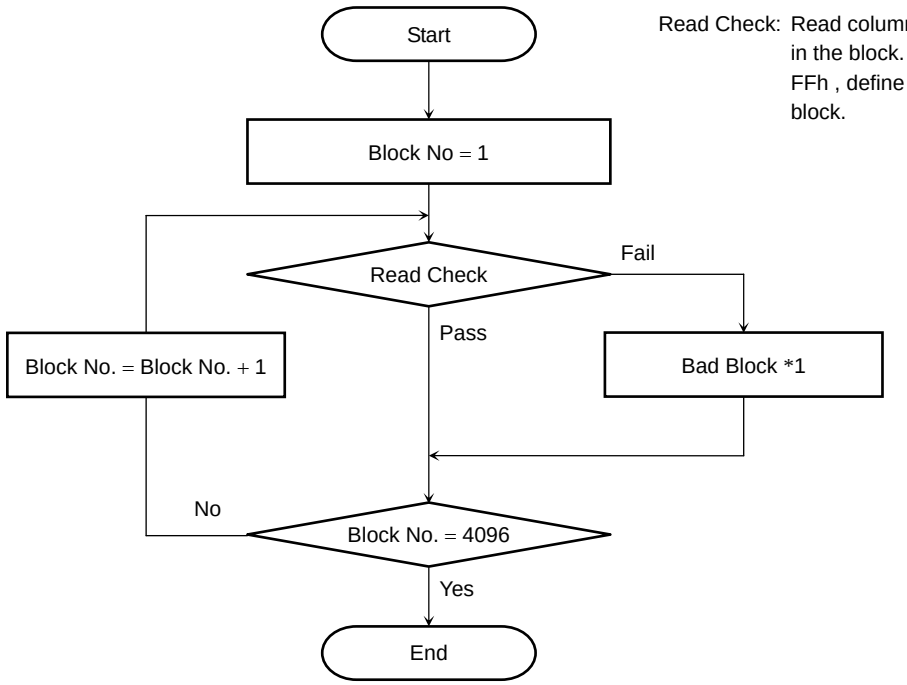
Check if the device has any bad blocks after installation into the system. Figure 25 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	4016	—	4096	Block

Bad Block Test Flow



Read Check: Read column 517 of the 1st page in the block. If the column is not FFh , define the block as a bad block.

*1: No erase operation is allowed to detected bad blocks

Figure 25

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	ECC

- ECC: Error Correction Code. 1 bit correction per 512 Bytes is necessary.
- Block Replacement

Program

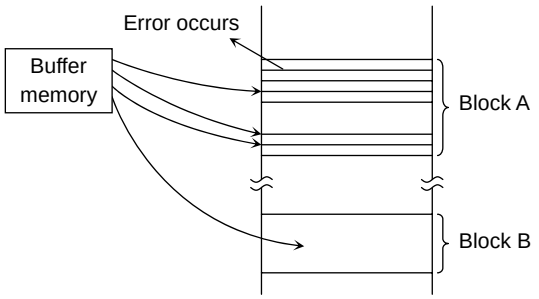


Figure 26.

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(17) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using NAND flash with 1 bit ECC for each 512 bytes. For detailed reliability data, please refer to TOSHIBA's reliability note. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

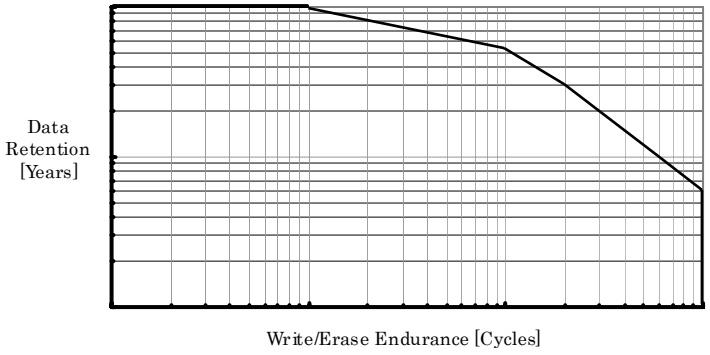
- **Write/Erase Endurance**

  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- **Data Retention**

  The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

  Here is the combined characteristics image of Write/Erase Endurance and Data Retention.

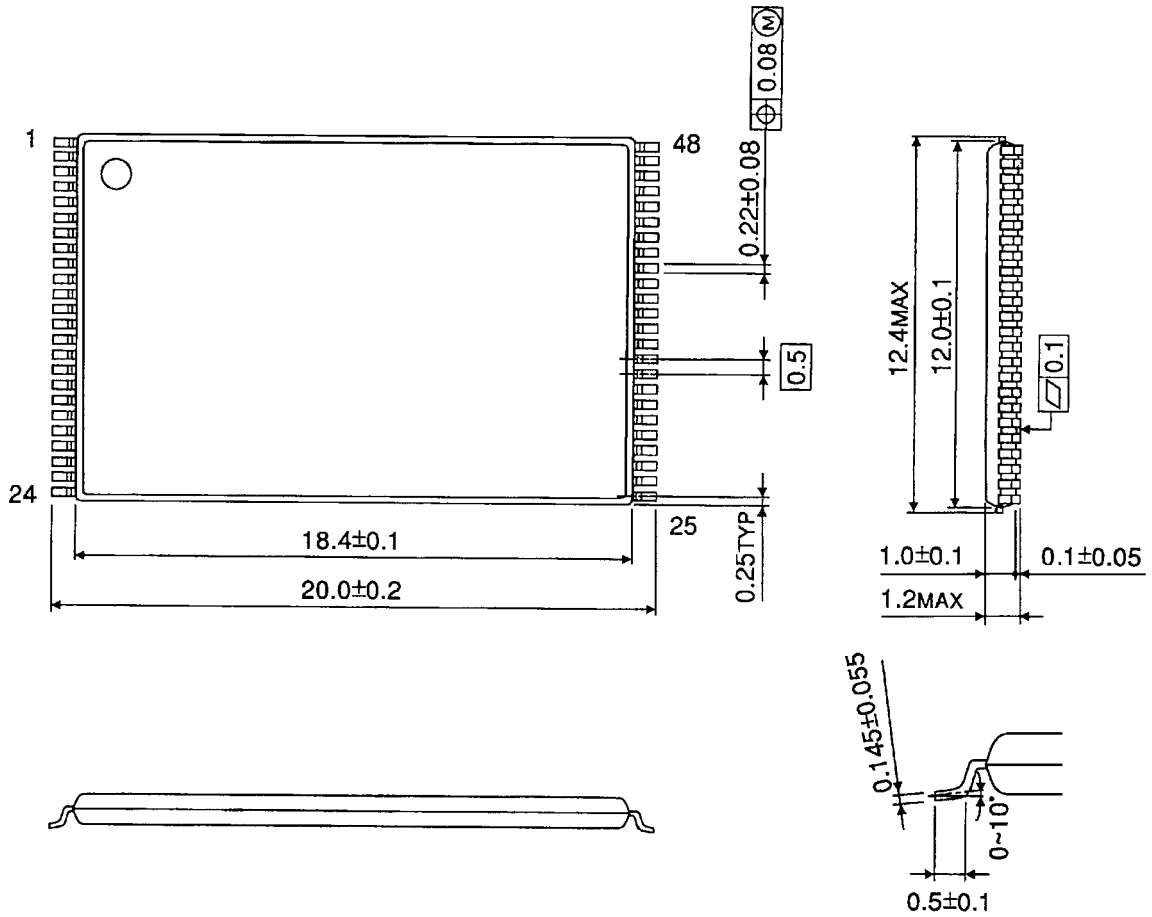


- **Read Disturb**

  A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Package Dimensions

TSOP I 48-P-1220-0.50 Unit : mm



Weight: 0.53 g (typ.)

Revision History

Date	Rev.	Description
2009-11-24	1.00	Original version
2010-04-23	1.01	Described ECC as 1 bit correction per 512 Bytes.
2010-07-13	1.02	Deleted TENTATIVE notation.

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