

TOSHIBA
NAND memory
Toggle DDR1.0
Technical Data Sheet

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Semiconductor & Storage Products

Memory Division

1. INTRODUCTION

1.1. General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.

Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.

Toggle DDR1.0 NAND supports the interface speed of up to 100 MHz, which is faster than the data transfer rate offered by SDR NAND. Toggle DDR NAND transfers data at high speed using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

This device supports both SDR interface and Toggle DDR interface. When starting, the device is activated in SDR mode. The interface mode can be changed into Toggle DDR interface utilizing specific command issued by the Host.

1.2. Definitions and Abbreviations

SDR

Acronym for single data rate.

DDR

Acronym for double data rate.

Address

The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

Column

The byte location within the page register.

Row

Refer to the block and page to be accessed.

Page

The smallest addressable unit for the Read and the Program operations.

Block

Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Plane

The unit that consists of a number of blocks. There are one or more Planes per LUN.

Page register

Register used to transfer data to and from the Flash Array.

Cache register

Register used to transfer data to and from the Host.

Defect area

The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2

Device

The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)

The minimum unit that can independently execute commands and report status. There are one or more LUNs per \overline{CE} .

Target

An independent NAND Flash component with its own \overline{CE} signal.

SR[x] (Status Read)

SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to section 5.13 for the definition of bit meanings within the status register.

1.3. Features

Organization

Table 1 Product Organization

| Parameter | TC58TEG6DCJ | TH58TEG7DCJ | TH58TEG8DCJ |
|--|-----------------------|-------------------------|-------------------------|
| Part number (T _{OPER} : 0~70°C) | TC58TEG6DCJTA00 | TH58TEG7DCJTA20 | TH58TEG8DCJTA20 |
| Part number (T _{OPER} : -40~85°C) | TC58TEG6DCJTAI0 | TH58TEG7DCJTAK0 | TH58TEG8DCJTAK0 |
| Device capacity | 17664×256×2092×8 bits | 17664×256×2092×8×2 bits | 17664×256×2092×8×4 bits |
| Page size | 17664 Bytes | 17664 Bytes | 17664 Bytes |
| Block size | (4M + 320 K) Bytes | (4M + 320 K) Bytes | (4M + 320 K) Bytes |
| Plane size | 9459990528Bytes | 9459990528 Bytes | 9459990528Bytes |
| Plane per one LUN | 1 Planes | 1 Planes | 1 Planes |
| LUN per one target | 1 LUNs | 1 LUNs | 2LUNs |
| Target per one device | 1 target | 2 targets | 2 targets |
| Number of valid blocks per a device (min) | 2018 | 4036 | 8072 |
| Number of valid blocks per a device (max) | 2092 | 4184 | 8368 |

- **Modes**

- Basic Operation

- Page Read Operation (with Random Data Output), Data Out After Status Read, Sequential Cache Read Operation, Random Cache Read Operation, Page Program Operation (with Random Data Input), Cache Program Operation, Block Erase Operation, Copy-Back Program Operation (with Random Data Input), Set Feature Operation, Get Feature Operation, Read ID Operation, Read Status Operation, Reset Operation, Reset LUN Operation

- Extend Operation

- Page Copy (2) Operation, Device Identification Table Read Operation, Read Status Enhanced Operation, Read LUN #0 Status Operation

- Interleaving Operation

- Interleaving Page Program, Interleaving Page Read, Interleaving Block Erase, Interleaving Read to Page Program, Interleaving Copy-Back Program,

Table 2 Supported Operation Modes

| Operation Mode | TC58TEG6DCJ | TH58TEG7DCJ | TH58TEG8DCJ |
|------------------------|---------------|---------------|-------------|
| Basic Operation | Supported | Supported | Supported |
| Extend Operation | Supported | Supported | Supported |
| Interleaving Operation | Not supported | Not supported | Supported |

NOTE :

Read LUN #1 Status Operation is supported only if the Target has more than 2 LUNs.

- **Mode control**

- Serial input/output
 - Command control

- **Power supply**

- V_{CC} = 2.7 V to 3.6 V

- V_{CCQ} = 2.7 V to 3.6 V / 1.7 V to 1.95V

- **Access time**
 - Cell array to register 100 μ s max (TENTATIVE)
 - 50 μ s typ.
 - Data Transfer rate 100MHz
- **Program/Erase time**
 - Auto Page Program 1700 μ s/page typ.
 - Auto Block Erase 5 ms/block typ.
- **Operating current**
 - Read TBD mA max. (per 1 chip)
 - Program (avg.) TBD mA max. (per 1 chip)
 - Erase (avg.) TBD mA max. (per 1 chip)
 - Standby TBD μ A max. (per 1 chip)
- **Package**
 - (Weight: TBD g typ.)
- **Reliability**
 - Refer to APPLICATION NOTES AND COMMENTS.

1.4. Diagram Legend

Diagrams in the Toggle DDR1.0 datasheet use the following legend:

Command

This legend shows the command data. Refer to the Table 32 for more information about the command data.

Address

 ([C1 C2 R1 R2 R3])

This legend shows the Address data. The addresses are comprised of 2 cycles column address and 3 cycles row address.

- C1: Column address 1
- C2: Column address 2
- R1: Row address 1
- R2: Row address 2
- R3: Row address 3

W-Data

This legend shows Host writing data (data input) to the device.

R-Data

This legend shows Host reading data (data output) from the device.

SR[x]

This legend shows Host reading the status register within a particular LUN.

2. PHYSICAL INTERFACE

2.1. Pin Descriptions

Table 3 Pin Descriptions

| SDR | Toggle DDR1.0 | Pin Function |
|-------------------|-------------------|---|
| DQ[7:0] | DQ[7:0] | DATA INPUTS/OUTPUTS The DQ pins are used to input command, address and data and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled. |
| CLE | CLE | COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the \overline{WE} signal. |
| ALE | ALE | ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of \overline{WE} with ALE high. |
| \overline{CE} | \overline{CE} | CHIP ENABLE The \overline{CE} input is the device selection control. When the device is in the Busy state, \overline{CE} high is ignored, and the device does not return to standby mode in program or erase operation. |
| \overline{RE} | \overline{RE} | READ ENABLE The \overline{RE} input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSR} of rising edge & falling edge of \overline{RE} , which also increments the internal column address counter by each one. |
| \overline{WE} | \overline{WE} | WRITE ENABLE The \overline{WE} input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the \overline{WE} pulse. |
| \overline{WP} | \overline{WP} | WRITE PROTECT The \overline{WP} pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the \overline{WP} pin is active low. |
| R/ \overline{B} | R/ \overline{B} | READY/BUSY OUTPUT The R/ \overline{B} output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. |
| - | DQS | DATA STROBE Output with read data, input with write data. Edge-aligned with read data, centered in write data. |
| Vcc | Vcc | POWER VCC is the power supply for device. |
| VccQ | VccQ | DQ POWER The VccQ is the power supply for input and/or output signals. |
| Vss | Vss | GROUND |
| VssQ | VssQ | DQ GROUND The VssQ is the power supply ground |
| NC | NC | No connection NCs are not internally connected. They can be driven or left unconnected. |
| NU | NU | Not use Nus must be left unconnected. |

NOTE:

- 1) Connect all Vcc and Vss pins of each device to common power supply outputs.
- 2) Do not leave all Vcc, VccQ, Vss and VssQ disconnected.

2.2. PIN ASSIGNMENT (TOP VIEW)

Tx58TEGxDCJ

| SDR only | SDR/Toggle DDR1.0 | | | | SDR/Toggle DDR1.0 | SDR only |
|----------|----------------------|---|----|---|----------------------|----------|
| Vcc | Vcc | □ | 1 | ○ | 48 | □ Vss |
| Vss | Vss | □ | 2 | | 47 | □ NC |
| NC | NC | □ | 3 | | 46 | □ VssQ |
| NC | NC | □ | 4 | | 45 | □ VccQ |
| NC | NC | □ | 5 | | 44 | □ DQ7 |
| RY/BY 1 | RY/BY 1 | □ | 6 | | 43 | □ DQ6 |
| RY/BY 0 | RY/BY 0 | □ | 7 | | 42 | □ DQ5 |
| RE | RE | □ | 8 | | 41 | □ DQ4 |
| CE 0 | CE 0 | □ | 9 | | 40 | □ VssQ |
| CE 1 | CE 1 | □ | 10 | | 39 | □ VccQ |
| NC | NC | □ | 11 | | 38 | □ VccQ |
| Vcc | Vcc | □ | 12 | | 37 | □ Vcc |
| Vss | Vss | □ | 13 | | 36 | □ Vss |
| NC | NC | □ | 14 | | 35 | □ DQS |
| NC | NC | □ | 15 | | 34 | □ VccQ |
| CLE | CLE | □ | 16 | | 33 | □ VssQ |
| ALE | ALE | □ | 17 | | 32 | □ DQ3 |
| WE | WE | □ | 18 | | 31 | □ DQ2 |
| WP | WP | □ | 19 | | 30 | □ DQ1 |
| NC | NC | □ | 20 | | 29 | □ DQ0 |
| NC | NC | □ | 21 | | 28 | □ VccQ |
| NC | NC | □ | 22 | | 27 | □ VssQ |
| Vss | Vss | □ | 23 | | 26 | □ NC |
| Vcc | Vcc | □ | 24 | | 25 | □ Vss |

NOTE:

The Pin assignment supports 2CE/2RB.

2.3. BLOCK DIAGRAM

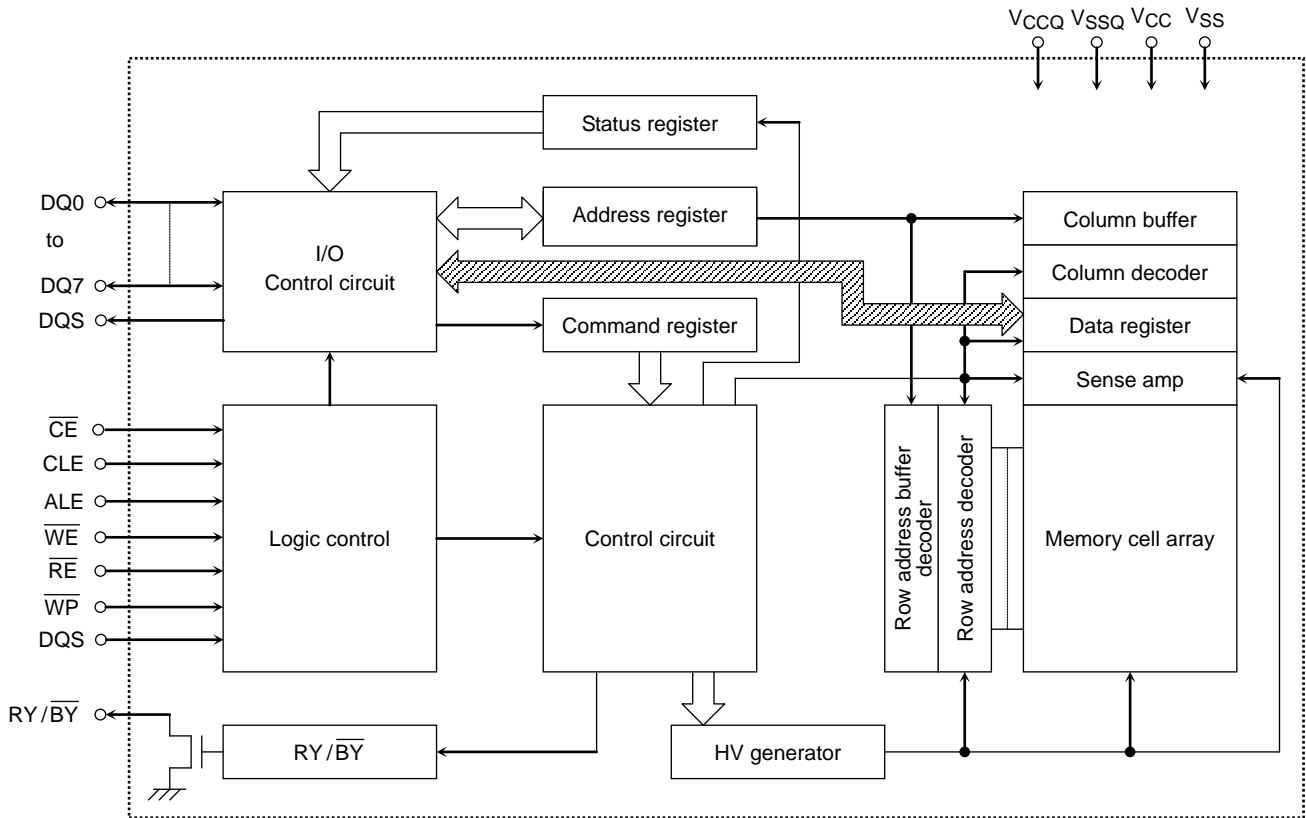


Figure 1. Block Diagram (TC58TEG6DCJ)

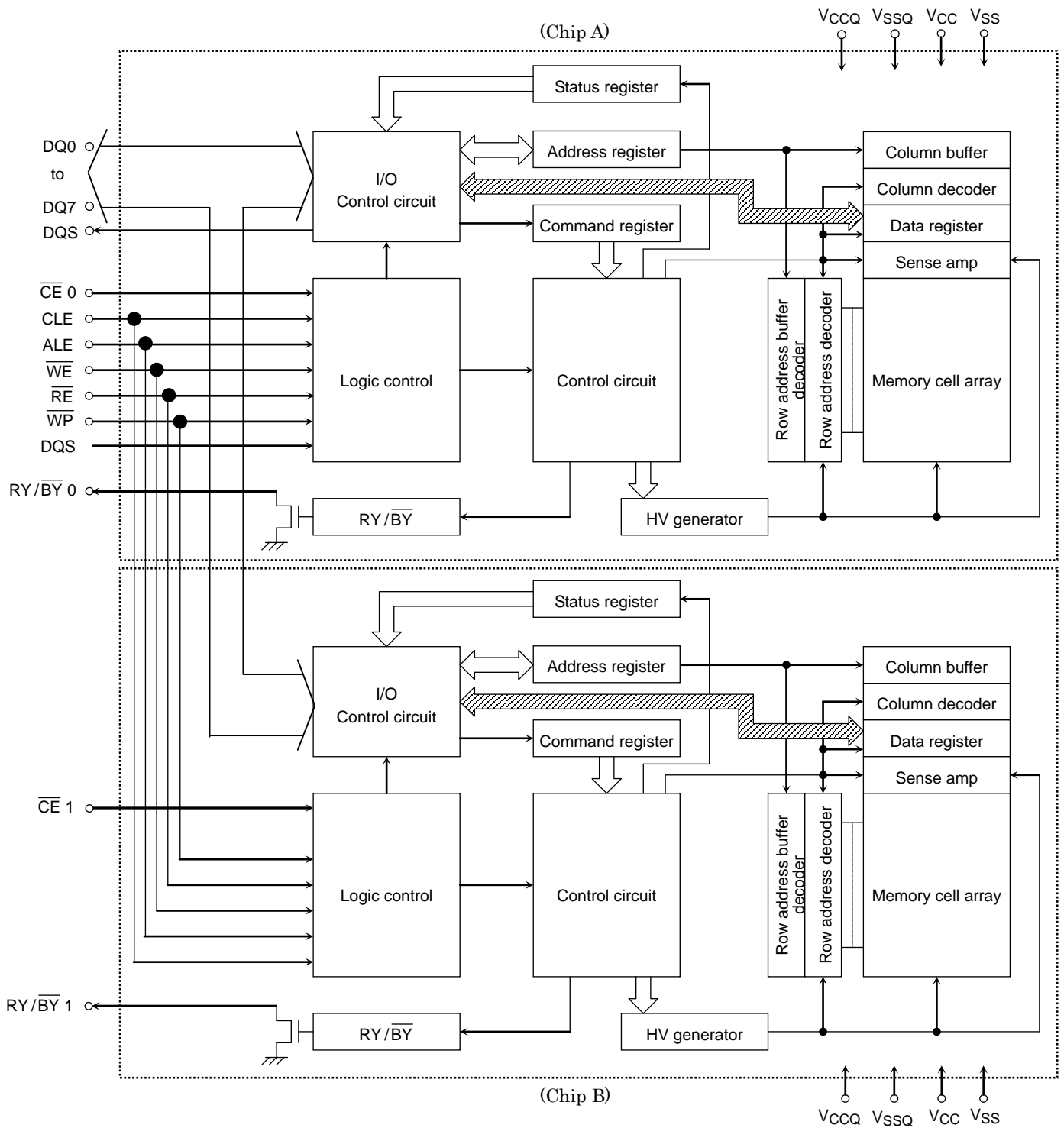


Figure 2. Block Diagram (TH58TEG7DCJ)

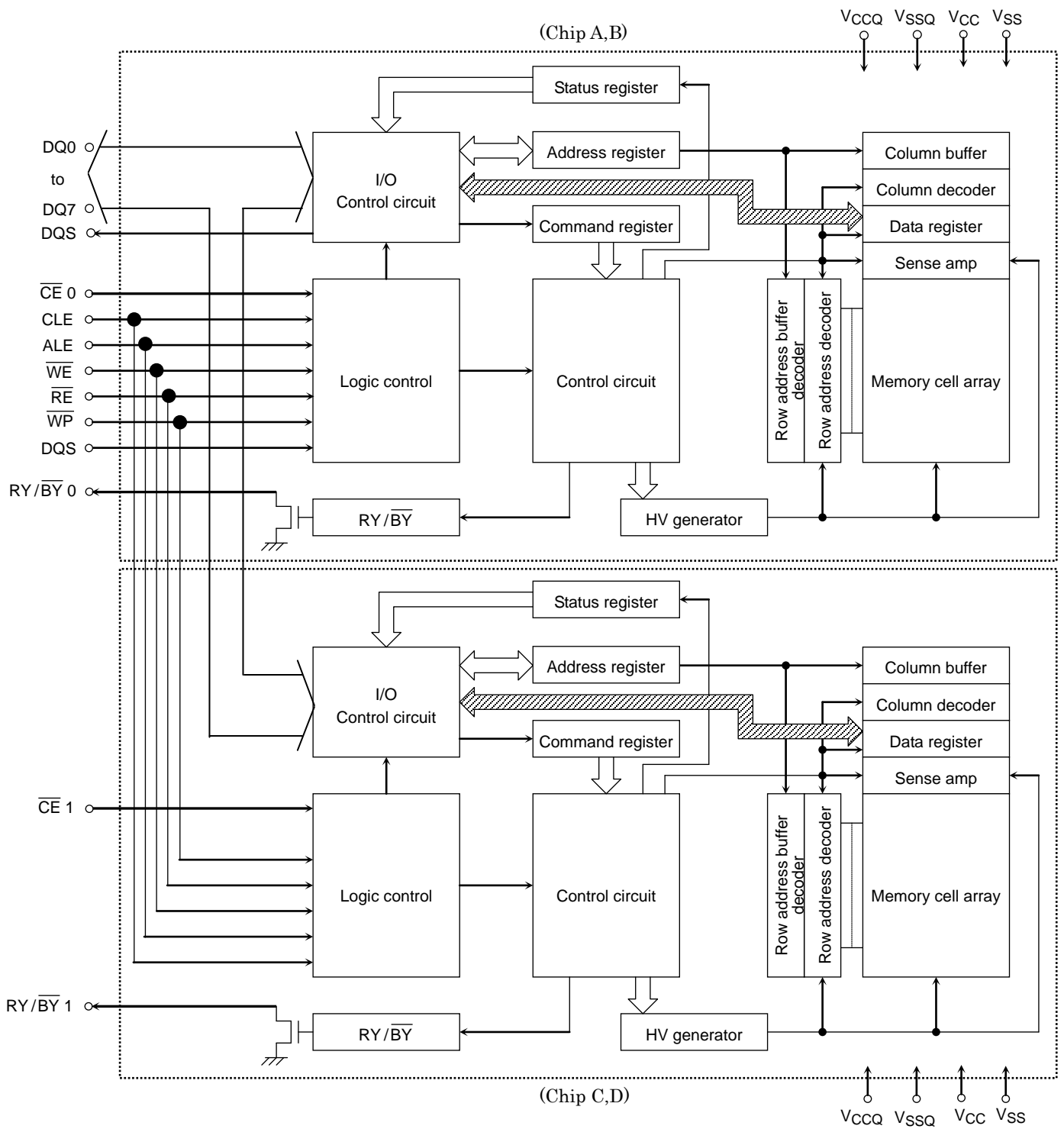


Figure 3. Block Diagram (TH58TEG8DCJ)

2.4. Independent Data Buses

There may be two independent 8-bit data buses in some packages, with two, four or eight \overline{CE} signals. If the device supports two independent data buses, then $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, and $\overline{CE}7$ (if connected) shall use the second data bus. $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, and $\overline{CE}6$ shall always use the first data bus pins. Note that all \overline{CE} s may use the first data bus and the first set of control signals ($\overline{RE}0$, $\overline{CLE}0$, $\overline{ALE}0$, $\overline{WE}0$, and $\overline{WP}0$) if the device does not support independent data buses. Table 4 defines the control signal to \overline{CE} signal mapping when there are two independent x8 data buses.

Table 4 Dual Channel(x8) Data Bus Signal to \overline{CE} mapping

| Signal Name | CE |
|--------------------|---|
| R/ $\overline{B}0$ | $\overline{CE}0$, $\overline{CE}4$ |
| R/ $\overline{B}1$ | $\overline{CE}1$, $\overline{CE}5$ |
| R/ $\overline{B}2$ | $\overline{CE}2$, $\overline{CE}6$ |
| R/ $\overline{B}3$ | $\overline{CE}3$, $\overline{CE}7$ |
| $\overline{RE}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{RE}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |
| $\overline{CLE}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{CLE}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |
| $\overline{ALE}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{ALE}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |
| $\overline{WE}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{WE}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |
| $\overline{WP}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{WP}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |
| $\overline{DQS}0$ | $\overline{CE}0$, $\overline{CE}2$, $\overline{CE}4$, $\overline{CE}6$ |
| $\overline{DQS}1$ | $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, $\overline{CE}7$ |

Implementations may tie the data lines and control signals (\overline{RE} , \overline{CLE} , \overline{ALE} , \overline{WE} , \overline{WP} , and \overline{DQS}) together for the two independent 8-bit data buses externally to the device.

2.5. Absolute Maximum DC Rating

Stresses greater than those listing in Table 5 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 6 is not recommended. Extended exposure beyond these conditions may affect device reliability.

Table 5 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit | |
|------------------------------------|--------|--------------|------|--------------|
| Voltage on any pin relative to VSS | VCC | -0.6 to +4.6 | V | |
| | VIN | VccQ(3.3V) | | -0.6 to +4.6 |
| | | VccQ(1.8V) | | -0.2 to +2.4 |
| | VI/O | VccQ(3.3V) | | -0.6 to +4.6 |
| | | VccQ(1.8V) | | -0.2 to +2.4 |

2.6. Operating Temperature Condition

Table 6 Operating Temperature Condition

| Symbol | Parameter | Part Number | Rating | Unit |
|---------------------|--|-----------------|----------|------|
| T _{OPER} | Operating Temperature Range for Commercial | TC58TEG6DCJTA00 | 0~70 | °C |
| | Operating Temperature Range for Industrial | TC58TEG6DCJTAI0 | -40~+85 | |
| | Operating Temperature Range for Commercial | TH58TEG7DCJTA20 | 0~70 | |
| | Operating Temperature Range for Industrial | TH58TEG7DCJTAK0 | -40~+85 | |
| | Operating Temperature Range for Commercial | TH58TEG8DCJTA20 | 0~70 | |
| | Operating Temperature Range for Industrial | TH58TEG8DCJTAK0 | -40~+85 | |
| T _{SOLDER} | Soldering Temperature (10 s) | | 260 | |
| T _{STG} | Storage Temperature | | -55~+150 | |

NOTE:

- 1) Operating Temperature (T_{OPER}) is the case surface temperature on the center/top side of the NAND.
- 2) Operating Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between the range specified in the table under all operating conditions.

2.7. Recommended Operating Conditions

Table 7 Recommended Operating Condition

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---------------------------------------|------------------|-----|------|------|------|
| Supply Voltage | V _{CC} | 2.7 | 3.3 | 3.6 | V |
| Ground Voltage | V _{SS} | 0 | 0 | 0 | V |
| Supply Voltage for 1.8V I/O signaling | V _{ccQ} | 1.7 | 1.8 | 1.95 | V |
| Supply Voltage for 3.3V I/O signaling | V _{ccQ} | 2.7 | 3.3 | 3.6 | V |
| Ground Voltage for I/O signaling | V _{ssQ} | 0 | 0 | 0 | V |

V_{ccQ} and V_{cc} may be distinct and unique voltages. The device shall support one of the following V_{ccQ}/V_{cc} combinations,

$$V_{cc} = 3.3V, V_{ccQ} = 3.3V$$

$$V_{cc} = 3.3V, V_{ccQ} = 1.8V$$

All parameters, timing modes and other characteristics are related to the supported voltage combination.

2.8. Valid Blocks

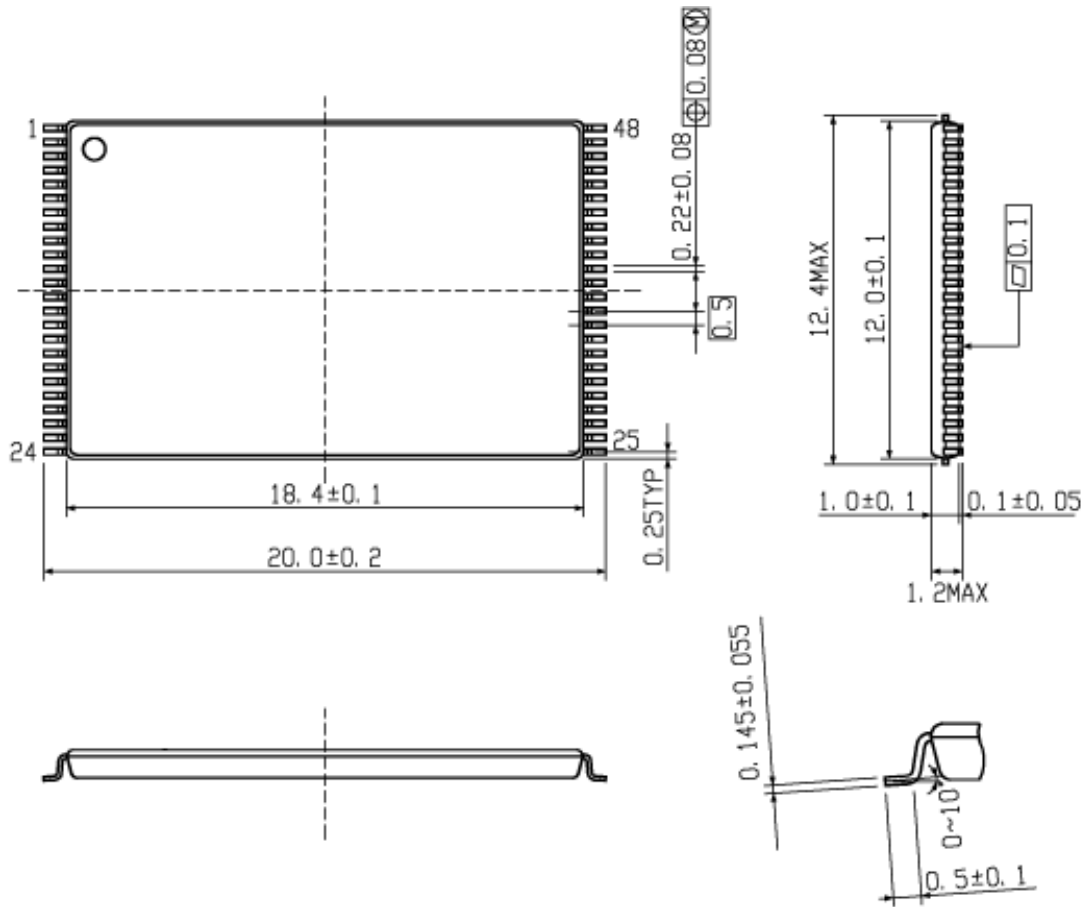
Table 8 Valid Blocks

| Number of Valid Blocks per a device | TC58TEG6DCJ | TH58TEG7DCJ | TH58TEG8DCJ |
|-------------------------------------|-------------|-------------|-------------|
| Min | 2018 | 4036 | 8072 |
| Max | 2092 | 4184 | 8368 |

NOTE:

- 1) The device occasionally contains unusable blocks.
- 2) The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
- 3) The specification for the minimum number of valid blocks is applicable over the device lifetime.
- 4) The number of valid blocks includes extended blocks.

7. Package Dimensions



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