TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

16 Mbit (2 M × 8 bit) CMOS NAND E²PROM (2M BYTE SmartMedia™)

DESCRIPTION

The TC58V16BDC device is a single 3.3 volt 16 M (17,301,504) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 264 bytes × 16 pages × 512 blocks. The device has a 264 byte static register which allows the program and read data to be transferred between the register and the memory cell array in 528 byte increments. The erase operation is implemented in a single block unit (4K bytes + 128 bytes : 264 bytes × 16 pages).

The TC58V16BDC is a serial type of memory device which utilizes the I/O pins for both address and data input / output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for digital still cameras and other systems which require a high-density non-volatile removable memory device.

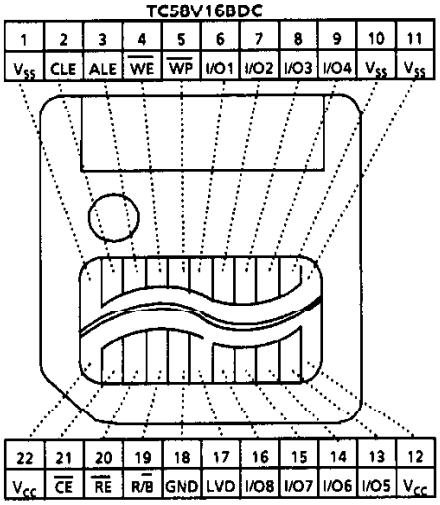
The data stored in the TC58V16BDC needs to comply with the data format standardized by the SSFDC Forum in order to maintain compatibility with other SmartMedia™ systems.

FEATURES

- Organization
  - Memory cell array 264 × 8K × 8
  - Register 264 × 8
  - Page size 264 bytes
  - Block size (4 K + 128) bytes
- Mode
  - Read, Reset, Auto page program
  - Auto block erase, Suspend/Resume, Status read
- Mode control
  - Serial input/output
  - Command control
- Complies with the SmartMedia™ Electrical Specification and Data Format Specification issued by the SSFDC Forum
- Power supply
  - V_{CC} = 3.3 V ± 0.3 V
- Access time
  - Cell array - Register 25 μs max
  - Serial Read Cycle 80 ns min
- Operating current
  - Read (80ns cycle) 15 mA typ
  - Program (ave.) 40 mA typ
  - Erase (ave.) 20 mA typ
  - Standby(CMOS) 100 μA max
- Package
  - TC58V16BDC : FDC - 22A
  - (Weight : 1.8g typ.)

PIN ASSIGNMENT (TOP VIEW)

TC58V16BDC



PIN NAMES

$I/O_{1\ to\ 8}$	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
$R/\overline{B}$	Ready / Busy
GND	Ground Input
LVD	Low Voltage Detect
V_{CC}	Power supply
V_{SS}	Ground

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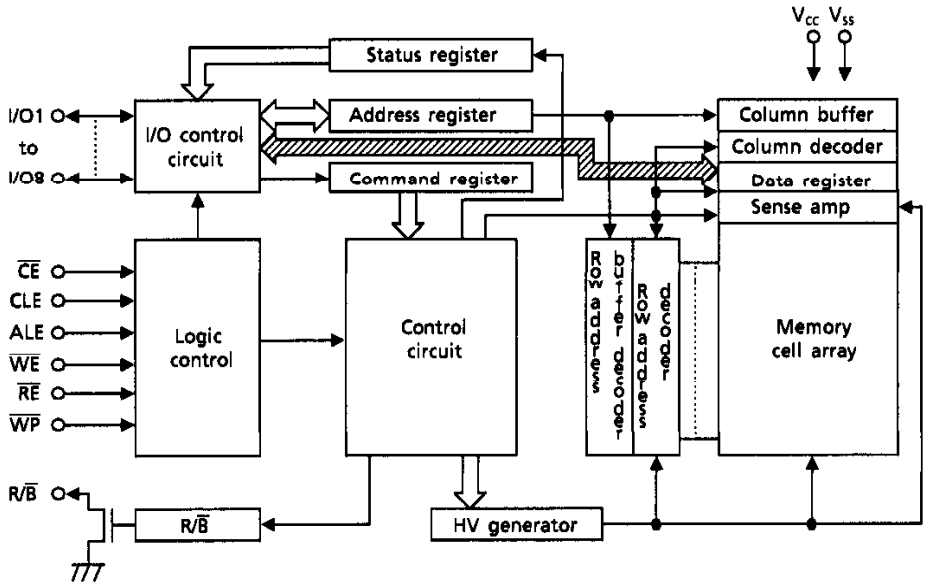
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply	−0.6 to 5.5	V
V_{IN}	Input Voltage	−0.6 to 5.5	V
$V_{I/O}$	Input/Output Voltage	−0.6 V to Vcc + 0.5 V (≤ 5.5 V)	V
P_D	Power Dissipation	0.5	W
T_{STG}	Storage Temperature	−20 to 65	°C
T_{OPR}	Operating Temperature	0 to 55	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	−	5	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	−	5	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS (1)

SYMBOL	PARAMETER	TC58V16			UNIT
		MIN	TYP.	MAX	
N_{VB}	Number of Valid Blocks	502	508	512	Blocks

(1) The TC58V16 occasionally contains unusable blocks. Refer to Application Note 17 toward the end of this document.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	2.0	–	V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage	–0.3*	–	0.8	V

* –2 V (pulse width ≤ 20 ns)

DC CHARACTERISTICS (Ta = 0° to 55°C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 V to V_{CC}	–	–	± 10	μA
I_{CC01}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 80 ns	–	15	30	mA
I_{CC02}	Operating Current (Command Input)	t_{cycle} = 80 ns	–	15	30	mA
I_{CC03}	Operating Current (Data Input)	t_{cycle} = 80 ns	–	40	60	mA
I_{CC04}	Operating Current (Address Input)	t_{cycle} = 80 ns	–	15	30	mA
I_{CC05}	Programming Current	–	–	40	60	mA
I_{CC06}	Erasing Current	–	–	20	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V	–	–	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = –400 μA	2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL}(R/$\overline{B}$)	Output Current of R/$\overline{B}$ Pin	V_{OL} = 0.4 V	–	8	–	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0° to 55°C, V_{CC} = 3.3 V ± 0.3 V) (1)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	20	–	ns	
t_{CLH}	CLE Hold Time	40	–	ns	
t_{CS}	$\overline{CE}$ Setup Time	20	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	40	–	ns	
t_{WP}	Write Pulse Width	40	–	ns	
t_{ALS}	ALE Setup Time	20	–	ns	
t_{ALH}	ALE Hold Time	40	–	ns	
t_{DS}	Data Setup Time	30	–	ns	
t_{DH}	Data Hold Time	20	–	ns	
t_{WC}	Write Cycle Time	80	–	ns	(2)
t_{WH}	$\overline{WE}$-High Hold Time	20	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Falling Edge	100	–	ns	
t_{RR}	Ready-to-$\overline{RE}$ Falling Edge	20	–	ns	
t_{RC}	Read Cycle Time	80	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	45	ns	
t_{CEH}	CE-High Time for Last Address in Serial Read Cycle	250	–	ns	(4)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	–	45	ns	
t_{RHZ}	$\overline{RE}$-High-to-Output-High Impedance	–	30	ns	
t_{CHZ}	$\overline{CE}$-High-to-Output-High Impedance	–	20	ns	
t_{REH}	$\overline{RE}$-High Hold Time	20	–	ns	
t_{IR}	Output-High-Impedance-to-$\overline{RE}$ Rising Edge (Status Read)	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	45	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	55	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low (Status Read)	50	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)	50	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_R	Memory Cell Array to Starting Address	–	25	μs	
t_{WB}	$\overline{WE}$ High to Busy	–	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	150	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	–	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (When interrupted by $\overline{CE}$ in Read Mode)	–	600 + tr ($R/\overline{B}$)	ns	(3)
t_{RST}	Device Reset Time (Read/Program/Erase/after Suspend Command)	–	10/20/500/10	μs	

AC TEST CONDITIONS

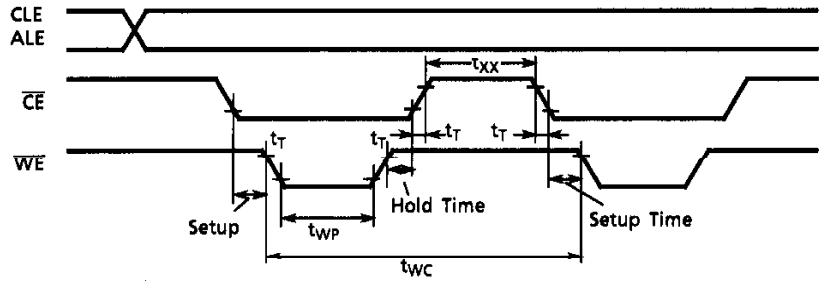
Input level	:	2.4 V / 0.4 V
Input comparison level	:	1.5 V / 1.5 V
Output data comparison level	:	1.5 V / 1.5 V
Output load	:	1 TTL + CL (100 pF)

(1) Transition time (t_T) = 5 ns

(2) When CLE, ALE and $\overline{CE}$ are input on the clock pulse, t_{WC} will exceed 80 ns.

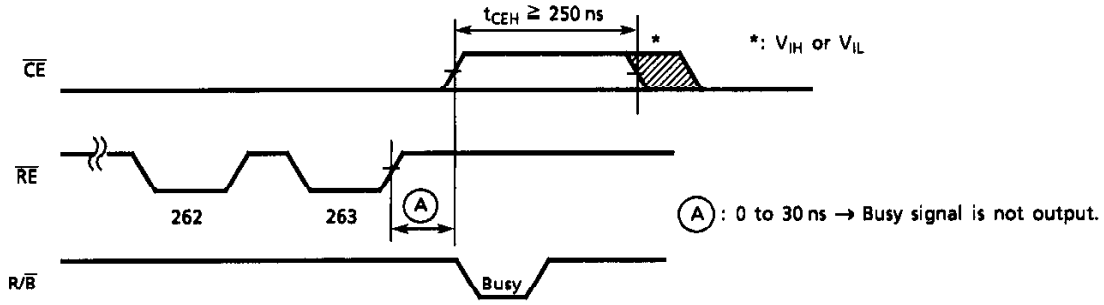
$$\underset{20\text{ ns}}{\underline{\text{Setup Time}}} + \underset{40\text{ ns}}{\underline{\text{Hold Time}}} + \underset{40\text{ ns}}{\underline{t_{WP}}} + \underline{t_{XX}} + \underset{20\text{ ns}}{\underline{4t_T}}$$

(e.g.)



(3) The $\overline{CE}$-High-to-Ready time depends on the pull-up resistor tied to the R/$\overline{B}$ pin. (Refer to Application Note 10 toward the end of this document.)

(4) If the delay between $\overline{RE}$ and $\overline{CE}$ is less than 200 ns and t_{CEH} is greater than or equal to 250 ns, reading will stop.
If the $\overline{RE}$-to-$\overline{CE}$ delay is less than 30 ns. the device will not re-enter Busy state.



PROGRAMMING AND ERASING CHARACTERISTICS (Ta = 0° to 55°C, V_{CC} = 3.3 V ± 0.3 V)

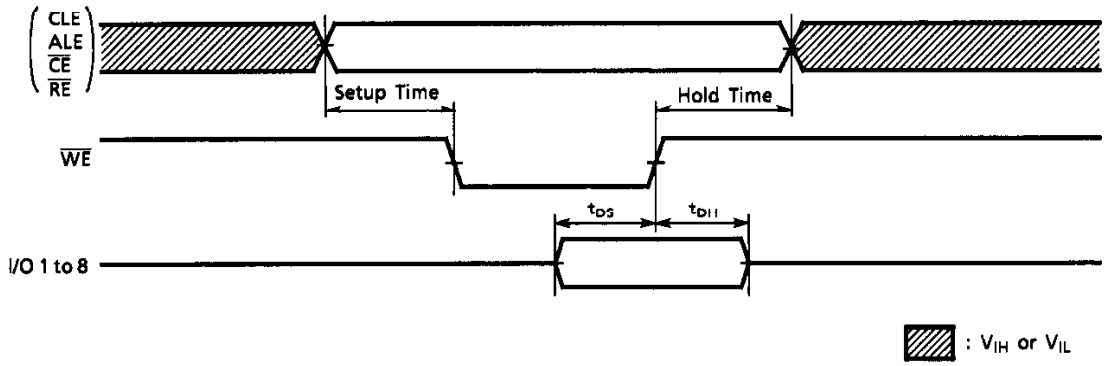
SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time		200 to 500	3000	μs	
N	Number of Programming Cycles on Same Page			10		(1)
t_{BERASE}	Block Erasing Time		4.5	100	ms	
t_{SR}	Suspend Input to Ready			500	μs	
$N_{W/E}$	Number of Write/Erase Cycles			1 x 10^6	Cycles	(2)

(1) Refer to Application Note 15 toward the end of this document.

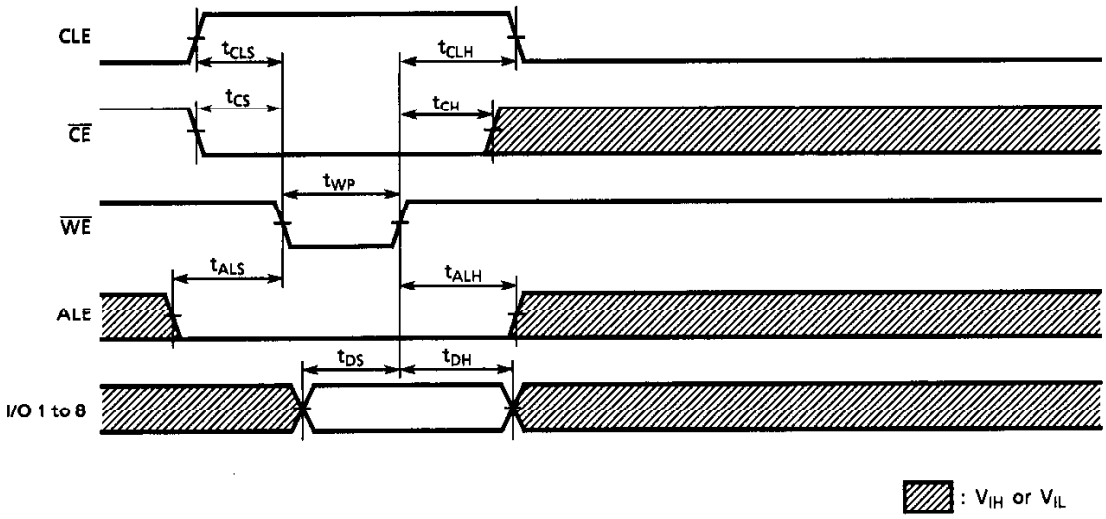
(2) Refer to Application Noto 18 toward the end of this document.

TIMING DIAGRAMS

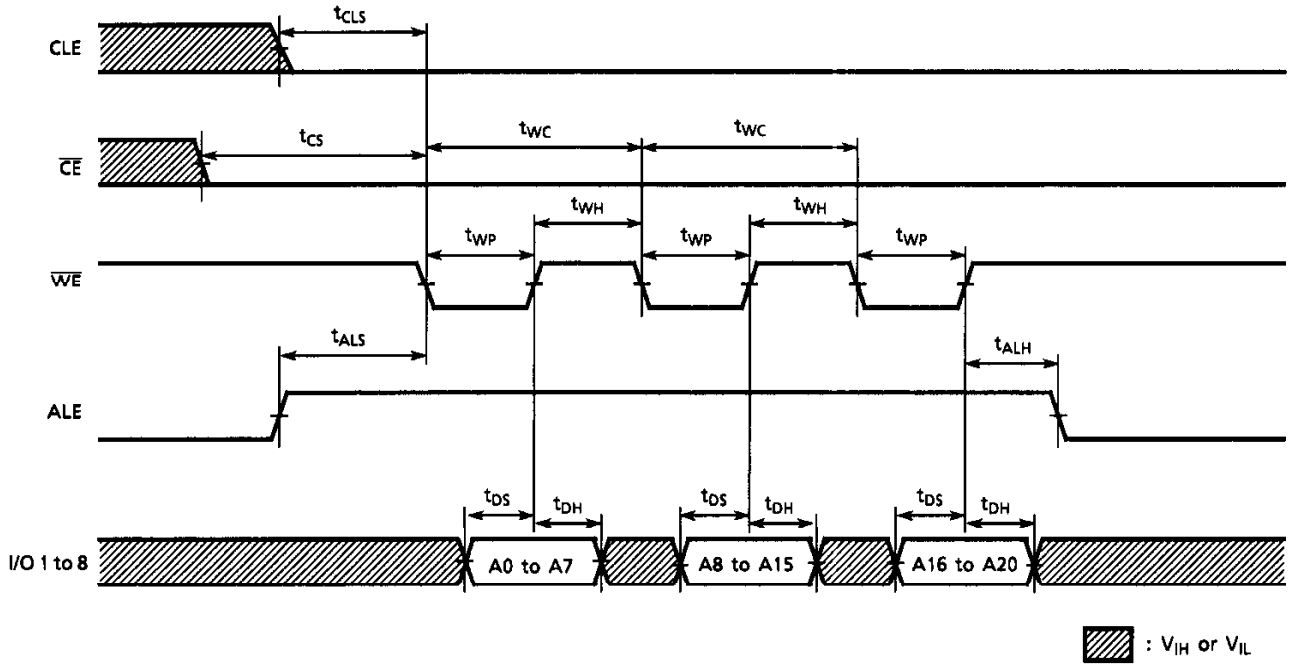
Latch Timing Diagram for Command/Address/Data



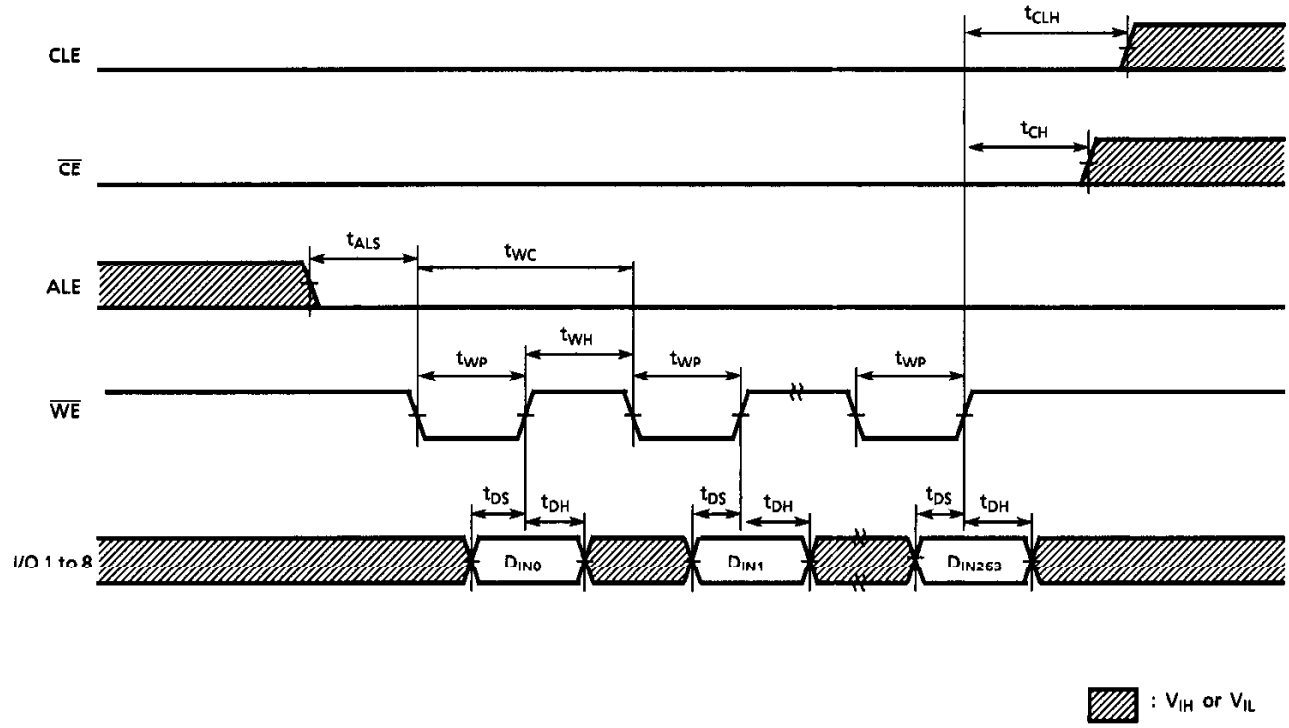
Command Input Cycle Timing Diagram



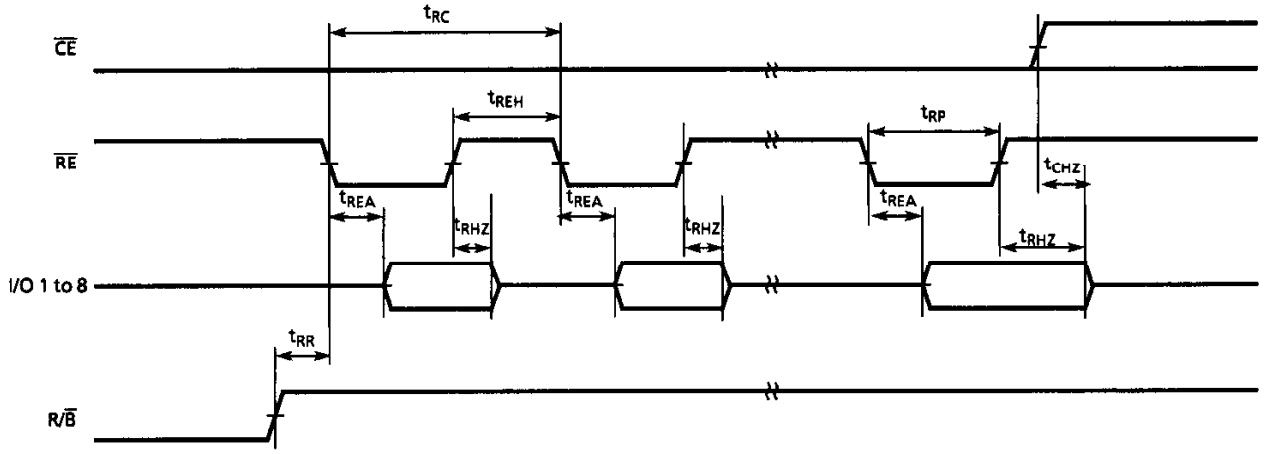
Address Input Cycle Timing Diagram



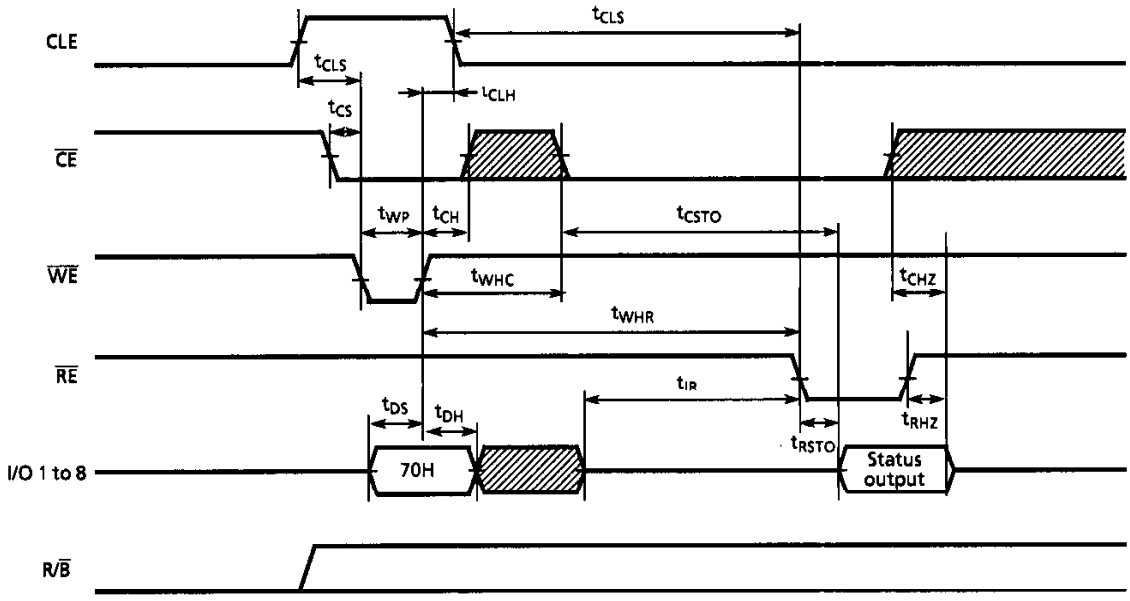
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

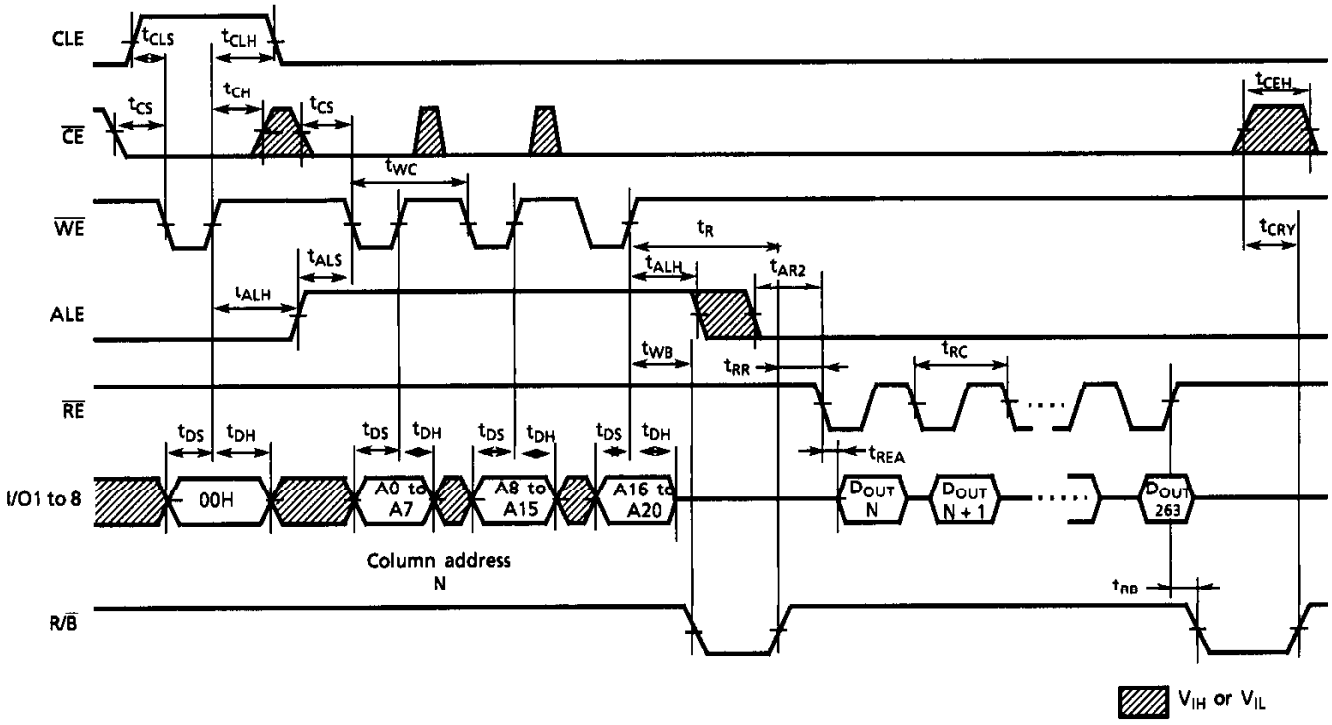


Status Read Cycle Timing Diagram

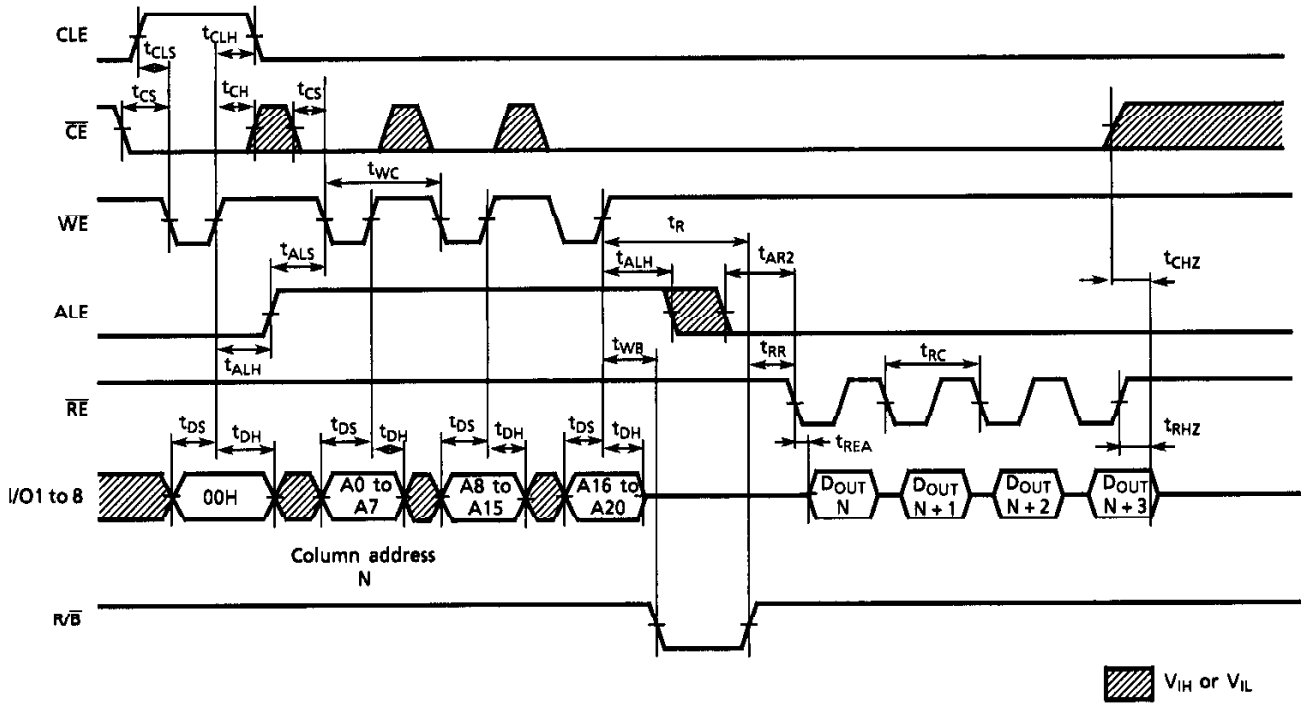


: V_{IH} or V_{IL}

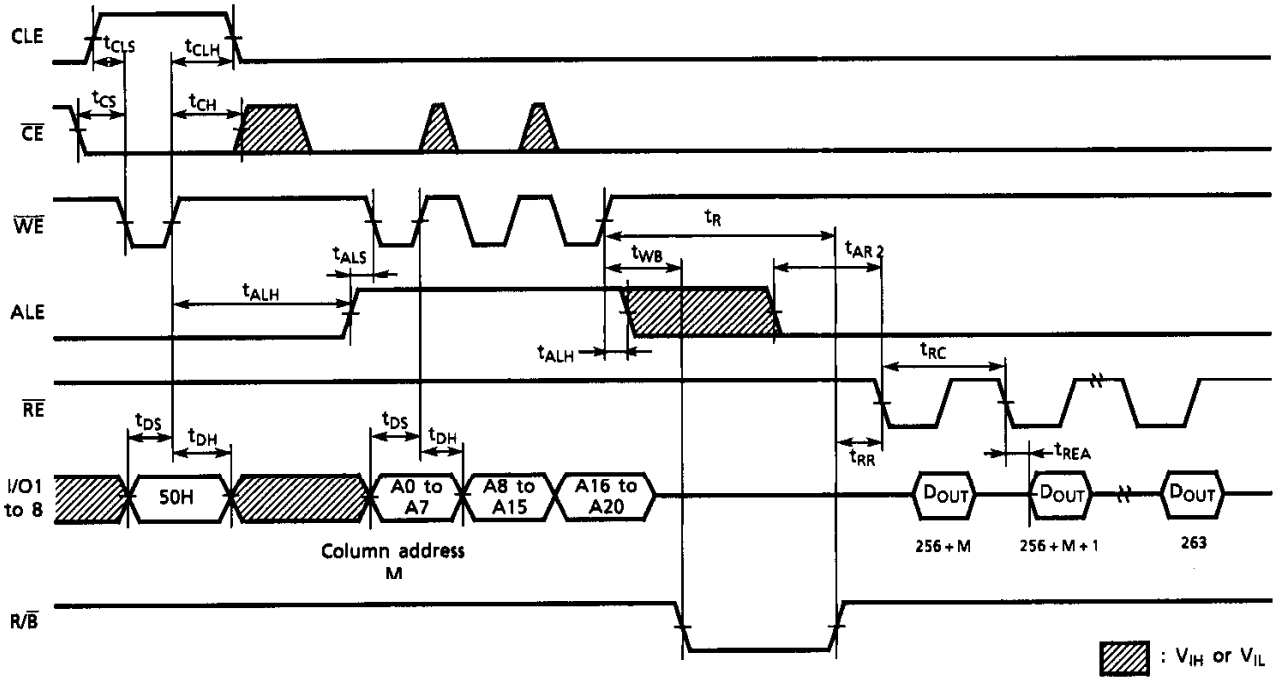
Read Cycle (1) Timing Diagram



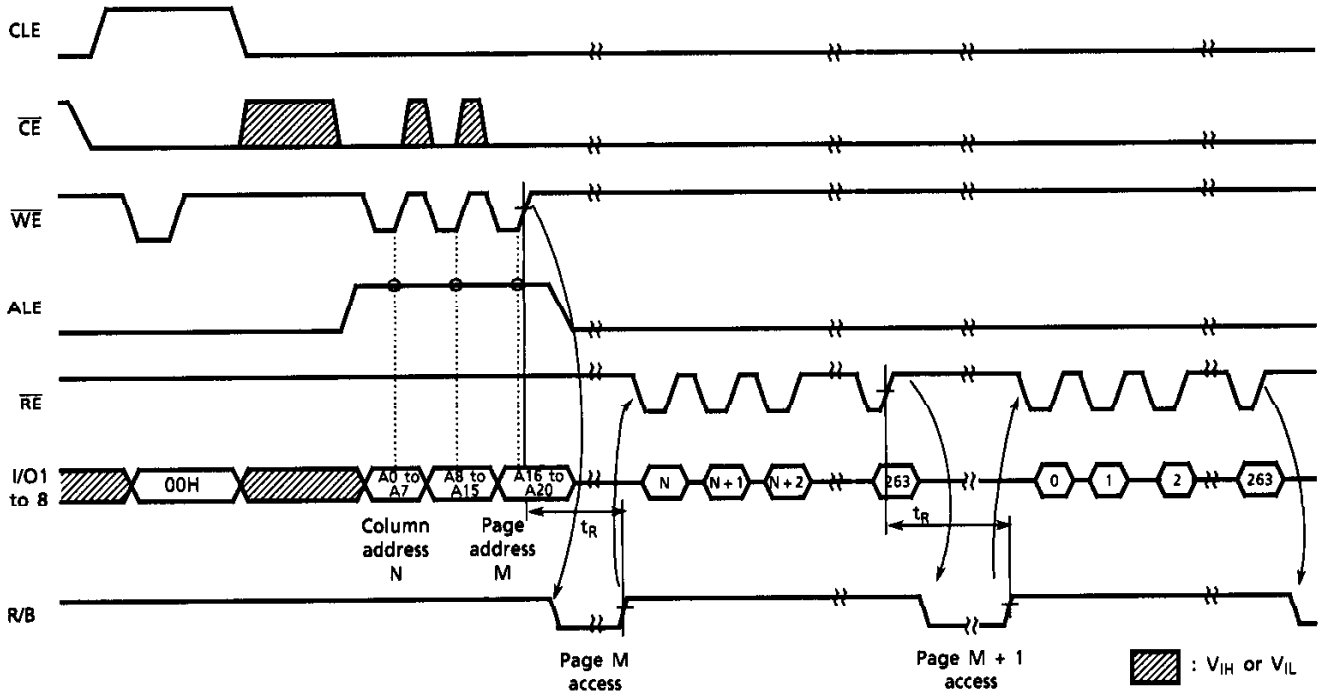
Read Cycle (1) Timing Diagram : Interrupted by $\overline{CE}$



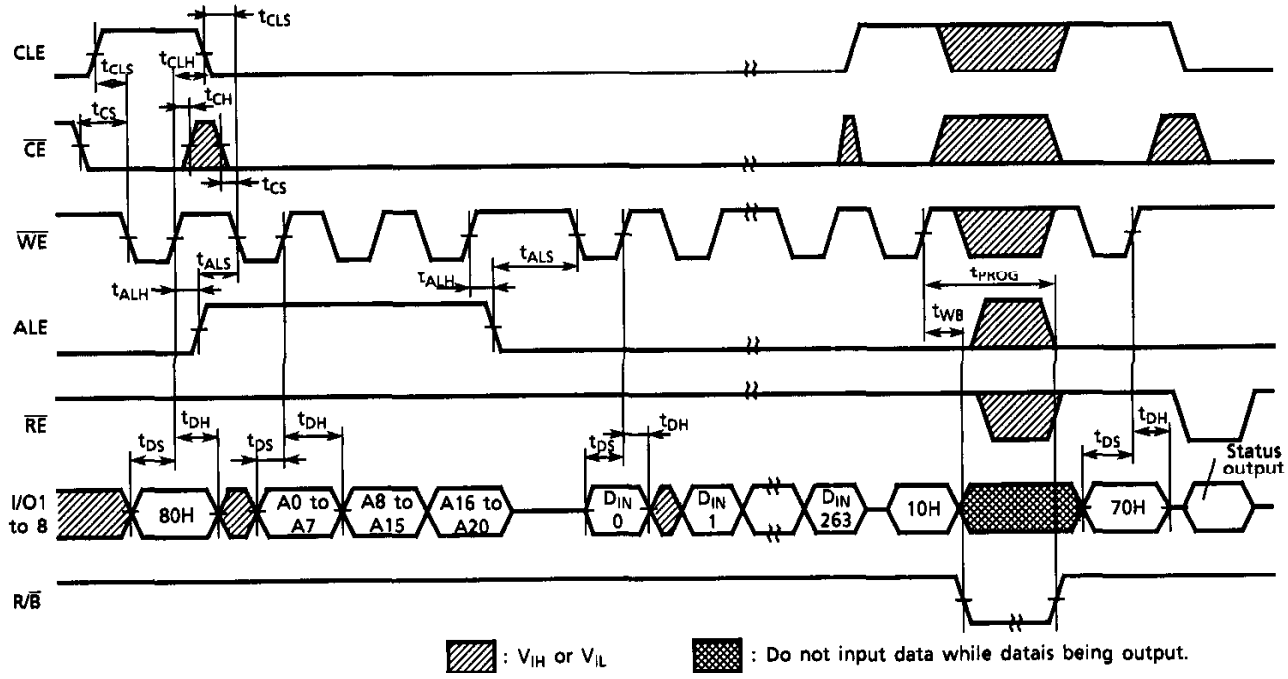
Read Cycle (2) Timing Diagram



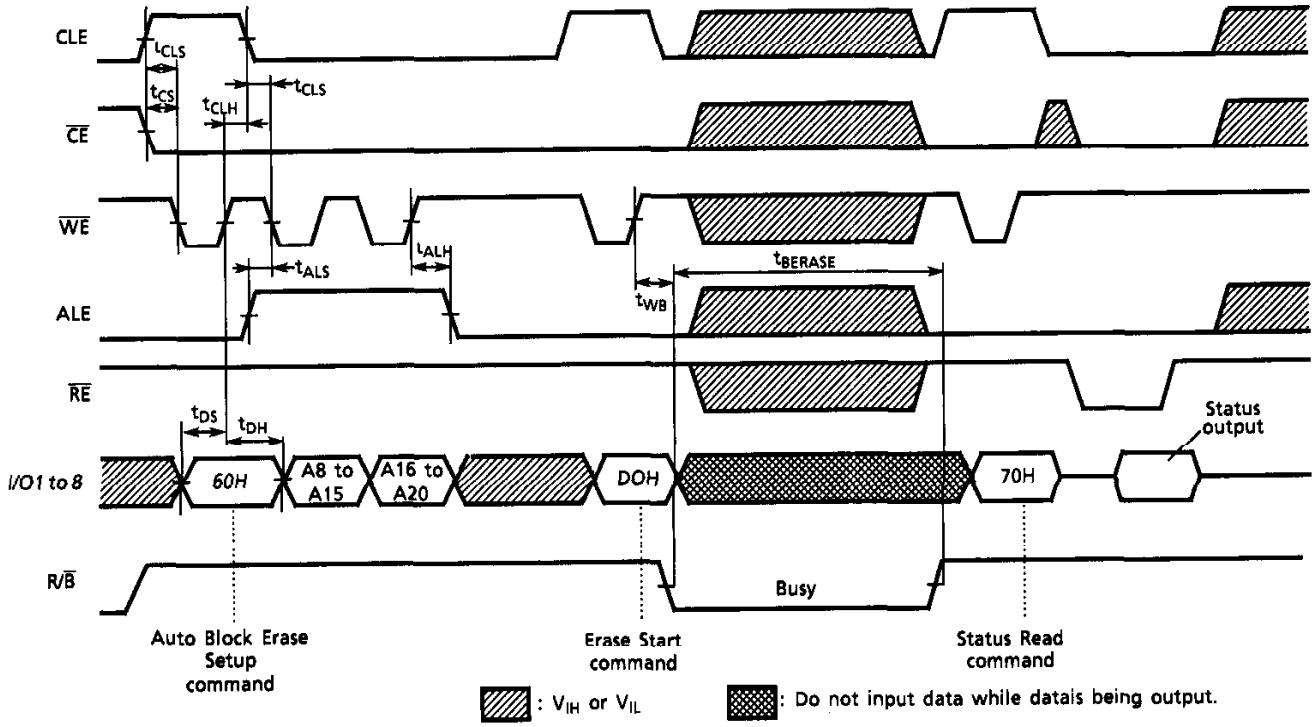
Sequential Read Timing Diagram



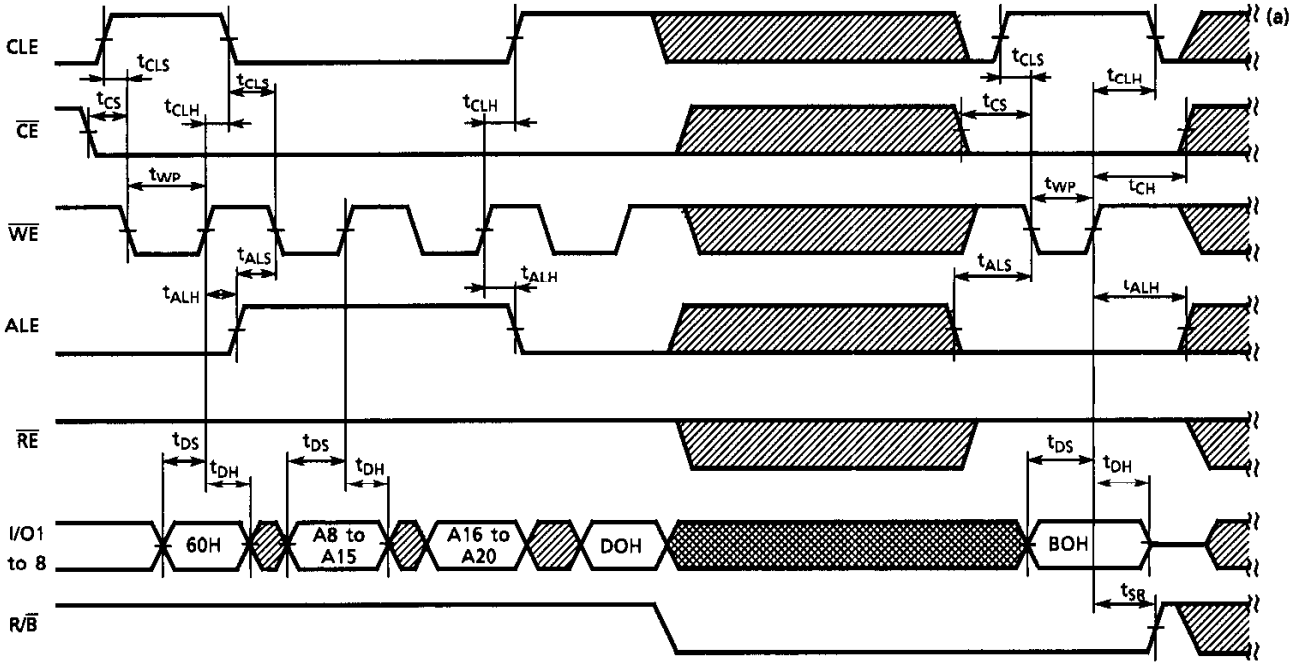
Auto Program Operation Timing Diagram

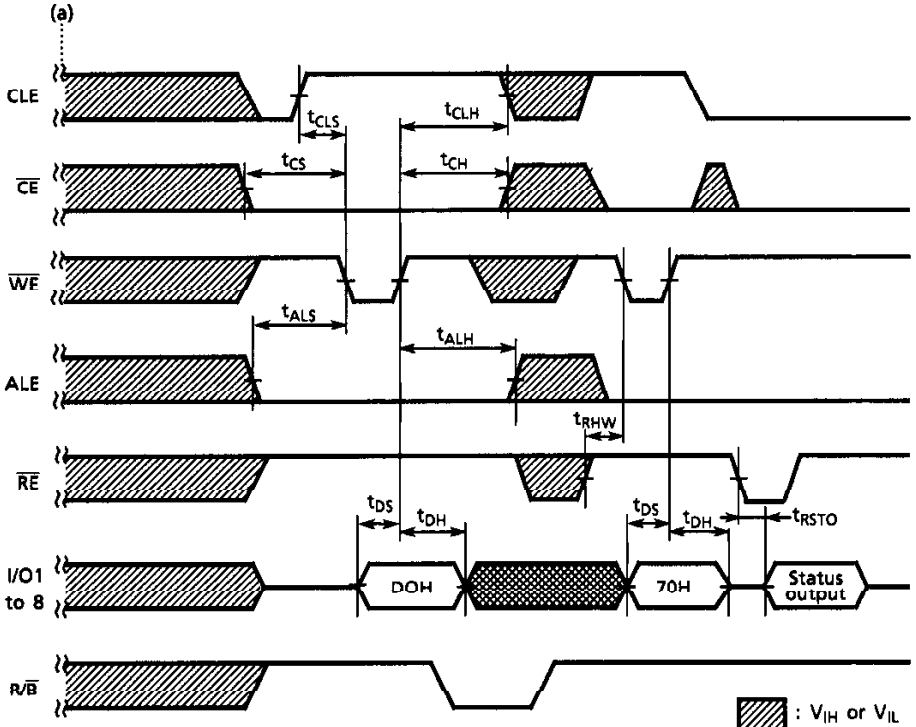


Auto Block Erase Timing Diagram



Suspend/Resume Block Erase Operation Timing Diagram



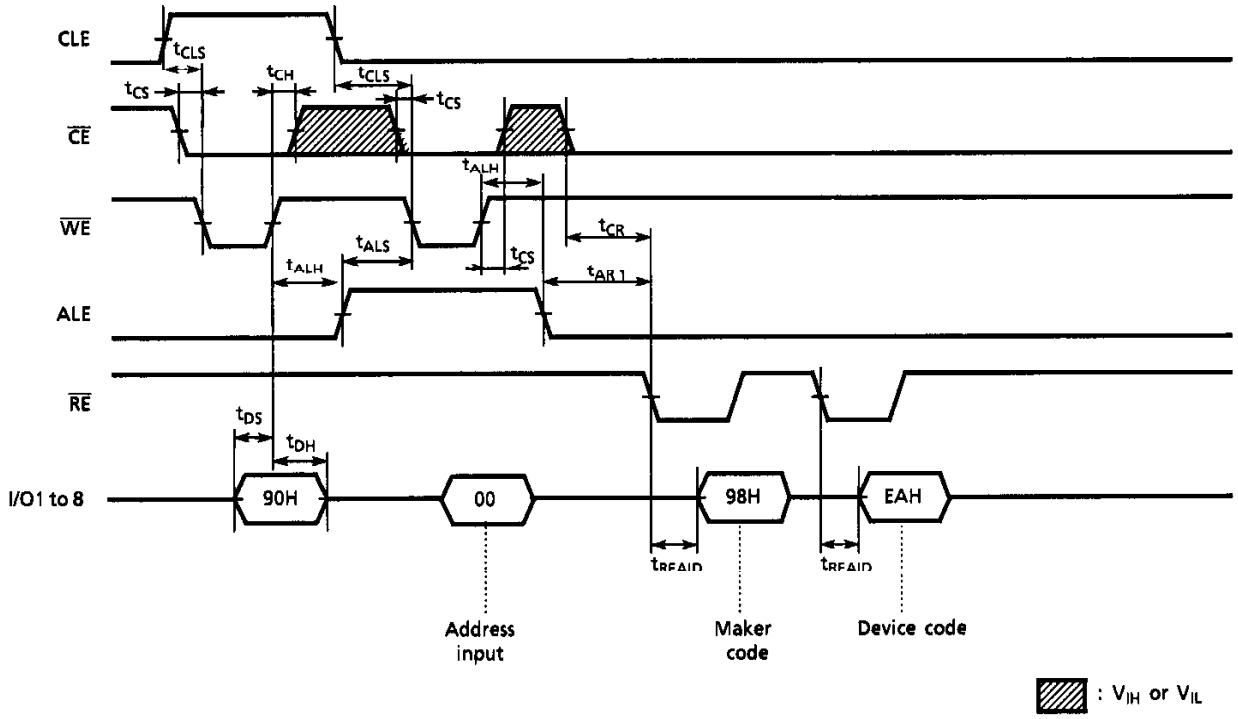


(a): Continued

: V_{IH} or V_{IL}

: Do not input data while data is being output.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The TC58V16 is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE (Figure 1. Pin No. 2)

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

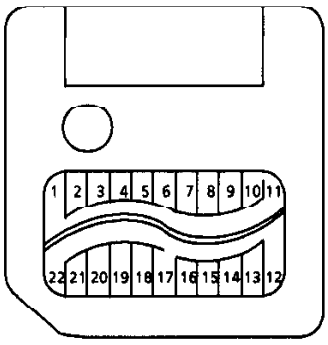


Figure 1. TC58V16 Pinout

Address Latch Enable: ALE (Figure 1. Pin No. 3)

The ALE signal is used to control loading of either address information or input data into the internal address/data register.
Address information is latched on the rising edge of $\overline{WE}$ if ALE is High.
Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$ (Figure 1. Pin No. 21)

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a Read operation. The $\overline{CE}$ signal is ignored when the device is in Busy state ($R/\overline{B}$ = L), such as during a Program or Erase operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$ (Figure 1. Pin No. 4)

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$ (Figure 1. Pin No. 20)

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8 (Figure 1. Pin Nos. 6 to 9 and 13 to 16)

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$ (Figure 1. Pin No. 5)

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $R/\overline{B}$ (Figure 1. Pin No. 19)

The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in Busy state ($R/\overline{B}$ = L) during the Program, Erase and Read operations and will return to Ready state ($R/\overline{B}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Low Voltage Detect: LVD (Figure 1. Pin No. 17)

The LVD pin is used to detect the power supply voltage level. By connecting this pin to V_{SS} via a pull-down resistor, it is possible to distinguish the 3.3-V product (TC58V16BDC) from the 5-V product (TC5816BDC). When a V_{CC} of 3.3 V is applied to pins 12 and 22, an H level can be detected on the system side if the device is a TC58V16BDC, and an L level if it is a TC5816BDC.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

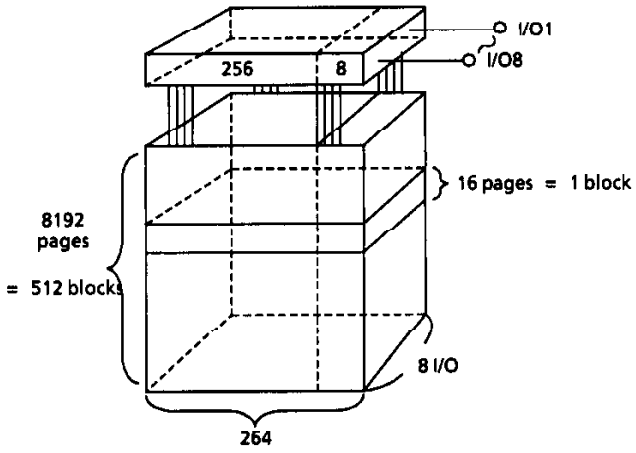


Figure 2. Schematic Cell Layout

A page consists of 264 bytes in which 256 bytes are used for main memory storage and eight bytes are for redundancy or for other uses.

1 page = 264 bytes
1 block = 264 bytes × 16 pages = (4K + 128) bytes
Capacity = 264 bytes × 16 pages × 512 blocks
= 16.5 Mbits (2.0625 Mbytes)

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third cycle	A16	A17	A18	A19	A20	*L	*L	*L

A0 to A7: Column address
A8 to A20: Page address
(A12 to A20: Block address
A8 to A11: NAND address in block)

*: I/O6 to 8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend and Reset are controlled by the eleven different command operations shown in Table 2. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

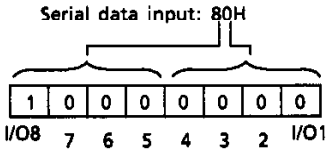
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⌐└↗	H	*
Data Input	L	L	L	⌐└↗	H	*
Address Input	L	H	L	⌐└↗	H	*
Serial Data Output	L	L	L	H	↘└⌐	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

Table 3. Command Table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	–	
Read Mode (1)	00	–	
Read Mode (2)	50	–	
Reset	FF	–	○
Auto-Program	10	–	
Auto Block Erase	60	D0	
Suspend Erasing	B0	–	○
Resume	D0	–	
Status Read	70	–	○
ID Read	90	–	

HEX data bit assignment
(Example)



Once the device has been set to Read mode by a 00H or 50H command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output Select	H	H	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.

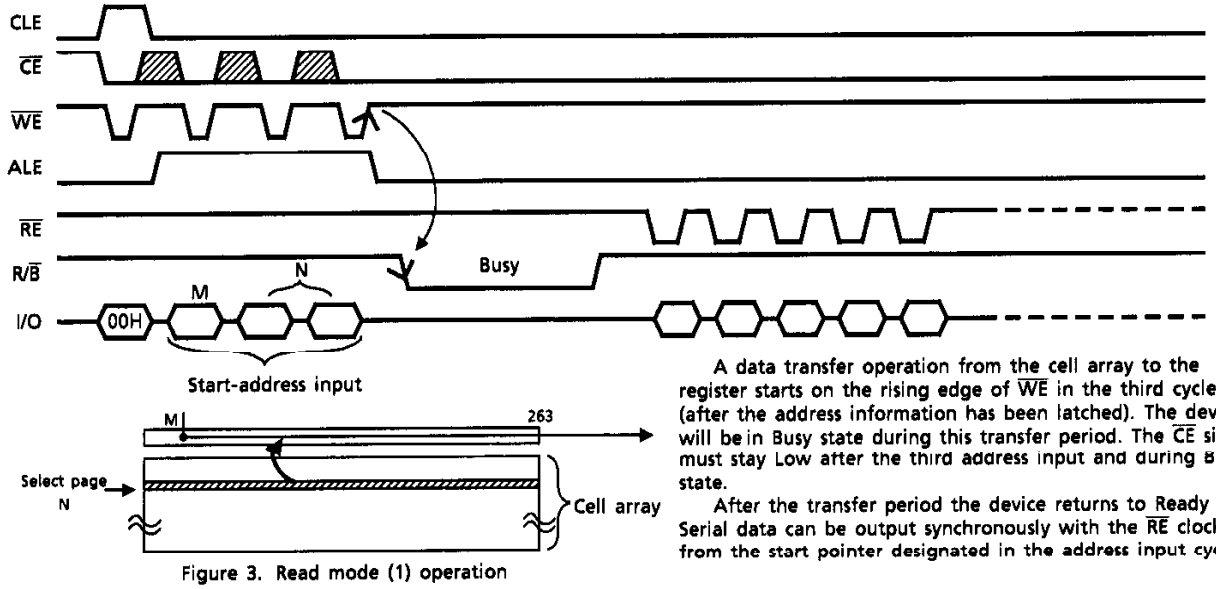


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)

Read mode (2) has the same timing as Read mode (1) but is used to access information in the extra 8-byte redundancy area of the page. The start pointer is therefore set to a value between byte 256 and byte 263.

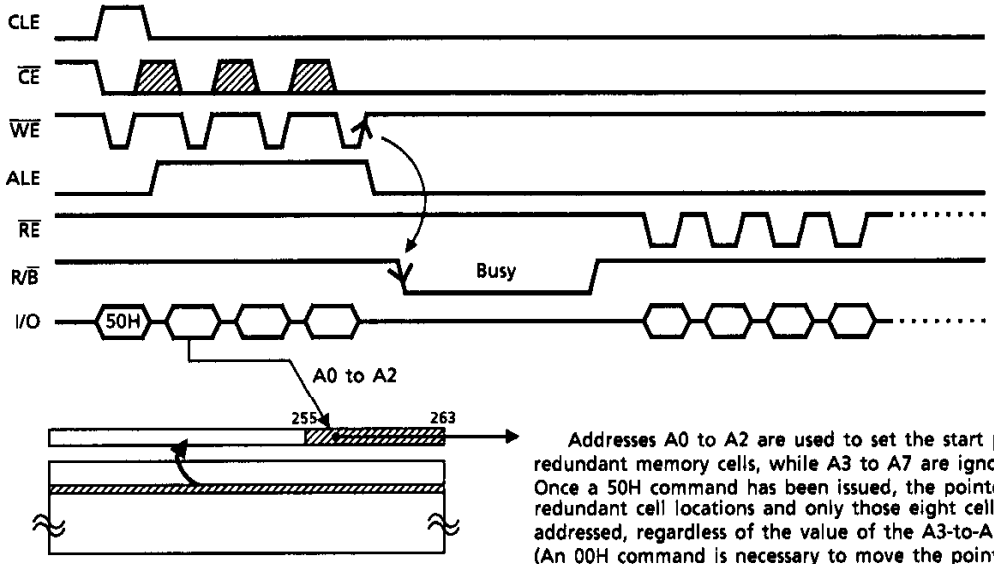


Figure 4. Output Select (2) operation

Addresses A0 to A2 are used to set the start pointer for the redundant memory cells, while A3 to A7 are ignored.
Once a 50H command has been issued, the pointer moves to the redundant cell locations and only those eight cells can be addressed, regardless of the value of the A3-to-A7 address.
(An 00H command is necessary to move the pointer back to the 0-to-255 main memory cell location.)

Sequential Read (1) (2)

This mode allows sequential reading without the additional address input.

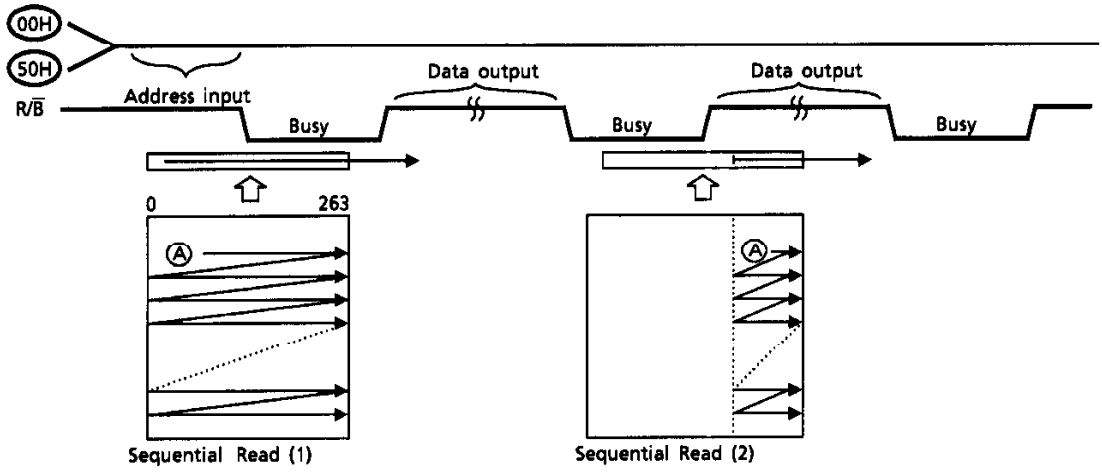


Figure 5. Sequential Read operation

Sequential Read mode (1) outputs the contents of addresses 0 to 263 while Sequential Read mode (2) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address on each $\overline{RE}$ clock signal.

Status Read

The TC58V16 automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Suspend or Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT
I/O1	Pass/Fail	Pass: 0 Fail: 1
I/O2	Not Used	0
I/O3	Not Used	0
I/O4	Not Used	0
I/O5	Not Used	0
I/O6	Suspend	Suspended: 1 Not Suspended: 0
I/O7	Ready/Busy	Ready: 1 Busy: 0
I/O8	Write Protect	Protect: 0 Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.
The device will always indicate Fail status while in Busy state during the Program and Erase operations.

An application example with multiple devices is shown in Figure 6.

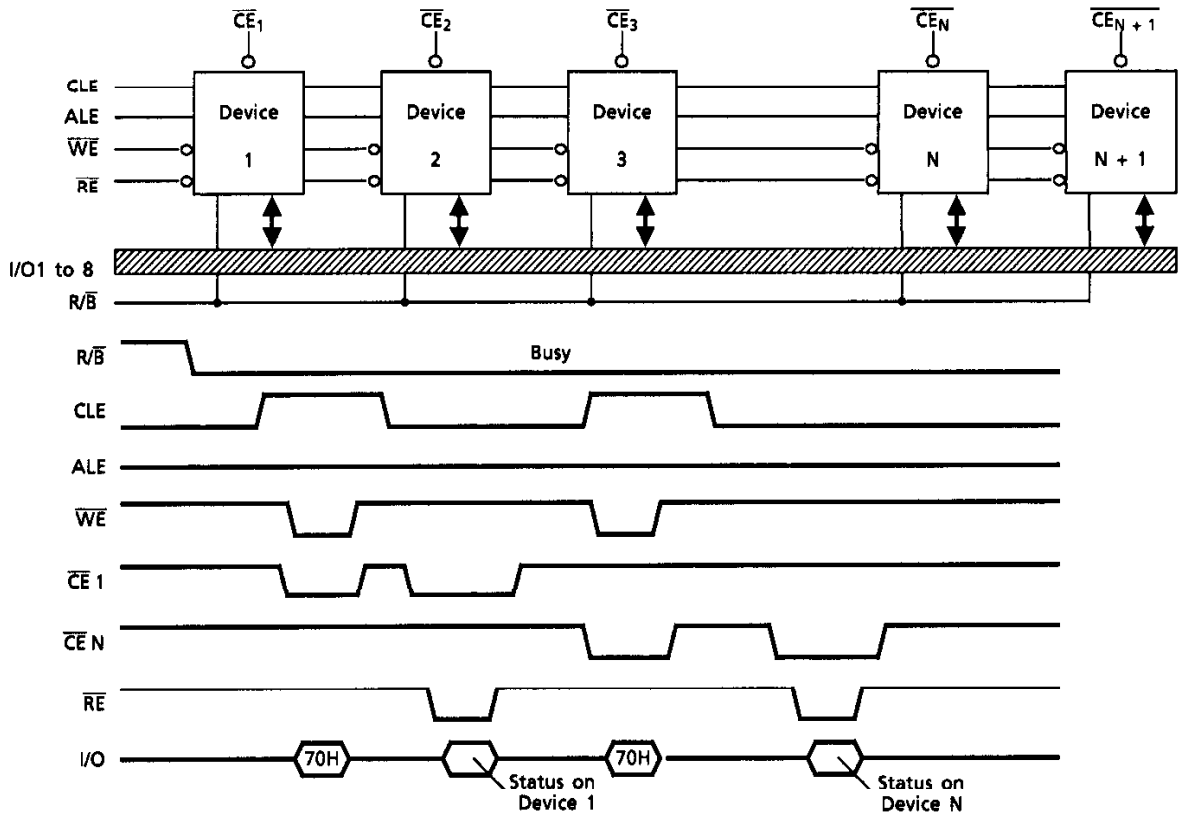
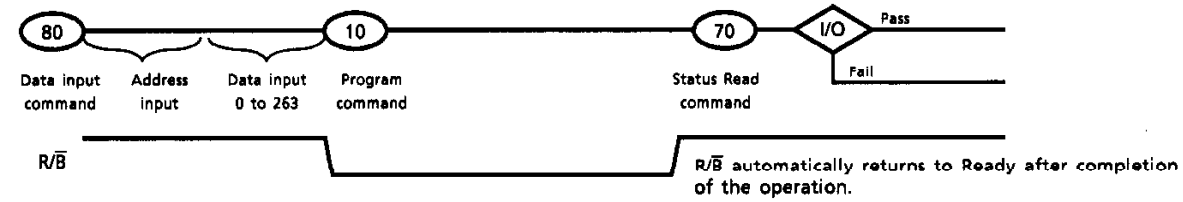


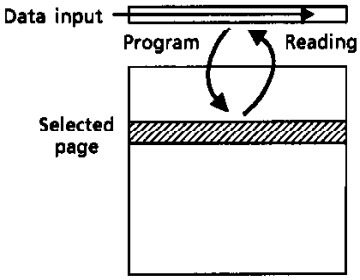
Figure 6. Status Read timing application example

System Design Note: If the R/$\overline{B}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The TC58V16 carries out an Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)





The data is transferred (programmed) from the register to the selected page on the rising edge of WE following input of the 10H command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command D0H which follows the Erase Setup command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

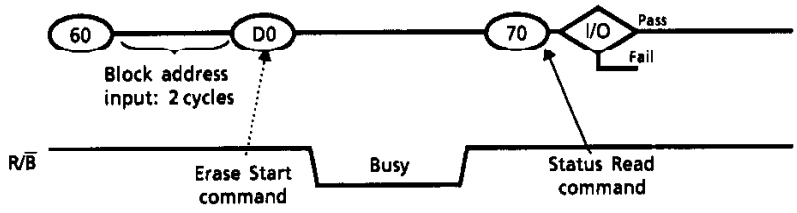


Figure 8. Auto Block Erase

Suspend / Resume

Because a Block Erase operation can keep the device in the Busy state for an extended period of time, the TC58V16 has the ability to suspend the Erase operation in order to allow Program or Read operations to be performed on the device. The block diagram and command sequence for this operation are shown below. (Refer to the detailed timing chart.)

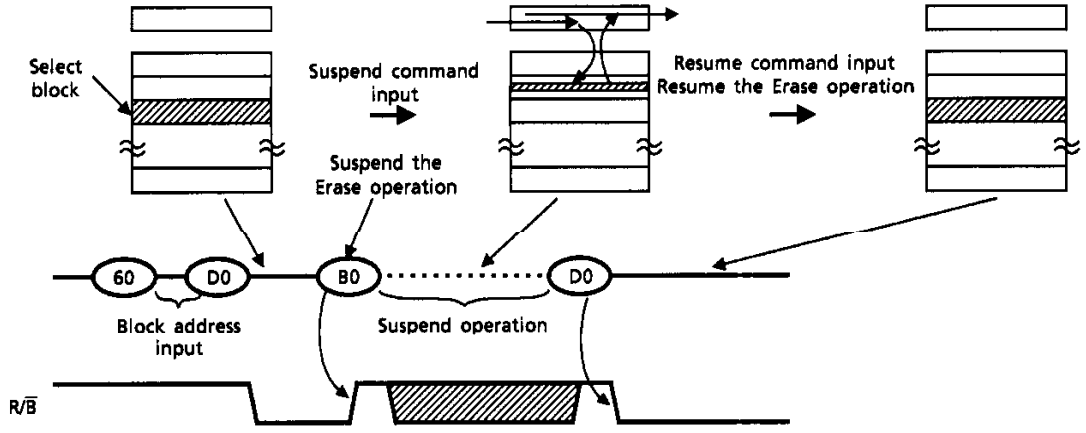


Figure 9. Suspend/Resume operation

The B0 ···· D0 Suspend/Resume cycle can be repeated up to 20 times during a Block Erase operation. When the Resume command is input, the Erase operation automatically continues from the point at which it left off.

Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation, the internally generated voltage is discharged to 0 V and the device enters Wait state.
The address and data register are set as follows after a Reset:

- Address Register: All 0s
- Data Register: All 1s
- Operation Mode: Wait state

The response to an FFH Reset command input during the various device operations is as follows:

- When a Reset (FFH) command is input during programming

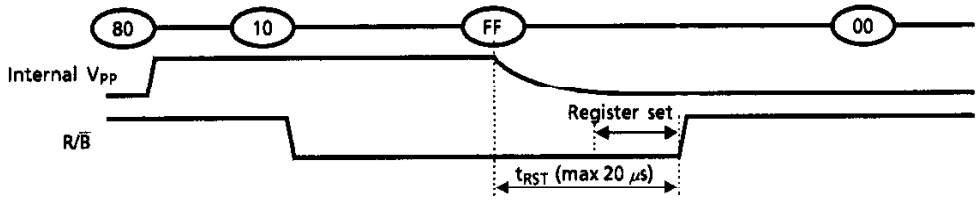


Figure 10.

- When a Reset (FFH) command is input during erasing

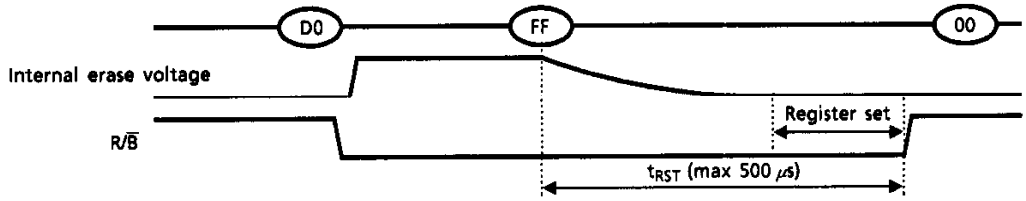


Figure 11.

- When a Reset (FFH) command is input during a Read operation

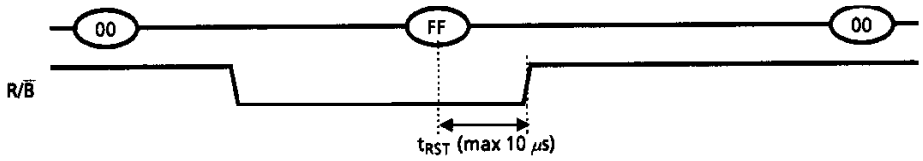


Figure 12.

- When a Reset (FFH) command is input after a Suspend command

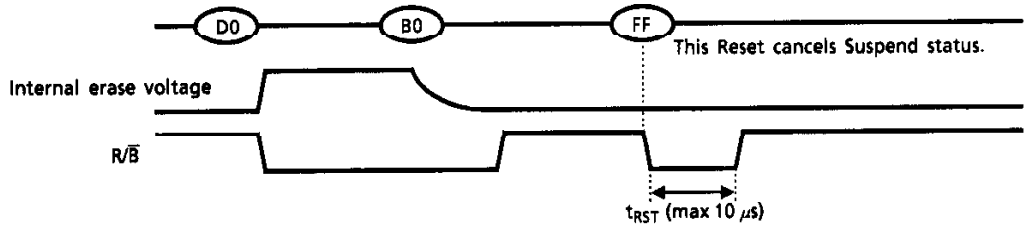


Figure 13.

- When a Status Read command (70H) is input after a Reset

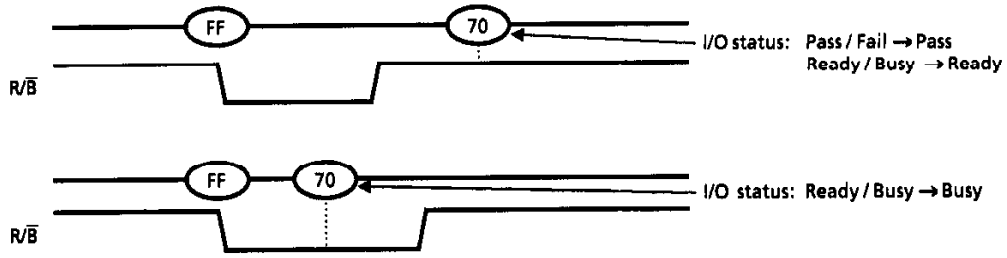


Figure 14.

- When two or more Reset commands are input in succession

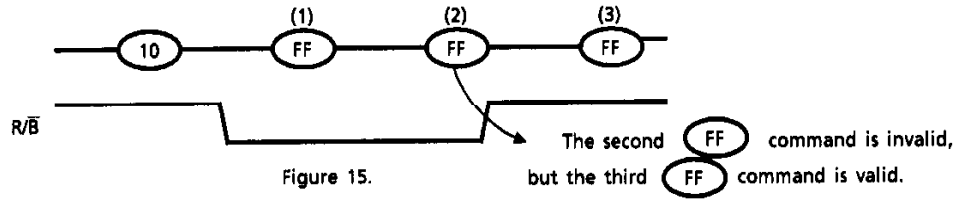
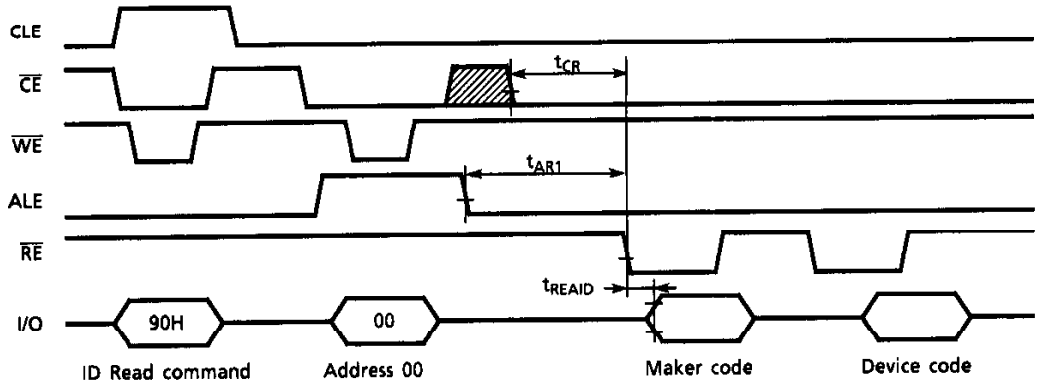


Figure 15.

ID Read

The TC58V16 contains ID codes which identify the device type and the manufacturer. The ID codes can be read out under the following timing conditions:



Refer to the specifications for the t_{READID}, t_{CR} and t_{AR1} access timings.

Figure 16. ID Read timing

Table 6. Code table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	1	1	1	0	1	0	1	0	EAH

DEVICE PHYSICS:

Program Operation

Figure 17 shows the programming mechanism at the NAND memory cell level. The Program operation is used to write 0 into an erased memory cell (a data cell that holds a 1) using a tunneling mechanism. An example Program operation to program 0 into TR1 and 1 into TR2 is as follows:

(1) A high level is applied to Select line 1 and a low level to Select line 2, so that the device is connected to the Bit line and disconnected from the ground line.

(2) Vpp (≈20 V) is applied to the selected word line and an inhibit voltage of VPI (≈10 V) is applied to the unselected word lines.

(3) 0 V is applied to the bit line tied to cell transistor TR1 and the inhibit voltage VDPI (≈10 V) is applied to the bit line tied to TR2.

(4) Vpp is applied between the control gate and the channel in TR1, as shown in Figure 18, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.

(5) The injected electrons are captured in the floating gate which is surrounded by an oxide layer and will remain there, even after power is cut off, until they are removed by an Erase operation.

(6) Although 20 V is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10 V because the voltage of the channel is 10 V. Therefore, tunneling does not take place (i.e. electrons are not injected into the floating gate).

(7) Tunneling does not take place in the unselected pages because of the 10 V (VPI) applied to the unselected word lines which makes the voltage difference between the control gate and channel only 10 V.

Thus the floating gate of the 0 cell becomes negatively charged and that of the 1 cell becomes positively charged.

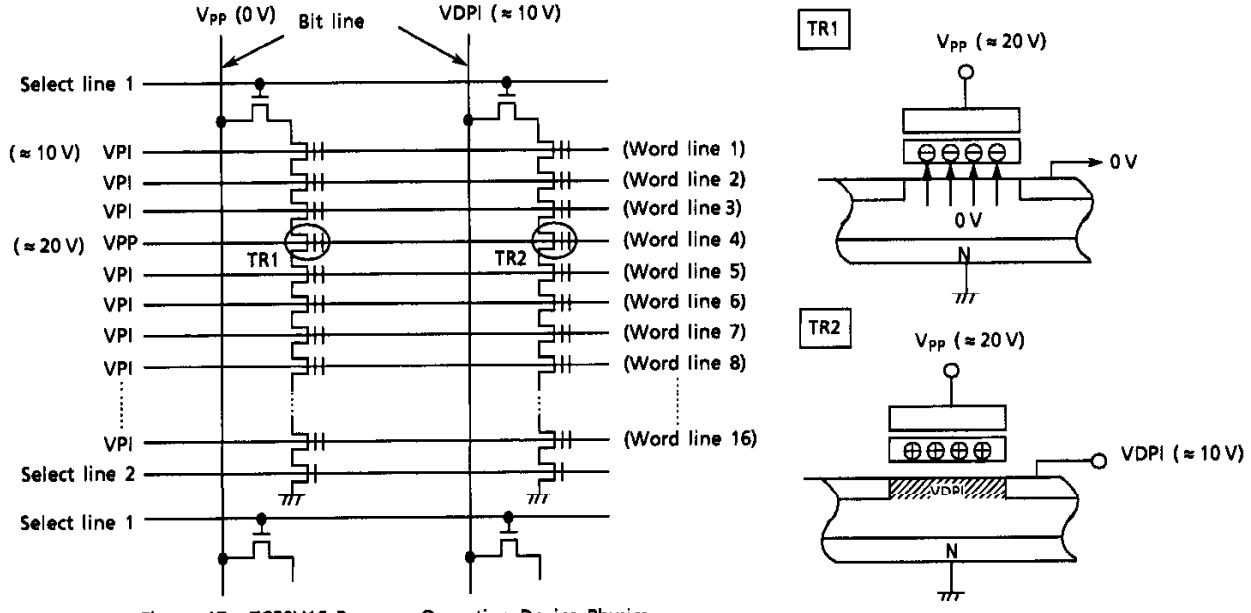


Figure 17. TC58V16 Program Operation Device Physics

Erase Operation

Figure 18 shows the Erase mechanism at the NAND memory cell level . The Erase operation is used to turn all the 0 (programmed) cells in a block back to 1 . The captured electrons are pulled out from the floating gate to the substrate by a tunneling mechanism.
0 V is applied to the control gate and Vpp (≈20 V) is applied to the substrate so that a 20-V potential is created, causing the electrons in the floating gate to be pulled out by the tunneling mechanism.

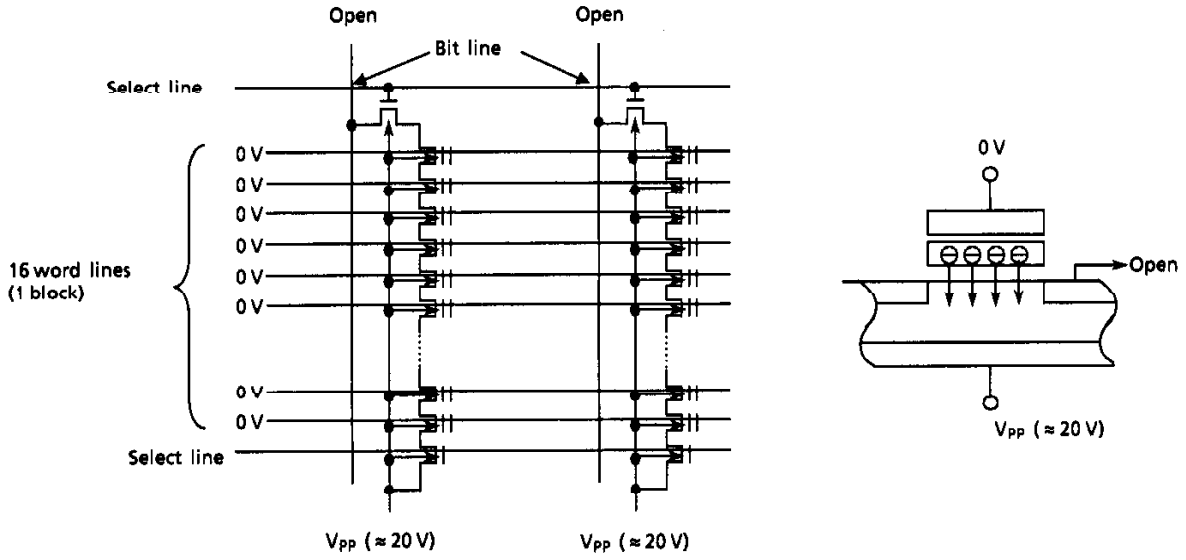


Figure 18. Erase Operation Device Physics

Read Operation

After programming, the state of the memory cell is either 0 (negative charge on the floating gate) or 1 (positive charge on the floating gate). The state is indicated by the threshold voltage (Vth) which is a parameter of the MOS transistor as shown in Figure 19. The threshold voltage of a transistor holding data 0 is distributed in the plus region, while that of a transistor holding data 1 is distributed in the minus region.

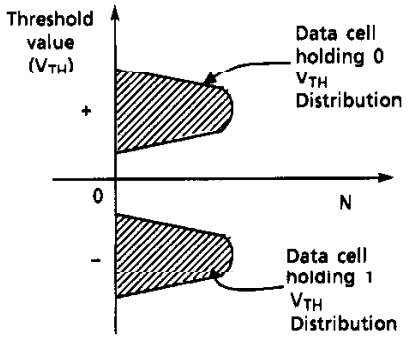


Figure 19. V_{TH} distribution for data cells holding 0 and 1

Figure 20 shows the Read operation mechanism at the memory cell level :

(1) A High voltage level is applied to Select lines 1 and 2 in the block which includes the selected page, so that the 16 NAND memory cells are connected to the Bit line and to ground.

(2) 0 V is applied to the control gates of the selected page and a High level voltage is applied to the control gates of the unselected pages.

(3) In Figure 20, transistor TR2, which is holding a 1, turns on, while transistor TR1, holding 0, turns off. All other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground, while the precharged bit line tied to TR1 remains High because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as 1 and 0 respectively.

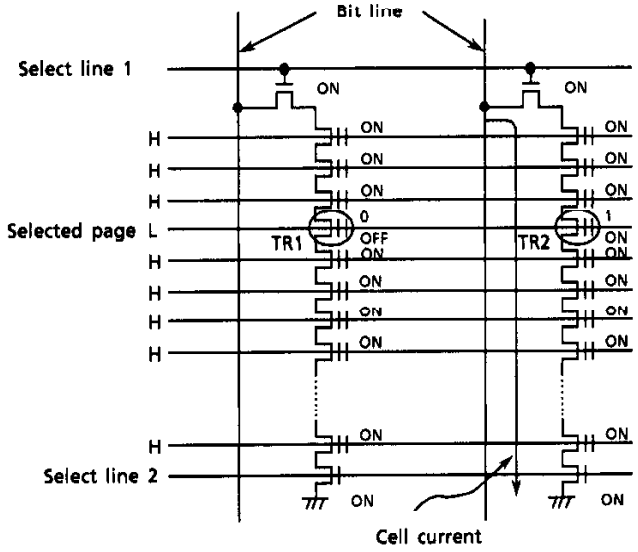


Figure 20. Read Operation Device Physics

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Pointer control for 00H and 50H

The TC58V16 has two Read modes, which respectively set the pointer to point to either the main memory area of a page or to the redundancy area. The pointer can be set to point to any location from 0 to 255 in Read mode (1) and to any location from 256 to 263 in Read mode (2). Figure 21 shows a block diagram of their operations.

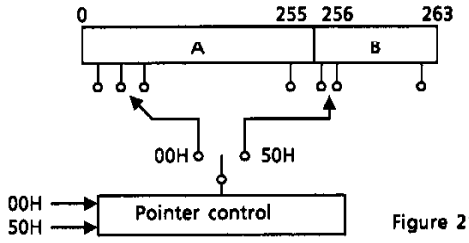


Figure 21. Pointer control

The pointer is set to region A by the 00H command and to region B by the 50H command.

(Example)

The 00H command must be input to set the pointer back to region A when the pointer is pointing to region B.

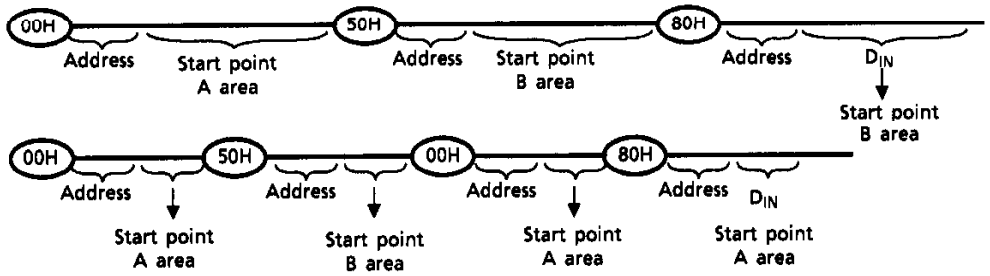
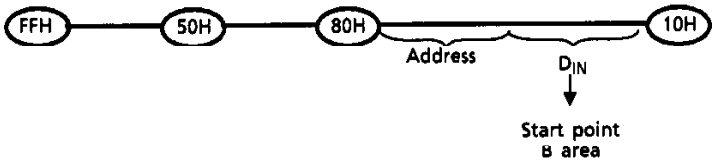


Figure 22. Example of How to Set the Pointer

If the start point is set in region B using the 50H command, so as to program region B only, the contents of the Data register must be set to 1 in advance using the FFH command.



(3) Acceptable commands after Serial Input command 80H

Once the Serial Input command (80H) has been input, do not input any command other than the Program Execution command (10H) or the Reset command (FFH).

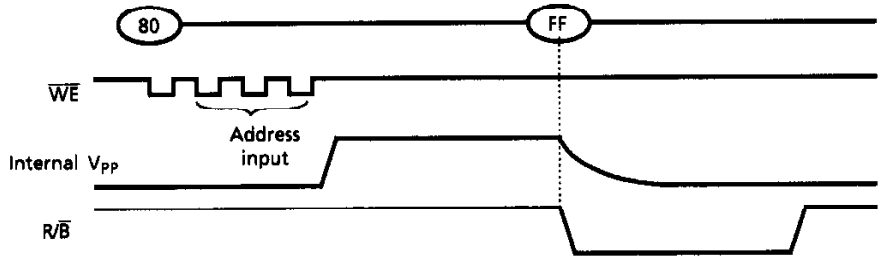
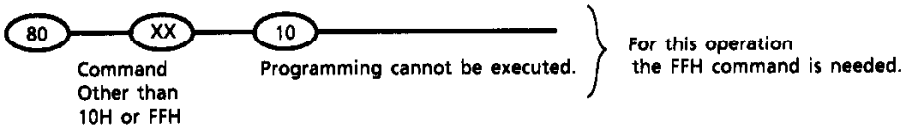


Figure 23.

If a command other than 10H or FFH is input, the Program operation is not performed.



(4) Status Read during a Read operation

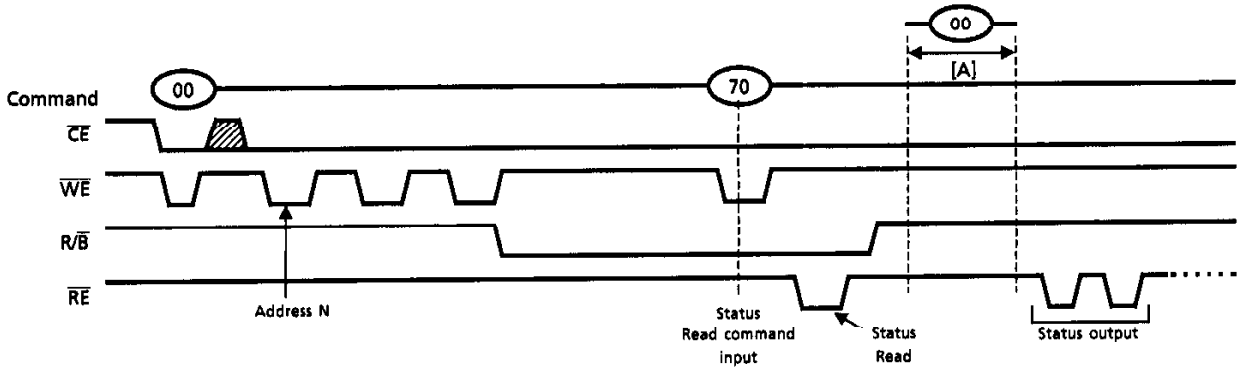


Figure 24.

The device status can be read out by inputting the Status Read command 70H in Read mode. Once the device has been set to Status Read mode by a 70H command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command 00H is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(5) Suspend command B0H

The following points need to be borne in mind when the device is interrupted by a B0H command during block erasing.

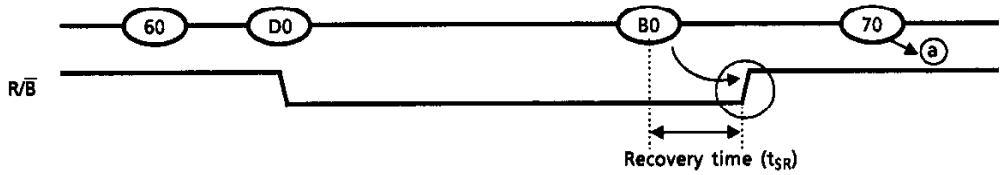


Figure 25.

The device status changes from Busy to Ready when B0H is input. However, the following two cases cannot readily be distinguished from one another.

- The B0H command suspends the Erase operation: Busy → Ready
- The D0H Erase operation is completed before the B0H (Suspend) command is received: Busy → Ready

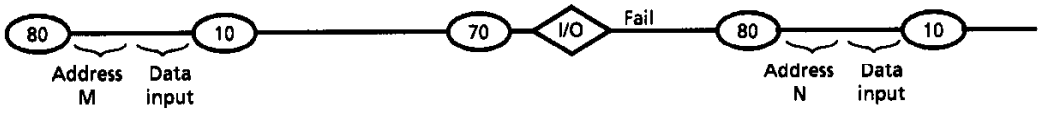
Therefore, the device status needs to be checked to see whether or not the B0H command was accepted. This is done by issuing a 70H command after the device goes to Ready.

The device responds as follows if a D0H command (Resume) is input instead of 70H.

- If B0H was accepted:
  Erase operation is resumed. (The device is Busy.)
- If B0H was not accepted. (Erase operation has been completed.):
  D0H command cannot be accepted. (The device is Ready.)

Distinguish between the above two cases by monitoring the R/$\overline{B}$ signal.

(6) Auto programming failure.



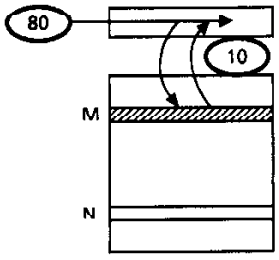


Figure 26.

If the programming result for page address M is Fail, try to program the page to address N in another block. Because the previous data has been lost, the same sequence of 80H command, address and data must be input.

(7) Data transfer

The data in page address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e. 1s will become 0s and 0s will become 1s).

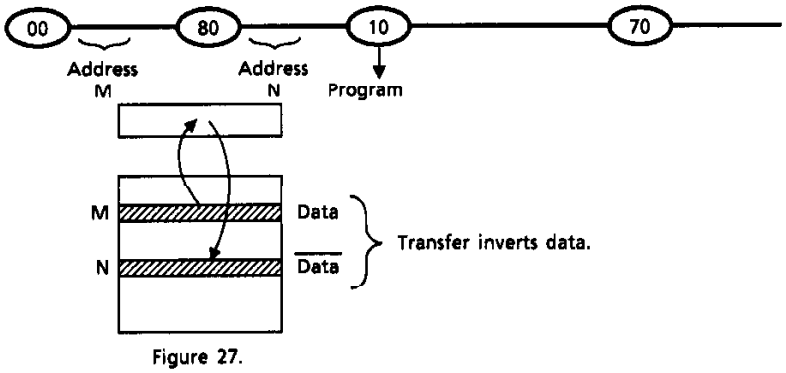
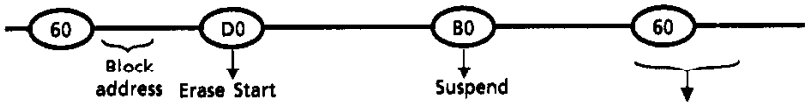


Figure 27.

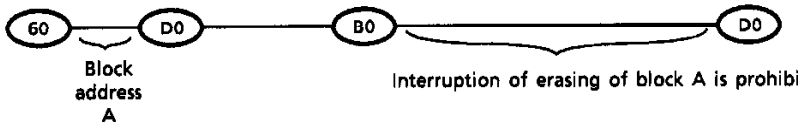
(8) Block Erase after Suspend command B0H



A Block Erase command is prohibited when the device has been suspended by the input of a B0H command during a Block Erase operation. Only a Program or Read operation is allowed during this Erase Suspend interruption.

(9) Interruption of block erasure

After input of a B0H command, neither a Program nor a Read operation is allowed for the block which is currently being erased.



(10) R/$\overline{B}$: termination for the Ready/Busy pin (R/$\overline{B}$)

A pull-up resistor must be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.

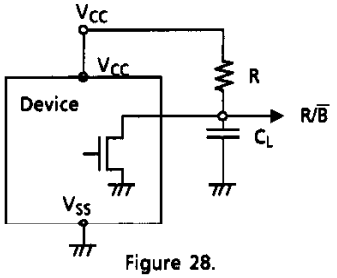
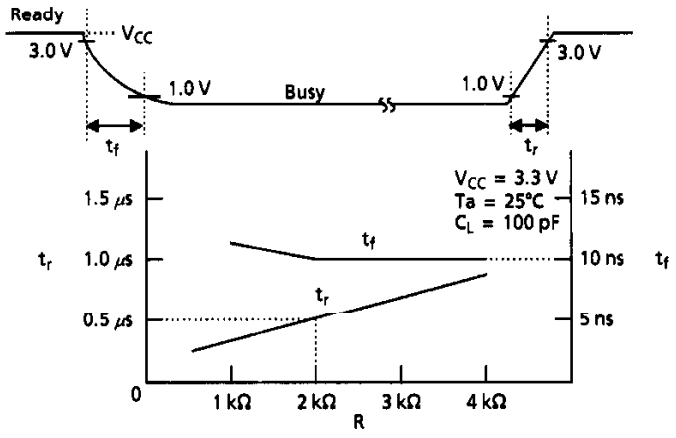


Figure 28.

This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

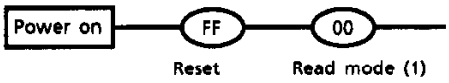


(11) Status after power-on

Although the device is set to Read mode after power-on, the following sequence is necessary because some input signals may not be stable at power-on.

- Operating mode : Read mode (1)
- Address register : All 0s
- Data register : Indeterminate
- High-voltage generation circuit: Off

Power-on sequence



(12) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary:

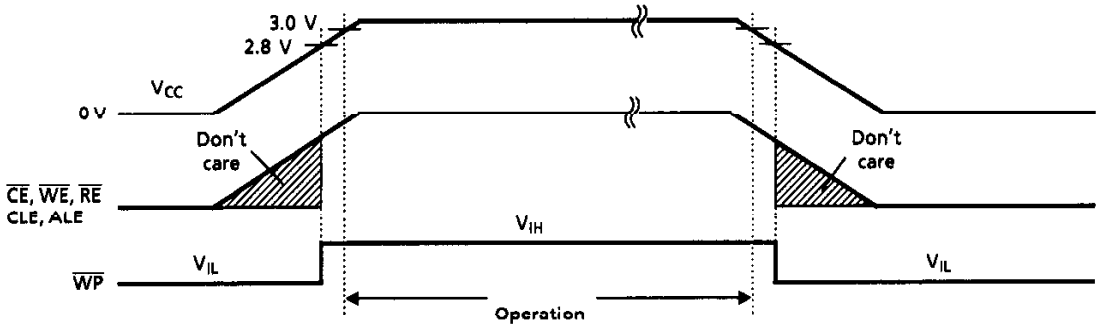


Figure 29. Power-on/off Sequence

(13) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The $\overline{WP}$ signal must be kept High before input of a 80H or 60H command (a Program or Erase commands).

If $\overline{WP}$ goes high after a Program (80H) or Erase (60H) command, the Program or Erase operation cannot be guaranteed.

Program

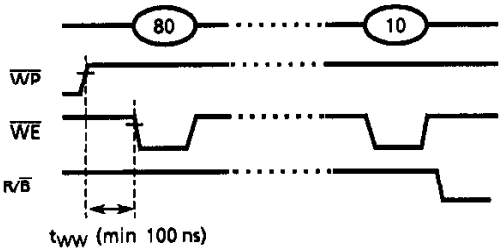


Figure 30.

Erase

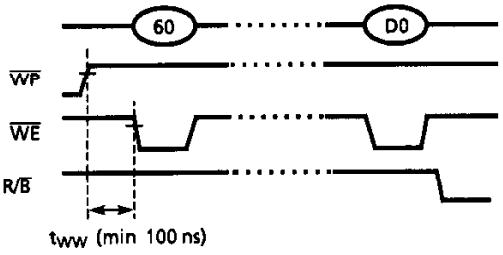
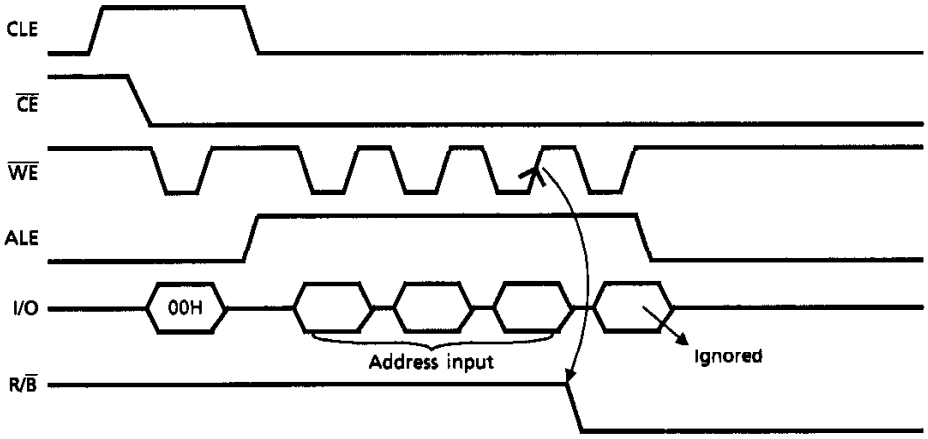


Figure 31.

(14) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when WE goes High in the third cycle.

Figure 32.

Programming operation

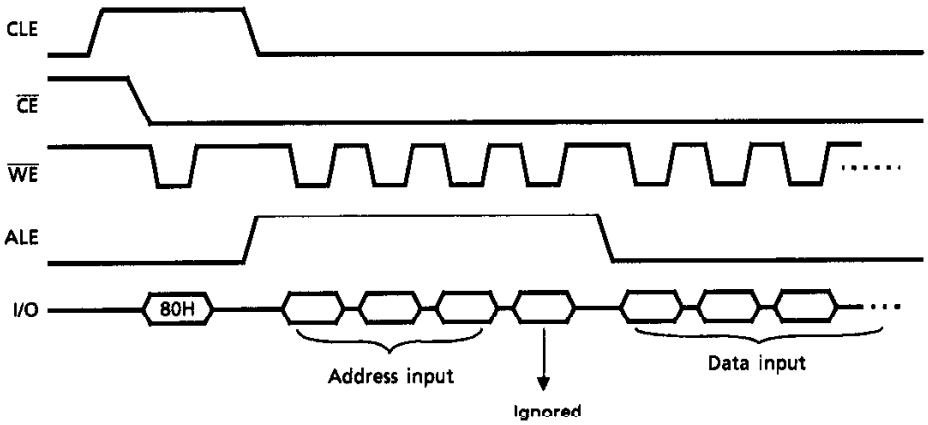


Figure 33.

(15) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as shown below.

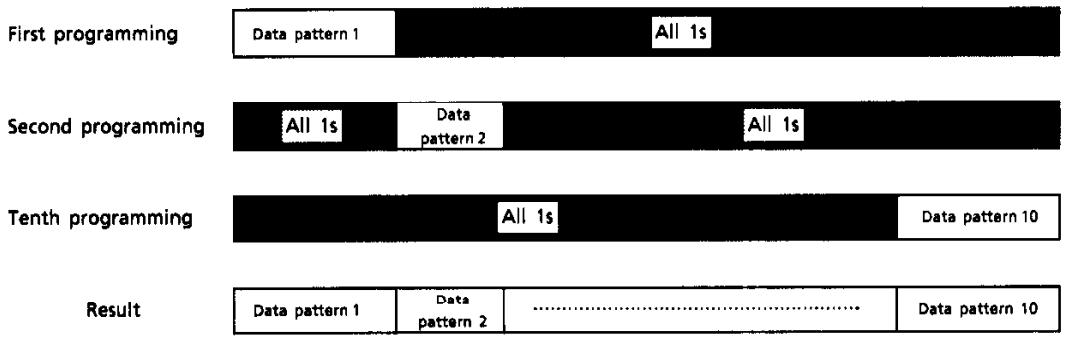


Figure 34.

Note: The input data for unprogrammed or previously programmed page segments must be 1 (i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to 1).

(16) Note Regarding the $\overline{RE}$ Signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a 00H or 50H command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing. If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array → register) will occur and the device will enter Busy state. (Refer to Figure 35.)

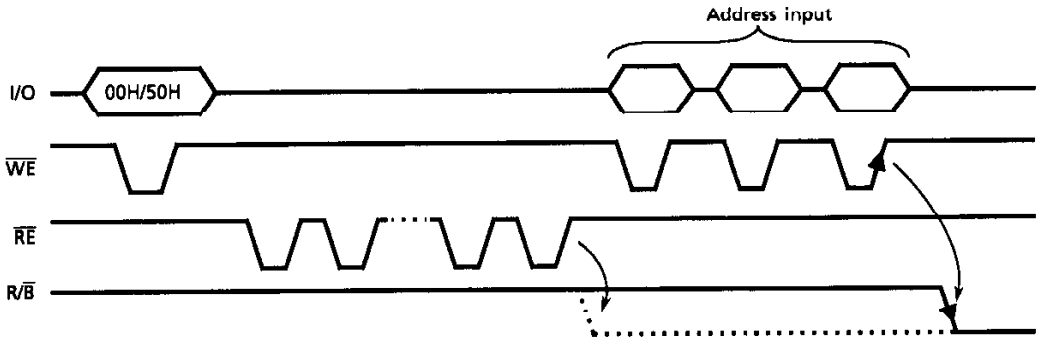


Figure 35.

Hence the $\overline{RE}$ clock input must start after the address input.

(17) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, the following issues must be recognized:

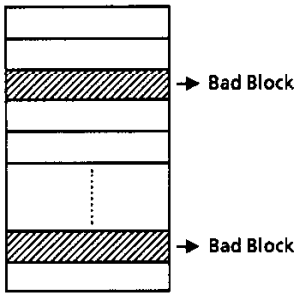


Figure 36.

Referring to the Block status area in the redundant area allows the system to detect bed blocks in the accordance with the physical data format issued by the SSFDC Forum. Detect the bad blocks by checking the Block Status Area at the system power-on, and do not access the bad blocks in the following routine.

The number of valid blocks at the time of shipment is as follows:

Table 7.

	MIN	TYP	MAX	UNIT
Valid (Good) Block Number	502	508	512	Block

(18) Failure Phenomena for Program and Erase Operations.

The device may fail during program or erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Program Failure	Status Read after Program → Block Replacement
Single Bit*	Program Failure '1'→'0'	(1) Block Verify after Program → Retry
		(2) ECC

* : (1) or (2)

- ECC : Error Correcting code
- Block Replacement

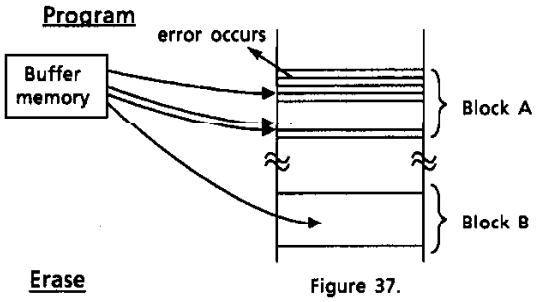


Figure 37.

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using other appropriate scheme).

(19) Chattering of Connector

There may be contact chattering when the TC58V16BDC is inserted or removed from a connector.

This chattering may cause damage to the data in the TC58V16BDC. Therefore, sufficient time must be allowed for contact bouncing to subside when a system is designed with SmartMedia™.

(20) The TC58V16BDC is formatted to comply with the Physical and Logical Data Format of the SSFDC Forum at the time of shipping.

Handling Precaution

(1) Avoid bending or subjecting the card to sudden impact.
(2) Avoid touching the connectors so as to avoid damage from static electricity.
This card should be kept in the antistatic film case when not in use.
(3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data corruption that may occur because of mishandling.

SSFDC Forum

The SSFDC Forum*1 is a voluntary organization intended to promote the SmartMedia™, a small removable NAND flash memory card. The SSFDC Forum standardized the following specifications in order to keep the compatibility of SmartMedia™ in systems. The latest specifications issued by the Forum must be referenced when a system is designed with SmartMedia™, especially with large capacity SmartMedia™ *2.

The major specifications issued by the Forum as of March 1998 are as follows (These specify 1Mbyte to 128Mbyte SmartMedia™).

SmartMedia™ Electrical Specifications Ver.1.10*3
SmartMedia™ Physical Format Specification Ver.1.20
SmartMedia™ Logical Format Specification Ver.1.10

*1: The flash memory card SSFDC (Solid State Floppy Disk Card) was renamed to SmartMedia™ in July 1996.

*2: The Physical Format of 32MByte and larger SmartMedia™ has a modification from that of the smaller capacity SmartMedia™.

*3: Some electrical specifications in this data sheet show differences from the Forum's electrical specification. complying with the Forum's electrical specification maintains compatibility with other SmartMedias.

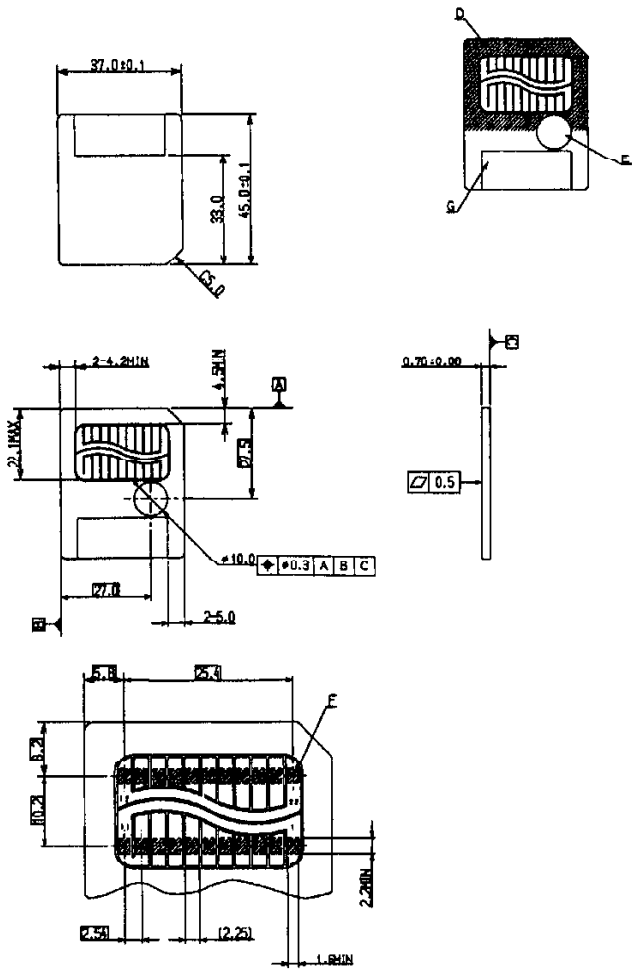
The SSFDC Forum can be contacted by accessing the Forum's home page.

URL http://www.ssfdc.or.jp

PACKAGE DIMENSIONS

FDC-22A

Unit: mm



E : Write-protect area

F : The distance between the surface of D and all contact areas is less than 0.1 mm.

G: Index area