# TC6215

## N-Channel and P-Channel Enhancement-Mode Dual MOSFETs

### Features

- Back-to-Back, Gate-Source Zener Diodes
- Guaranteed $R_{DS(ON)}$ at 4V Gate Drive
- Low Threshold
- Low On-resistance
- Independent N-channel and P-channel
- Electrically Isolated N-channel and P-channel
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdowns
- Low Input and Output Leakage

### Applications

- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interfaces

### General Description

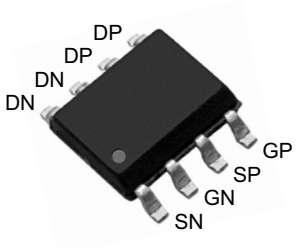
The TC6215 consists of high-voltage, low-threshold N-channel and P-channel MOSFETs in an 8-lead SOIC (TG) package. Both MOSFETs have integrated back-to-back gate-source Zener diode clamps and guaranteed $R_{DS(ON)}$ ratings down to 4V gate drive, allowing them to be driven directly with standard 5V CMOS logic.

These low-threshold Enhancement-mode (normally-off) transistors utilize an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

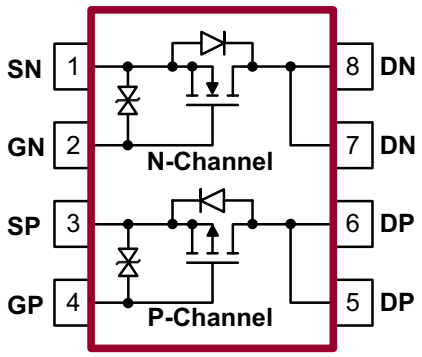
### Package Type

**8-lead SOIC**
(Top view)




See Table 3-1 for pin information.

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage ..... $BV_{DSS}$
Drain-to-Gate Voltage ..... $BV_{DGS}$
Gate-to-Source Voltage ..... ±20V
Operating Ambient Temperature, $T_A$ .....–55°C to +150°C
Storage Temperature, $T_S$ .....–55°C to +150°C

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $T_A$ = 25°C.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **N-CHANNEL** | | | | | | |
| **DC PARAMETER** (Note 1) | | | | | | |
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | 150 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1 | — | 2 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | — | –4.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA (Note 2) |
| Gate-Source, Back-to-Back Zener Voltage | $VZ_{GS}$ | ±14 | — | ±25 | V | $I_{GS}$ = ±1 mA |
| Zero-gate Voltage Drain Current | $I_{DSS}$ | — | — | 5 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Maximum rating |
| | | — | — | 1 | mA | $V_{DS}$ = 0.8 Maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C (Note 2) |
| On-state Drain Current | $I_{D(ON)}$ | — | 2 | — | A | $V_{GS}$ = 4.5V, $V_{DS}$ = 25V |
| | | — | 3.8 | — | | $V_{GS}$ = 10V, $V_{DS}$ = 25V |
| Static Drain-to-Source On-state Resistance | $R_{DS(ON)}$ | — | — | 4 | Ω | $V_{GS}$ = 4V, $I_D$ = 0.5A |
| | | — | — | 5 | | $V_{GS}$ = 5V, $I_D$ = 2A |
| | | — | — | 4 | | $V_{GS}$ = 10V, $I_D$ = 2A |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | — | 1 | %/°C | $V_{GS}$ = 5V, $I_D$ = 2A (Note 2) |
| **AC PARAMETER** (Note 2) | | | | | | |
| Forward Transconductance | $G_{FS}$ | 560 | — | — | mmho | $V_{DS}$ = 10V, $I_D$ = 0.5A |
| Input Capacitance | $C_{ISS}$ | — | 120 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1 MHz |
| Common-Source Output Capacitance | $C_{OSS}$ | — | 33 | — | pF | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | 11 | — | pF | |
| Turn-on Delay Time | $t_{d(ON)}$ | — | 2.5 | — | ns | $V_{DD}$ = 25V, $I_D$ = 1A, $R_{GEN}$ = 25Ω |
| Rise Time | $t_r$ | — | 2.3 | — | ns | |
| Turn-off Delay Time | $t_{d(OFF)}$ | — | 17.2 | — | ns | |
| Fall Time | $t_f$ | — | 11.3 | — | ns | |
| **DIODE PARAMETER** | | | | | | |
| Diode Forward Voltage Drop | $V_{SD}$ | — | — | 1.4 | V | $V_{GS}$ = 0V, $I_{SD}$ = 0.5A (Note 1) |
| Reverse Recovery Time | $t_{rr}$ | — | 90 | — | ns | $V_{GS}$ = 0V, $I_{SD}$ = 0.5A |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested and at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% sample tested.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise noted, $T_A$ = 25°C.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **P-CHANNEL** | | | | | | |
| **DC PARAMETER** (Note 1) | | | | | | |
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | –150 | — | — | V | $V_{GS}$ = 0V, $I_D$ = –1 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | –1 | — | –2 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = –1 mA |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | — | 4.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = –1 mA (Note 2) |
| Gate-Source Back-to-back Zener Voltage | $VZ_{GS}$ | ±14 | — | ±25 | V | $I_{GS}$ = ±1 mA |
| Zero-gate Voltage Drain Current | $I_{DSS}$ | — | — | –5 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Maximum rating |
| | | — | — | –1 | mA | $V_{DS}$ = 0.8 Maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C (Note 2) |
| On-state Drain Current | $I_{D(ON)}$ | — | –1.5 | — | A | $V_{GS}$ = –4.5V, $V_{DS}$ = –25V |
| | | — | –3 | — | | $V_{GS}$ = –10V, $V_{DS}$ = –25V |
| Static Drain-to-Source On-state Resistance | $R_{DS(ON)}$ | — | — | 7.5 | Ω | $V_{GS}$ = –4V, $I_D$ = –0.25A |
| | | — | — | 9 | | $V_{GS}$ = –5V, $I_D$ = –1A |
| | | — | — | 7 | | $V_{GS}$ = –10V, $I_D$ = –2A |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta_{RDS(ON)}$ | — | — | 1 | %/°C | $V_{GS}$ = –5V, $I_D$ = –0.25A (Note 2) |
| **AC PARAMETER** (Note 2) | | | | | | |
| Forward Transconductance | $G_{FS}$ | 290 | — | — | mmho | $V_{DS}$ = –10V, $I_D$ = –0.25A |
| Input Capacitance | $C_{ISS}$ | — | 127 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = –25V, f = 1 MHz |
| Common-Source Output Capacitance | $C_{OSS}$ | — | 29 | — | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | 9 | — | | |
| Turn-on Delay Time | $t_{d(ON)}$ | — | 2.4 | — | ns | $V_{DD}$ = –25V, $I_D$ = –1A, $R_{GEN}$ = 25Ω |
| Rise Time | $t_r$ | — | 2.3 | — | | |
| Turn-on Delay Time | $t_{d(OFF)}$ | — | 16.2 | — | | |
| Fall Time | $t_f$ | — | 11.1 | — | | |
| **DIODE PARAMETER** | | | | | | |
| Diode Forward Voltage Drop | $V_{SD}$ | — | — | –1.4 | V | $V_{GS}$ = 0V, $I_{SD}$ = –0.25A (Note 1) |
| Reverse Recovery Time | $t_{rr}$ | — | 80 | — | ns | $V_{GS}$ = 0V, $I_{SD}$ = –0.25A |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested and at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% sample tested.

## TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | |
| Operating Ambient Temperature | $T_A$ | –55°C | — | +150 | °C | |
| Storage Temperature | $T_S$ | –55°C | — | +150 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 8-lead SOIC | $\theta_{JA}$ | — | 101 | — | °C/W | Note 1 |

**Note 1:** 1 oz, 4-layer, 3” x 4” PCB

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

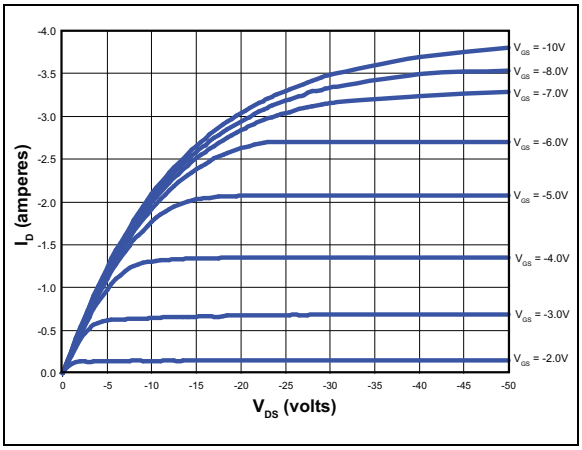



***FIGURE 2-1:*** *P-channel Output Characteristics.*

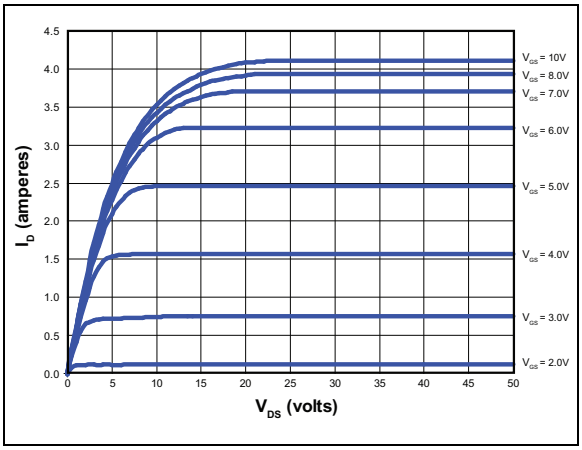



***FIGURE 2-3:*** *N-channel Output Characteristics.*

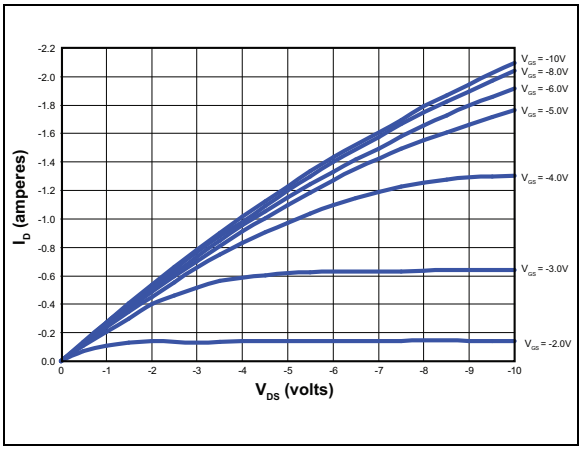



***FIGURE 2-2:*** *P-channel Saturation Characteristics.*

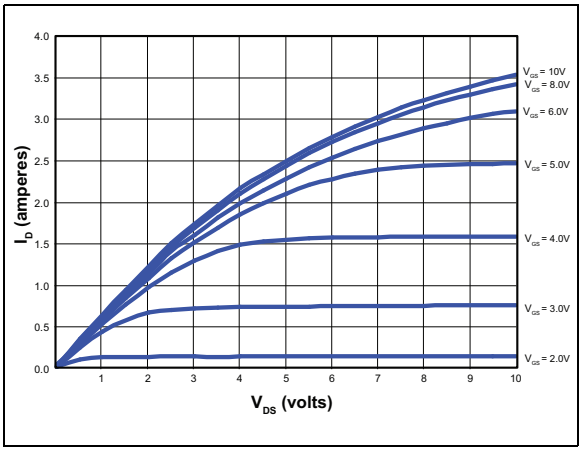



***FIGURE 2-4:*** *N-channel Saturation Characteristics.*

## 3.0 PIN DESCRIPTION

Table 3-1 shows the description of pins in TC6215. Refer to **Package Type** for the location of pins.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | SN | Source N-Channel |
| 2 | GN | Gate N-Channel |
| 3 | SP | Source P-Channel |
| 4 | GP | Gate P-Channel |
| 5 | DP | Drain P-Channel |
| 6 | DP | Drain P-Channel |
| 7 | DN | Drain N-Channel |
| 8 | DN | Drain N-Channel |

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 and Figure 4-2 illustrate the switching waveforms and test circuits for TC6215.

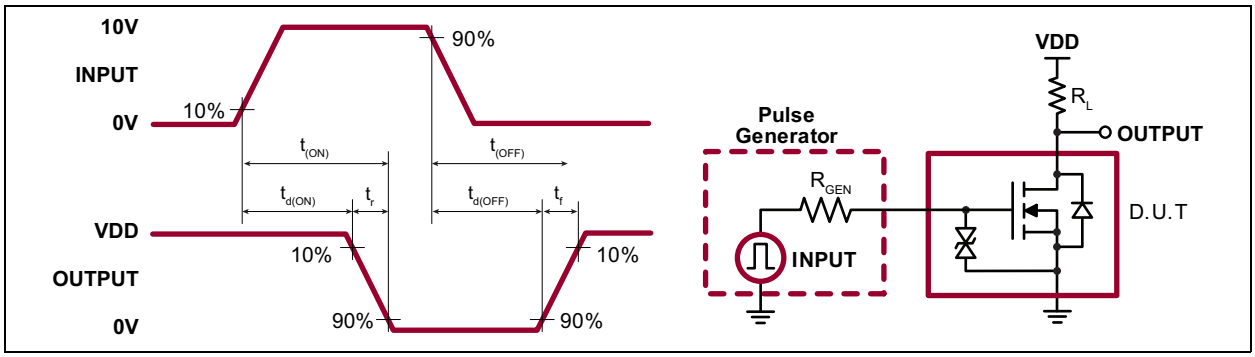



***FIGURE 4-1:*** *N-channel Switching Waveforms and Test Circuit.*

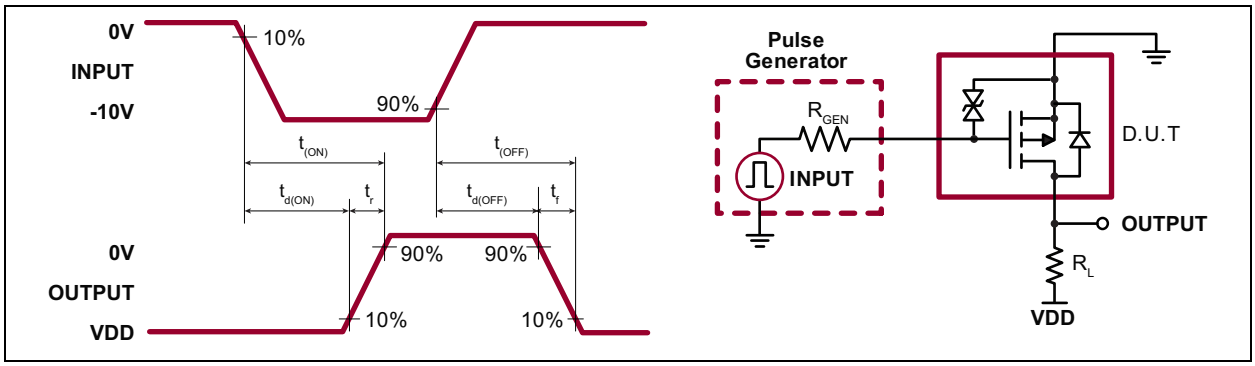



***FIGURE 4-2:*** *P-channel Switching Waveforms and Test Circuit.*

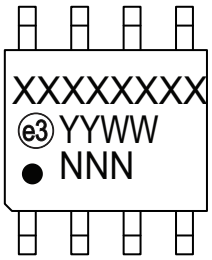
**TABLE 4-1: PRODUCT SUMMARY**

| $BV_{DSS}/BV_{DGS}$ (V) | | $R_{DS(ON)}$ (Maximum) (Ω) | |
|---|---|---|---|
| **N-Channel** | **P-Channel** | **N-Channel** | **P-Channel** |
| 150 | –150 | 4 | 7 |

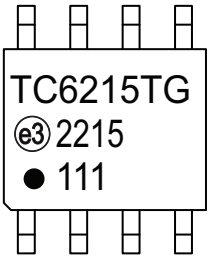
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

8-lead SOIC




Example

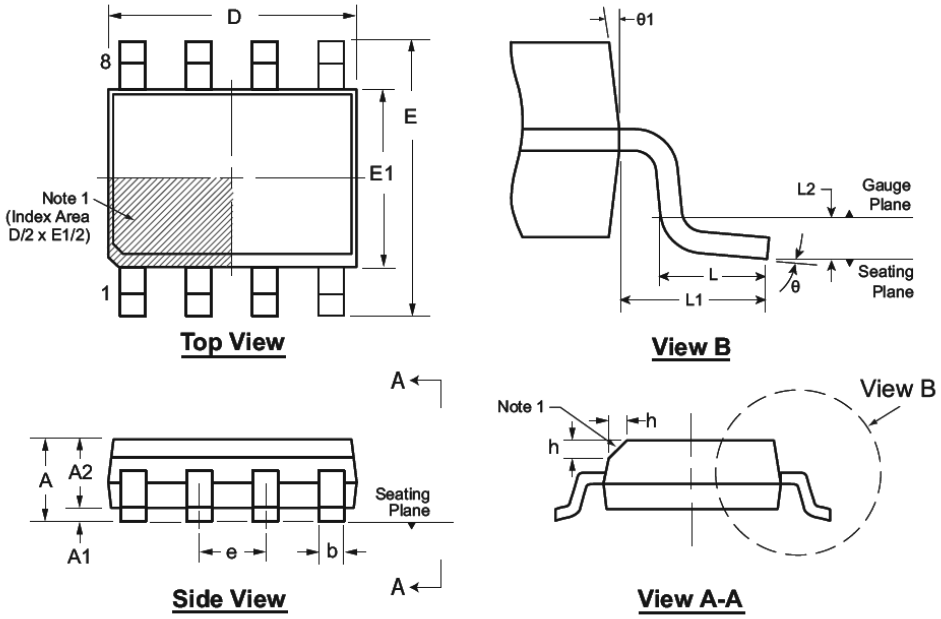



| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

## 8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

***4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch***




Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

***Note:***

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 4.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

*JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.*
** This dimension is not specified in the JEDEC drawing.*
***Drawings are not to scale.***

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (June 2022)

- Converted Supertex Doc# DSFP-TC6215 to Microchip DS20005776A
- Changed the package marking format
- Changed the packaging quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | TC6215 | = | N-Channel and P-Channel Enhancement-Mode Dual MOSFET |
| Package: | TG | = | 8-lead SOIC |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Type: | (blank) | = | 3300/Reel for a TG Package |

**Example:**

a) TC6215TG-G: N-Channel and P-Channel Enhancement-Mode Dual MOSFET, 8-lead SOIC, 3300/Reel

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