TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC374P, TC74AC374F, TC74AC374FT
TC74AC534P, TC74AC534F

Octal D-Type Flip-Flop with 3-state Output

TC74AC374P/F/FT	Non-Inverting
TC74AC534P/F	Inverting

The TC74AC374 and TC74AC534 are advanced high speed CMOS OCTAL FLIP-FLOPS fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

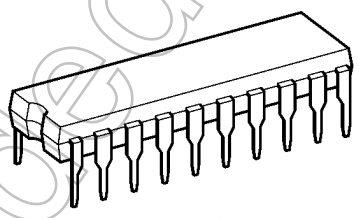
The TC74AC374 has non-inverting outputs, and TC74AC534 has inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

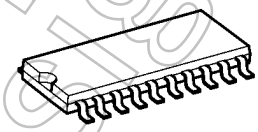
- High speed: f_{max} = 200 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74F374/534

TC74AC374P, TC74AC534P



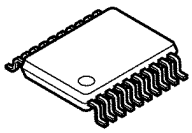
DIP20-P-300-2.54A

TC74AC374F, TC74AC534F



SOP20-P-300-1.27A

TC74AC374FT



TSSOP20-P-0044-0.65A

Weight

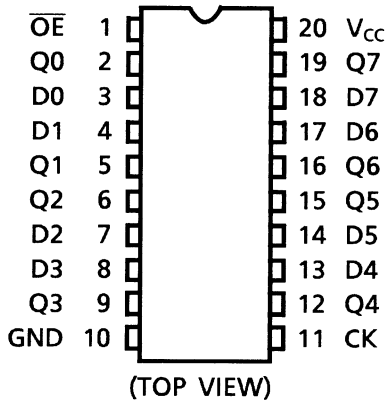
DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Not Recommended for New Design

Start of commercial production
1986-05

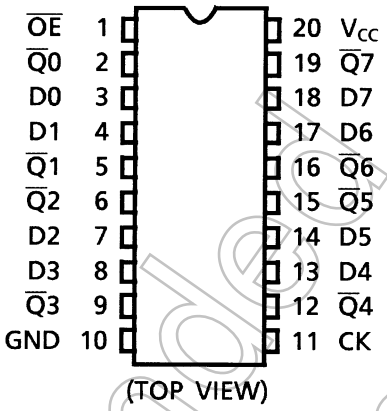
Pin Assignment

TC74AC374



(TOP VIEW)

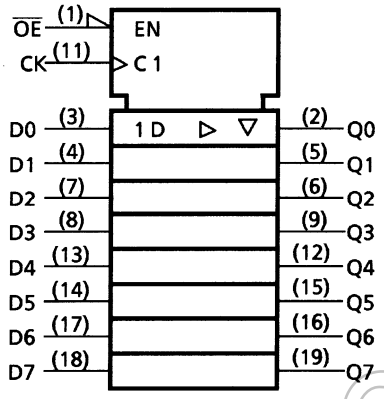
TC74AC534



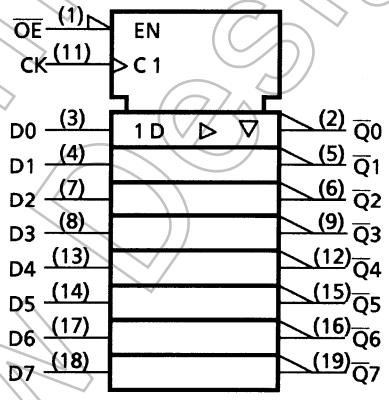
(TOP VIEW)

IEC Logic Symbol

TC74AC374



TC74AC534



Truth Table

Inputs			Outputs	
$\overline{OE}$	CK	D	Q (374)	$\overline{Q}$ (534)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q}_n$
L	↑	L	L	H
L	↑	H	H	L

X: Don't care

Z: High impedance

Q_n ($\overline{Q}_n$): No change

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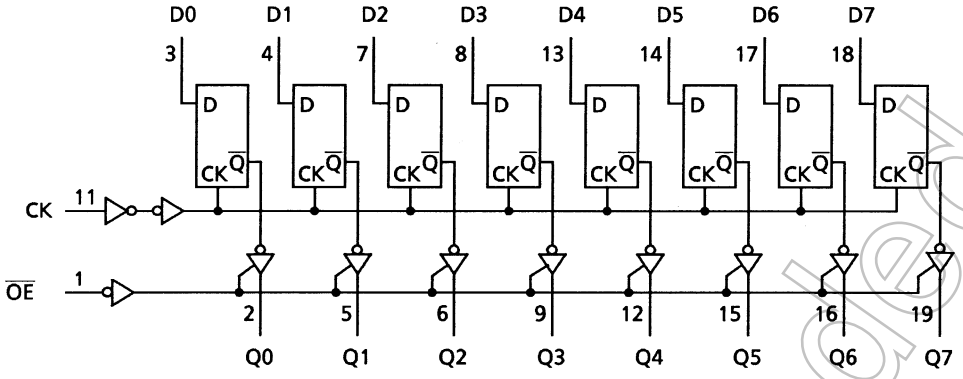
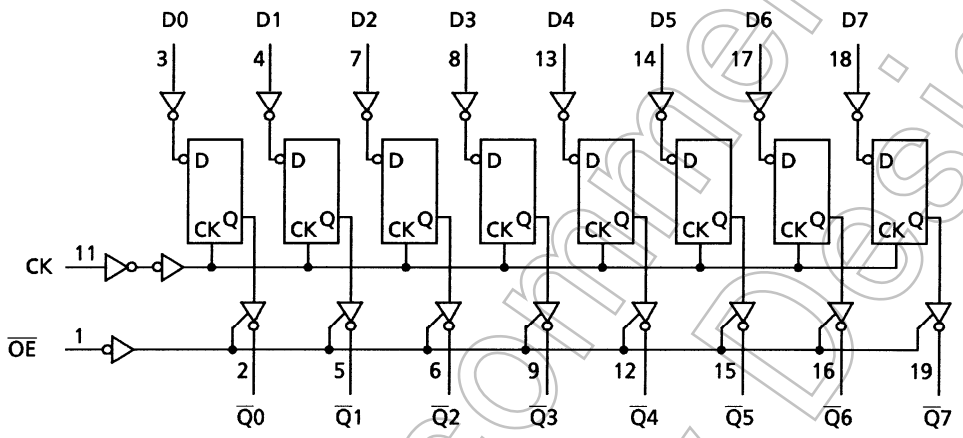
System Diagram

TC74AC374



TC74AC534



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Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C, a derating factor of −10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

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Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −24 mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

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Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = −40 to 85°C	Unit
			V_{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	$t_{W(H)}$	—	3.3 ± 0.3	7.0	7.0	ns
	$t_{W(L)}$		5.0 ± 0.5	5.0	5.0	
Minimum set-up time	t_s	—	3.3 ± 0.3	9.0	9.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum hold time	t_h	—	3.3 ± 0.3	0.0	0.0	ns
			5.0 ± 0.5	0.0	0.0	

AC Characteristics ($C_L = 50$ pF, $R_L = 500\ \Omega$, input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q, $\overline{Q}$)	t_{pLH}	—	3.3 ± 0.3	—	8.5	15.8	1.0	18.0	ns
	t_{pHL}		5.0 ± 0.5	—	6.1	8.7	1.0	10.0	
Output enable time	t_{pZL}	—	3.3 ± 0.3	—	7.5	14.0	1.0	16.0	ns
	t_{pZH}		5.0 ± 0.5	—	6.1	8.7	1.0	10.0	
Output disable time	t_{pLZ}	—	3.3 ± 0.3	—	5.5	12.3	1.0	14.0	ns
	t_{pHZ}		5.0 ± 0.5	—	4.7	7.0	1.0	8.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	55	120	—	55	—	MHz
			5.0 ± 0.5	100	160	—	100	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Output capacitance	C_{OUT}	—		—	10	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	37	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption

Average operating current can be obtained by the equation:

I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

C_{PD} (total) = 25 + 12·n

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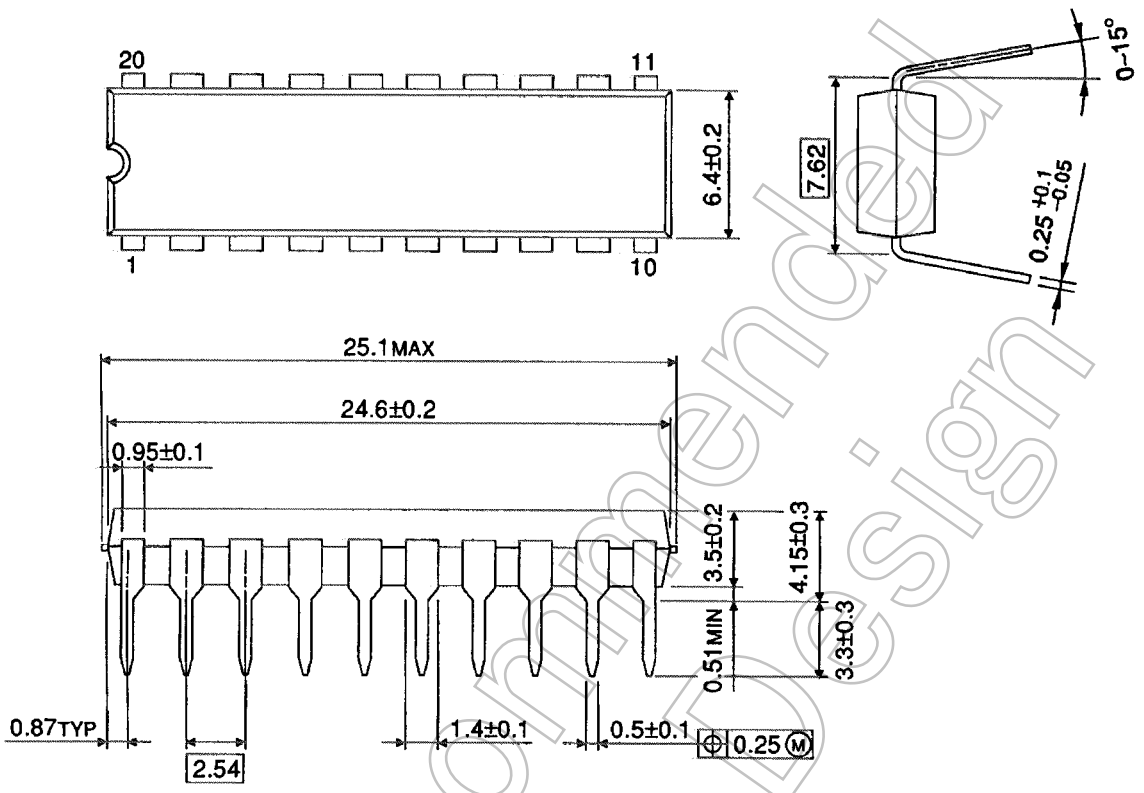
Package Dimensions

DIP20-P-300-2.54A Unit : mm



Weight: 1.30 g (typ.)

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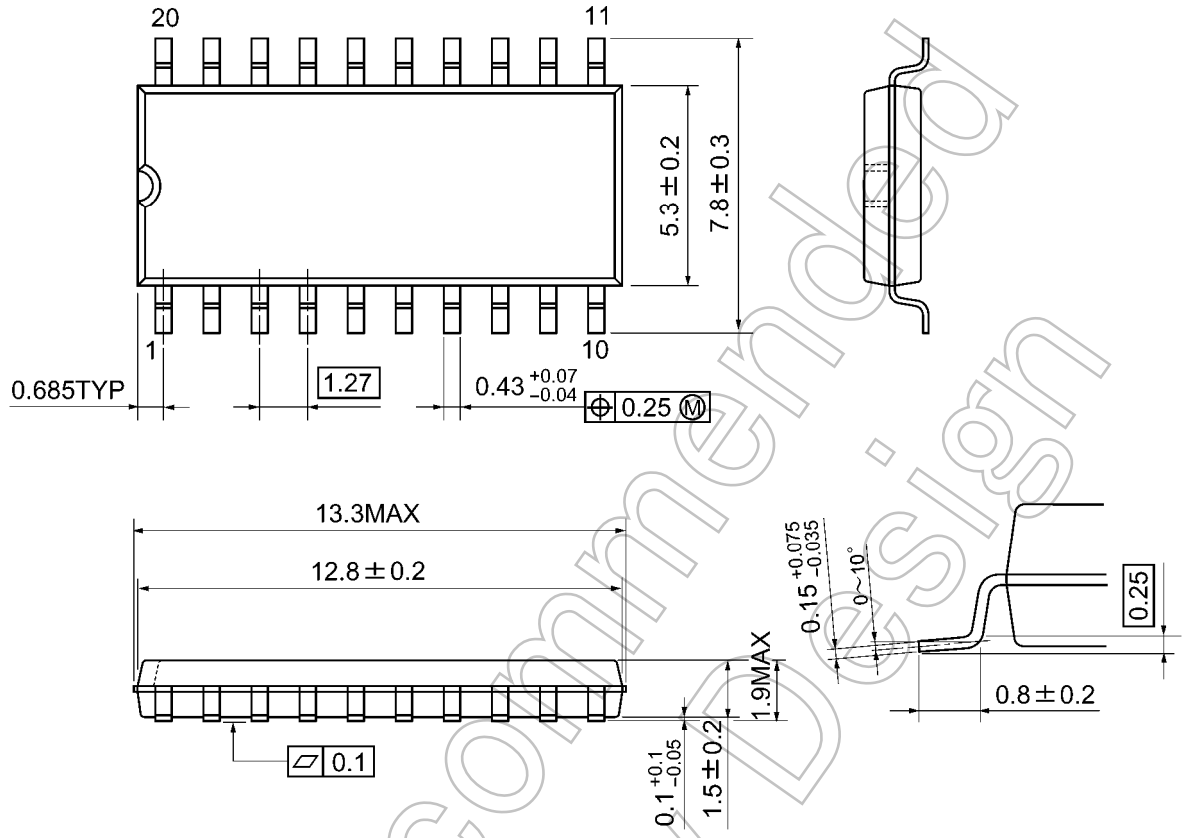
Package Dimensions

SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

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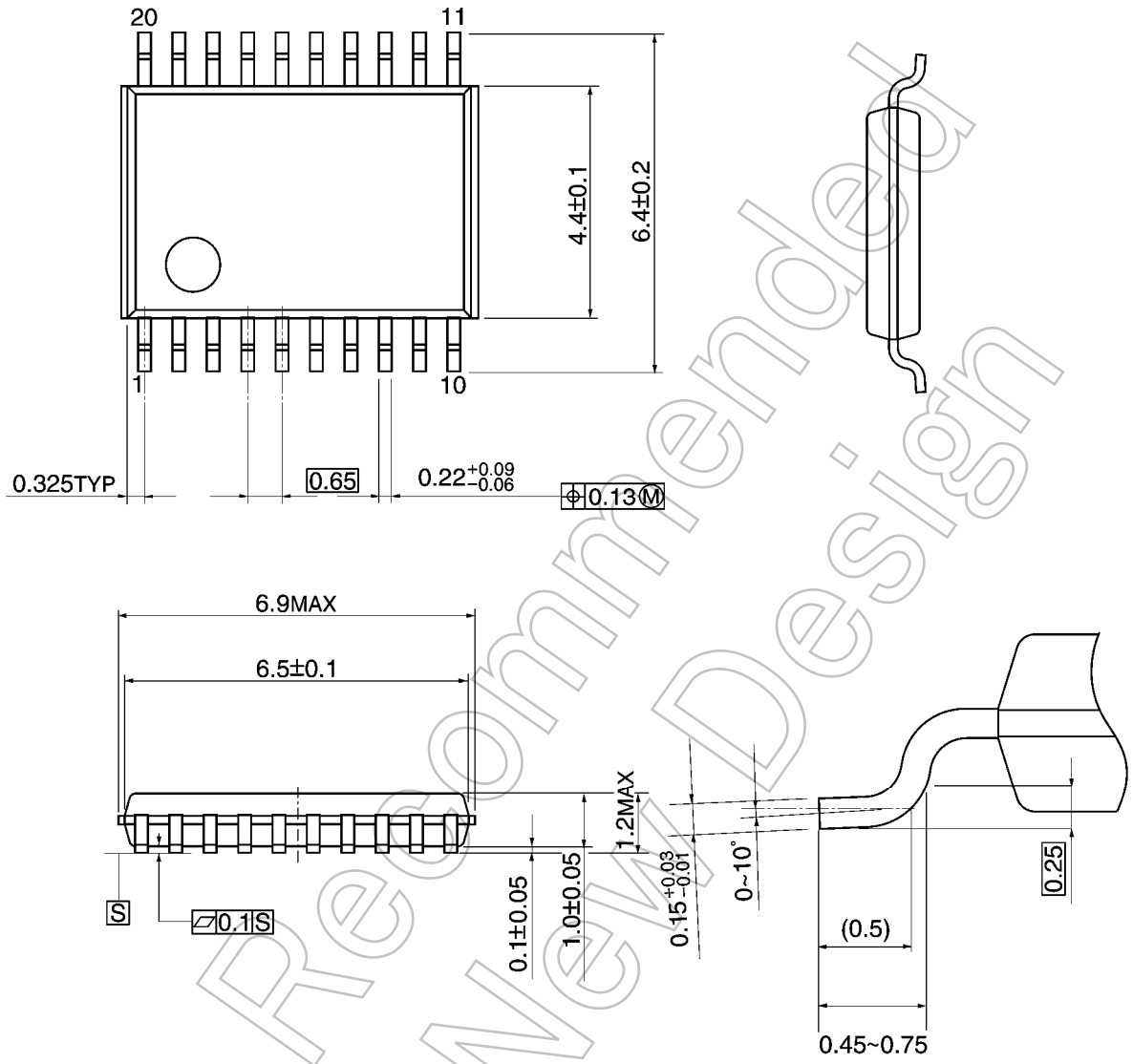
Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm



Weight: 0.08 g (typ.)

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