

# TC74ACT112P, TC74ACT112F

## Dual J-K Flip Flop with Preset and Clear

The TC74ACT112 is an advanced high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

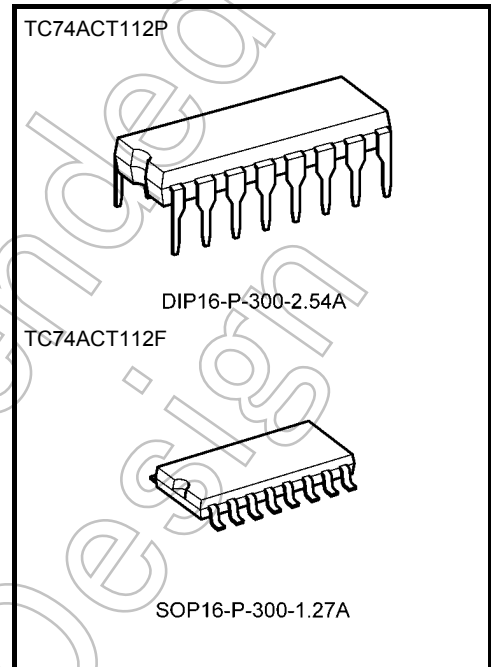
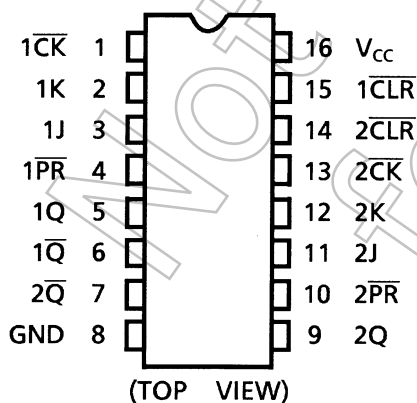
In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{max} = 175 \text{ MHz (typ.) at } V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V (max)}$   
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F112

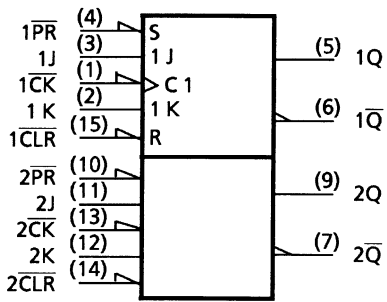
### Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production  
1989-11

**IEC Logic Symbol**

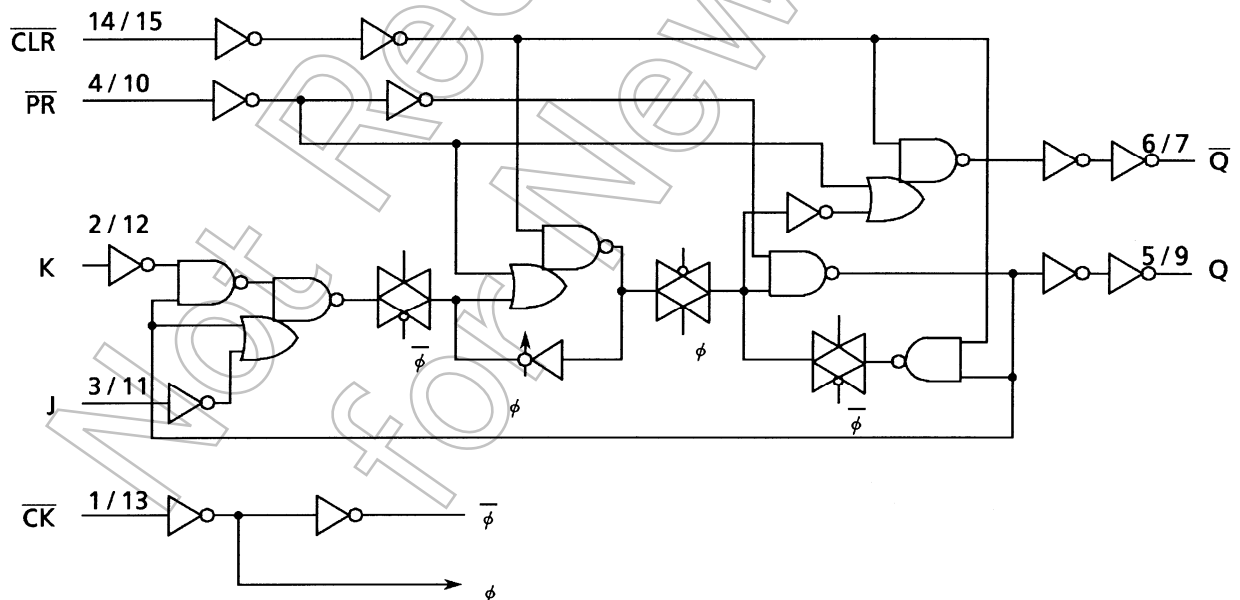


**Truth Table**

Inputs					Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	J	K	$\overline{\text{CK}}$	Q	$\overline{\text{Q}}$	
L	H	X	X	X	L	H	Clear
H	L	X	X	X	H	L	Preset
L	L	X	X	X	H	H	
H	H	L	L	$\downarrow$	$Q_n$	$\overline{Q}_n$	No Change
H	H	L	H	$\downarrow$	L	H	
H	H	H	L	$\downarrow$	H	L	
H	H	H	H	$\downarrow$	$\overline{Q}_n$	$Q_n$	Toggle
H	H	X	X	$\uparrow$	$Q_n$	$\overline{Q}_n$	No Change

X: Don't care

**System Diagram**



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied up to 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.5	4.4	4.5	—	4.4	—	V
			I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—	
			I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C	Ta = -40 to 85°C	Unit	
			V <sub>CC</sub> (V)	Limit		Limit
Minimum pulse width (CK)	t <sub>w</sub> (L) t <sub>w</sub> (H)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width (CLR, PR)	t <sub>w</sub> (L)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time	t <sub>s</sub>	—	5.0 ± 0.5	5.0	5.0	ns
Minimum hold time	t <sub>h</sub>	—	5.0 ± 0.5	1.0	1.0	ns
Minimum removal time (CLR, PR)	t <sub>rem</sub>	—	5.0 ± 0.5	3.0	3.0	ns

### AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \text{ } \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			VCC (V)	Min	Typ.	Max	Min		Max
Propagation delay time ( $\overline{CK} - Q$ , $\overline{Q}$ )	$t_{pLH}$	—	5.0 ± 0.5	—	6.4	10.0	1.0	11.5	ns
	$t_{pHL}$								
Propagation delay time ( $\overline{CLR}$ , $\overline{PR} - Q$ , $\overline{Q}$ )	$t_{pLH}$	—	5.0 ± 0.5	—	6.8	10.5	1.0	12.0	ns
	$t_{pHL}$								
Maximum clock frequency	$f_{max}$	—	5.0 ± 0.5	85	100	—	85	—	MHz
Input capacitance	$C_{IN}$	—	—	—	5	10	—	10	pF
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	—	32	—	—	—	pF

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

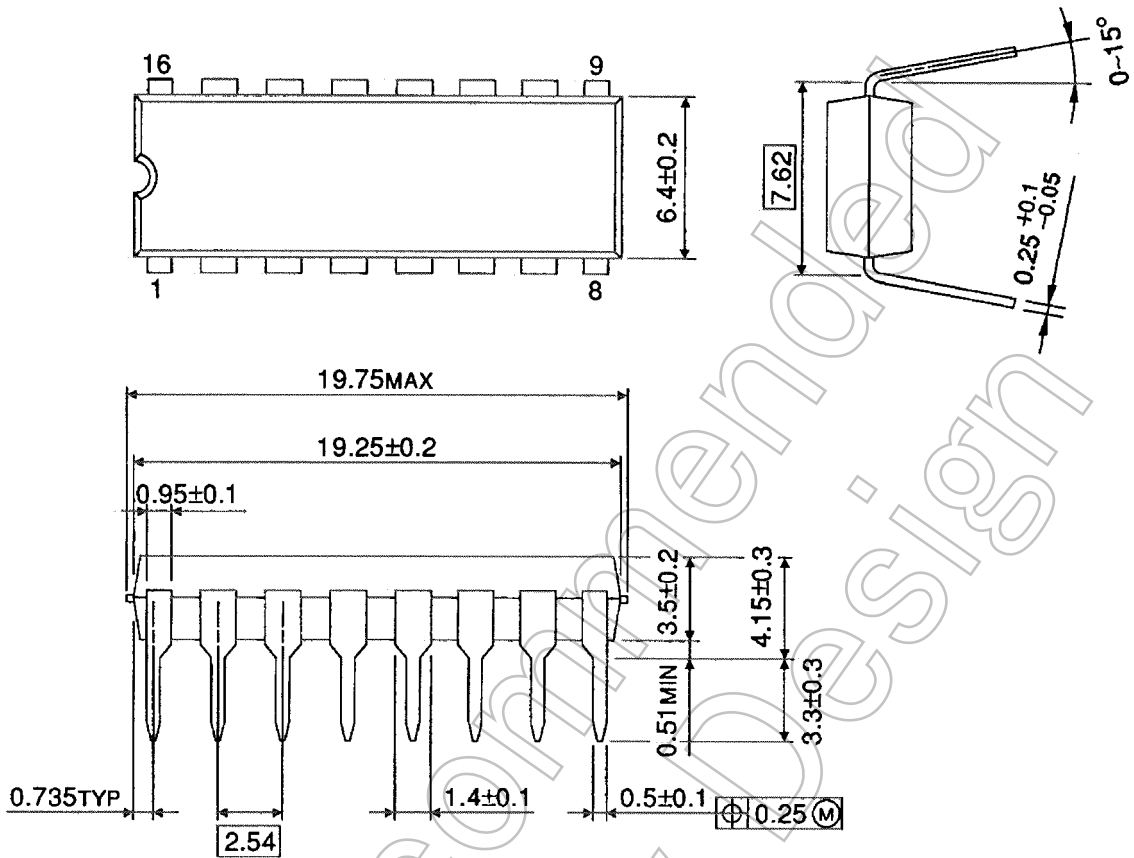
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

Not Recommended for New Design

**Package Dimensions**

DIP16-P-300-2.54A

Unit : mm



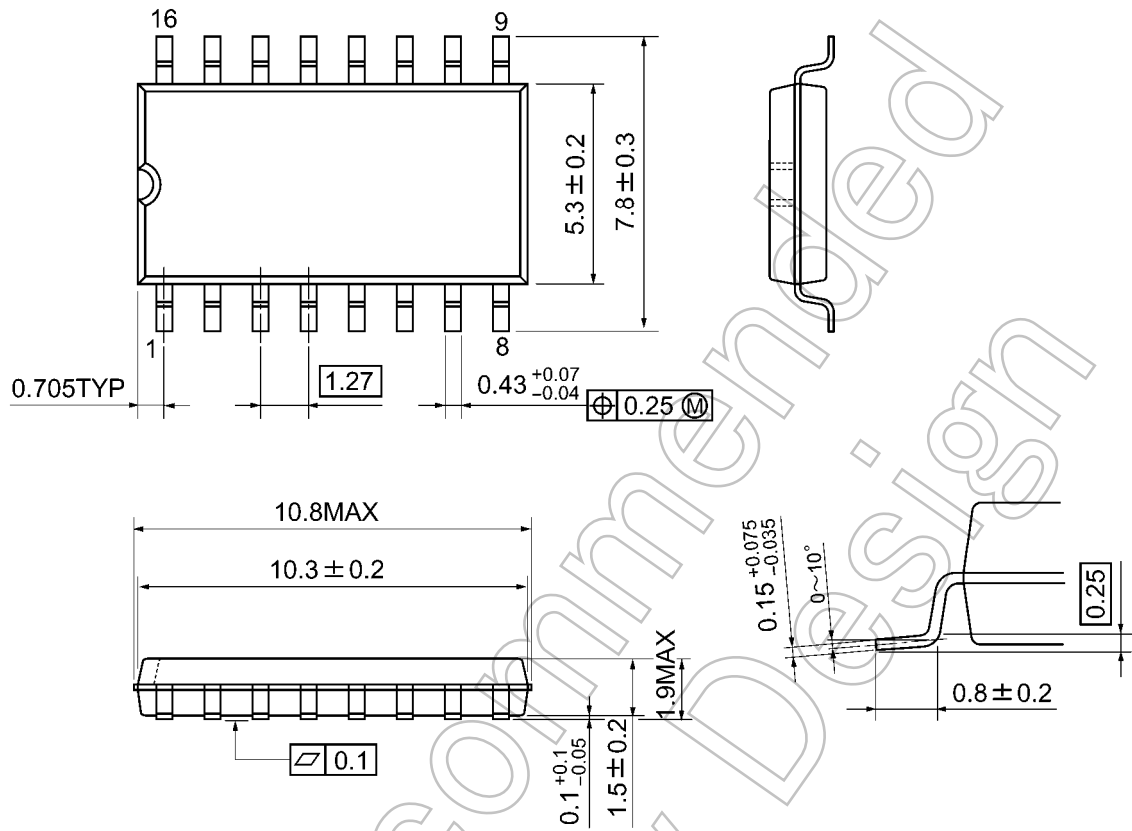
Weight: 1.00 g (typ.)

Not Recommended for New Design

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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