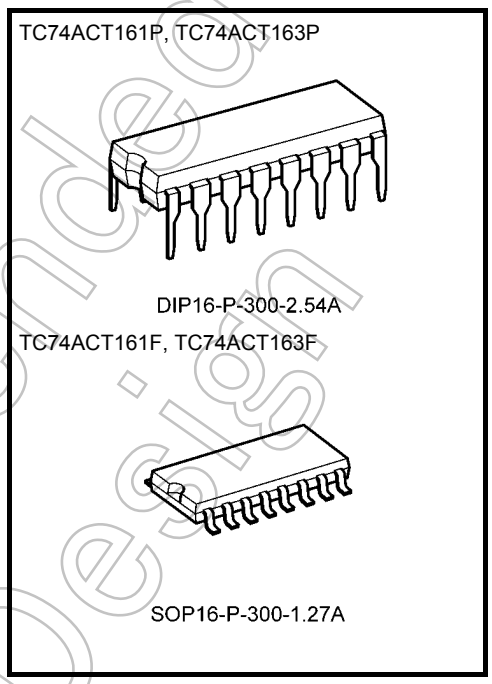
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74ACT161P, TC74ACT161F
TC74ACT163P, TC74ACT163F

Synchronous Presettable 4-Bit Binary Counter

TC74ACT161P/F/FN Asynchronous Clear

TC74ACT163P/F/FN Synchronous Clear



Weight
DIP16-P-300-2.54A : 1.00 g (typ.)
SOP16-P-300-1.27A : 0.18 g (typ.)

The TC74ACT161 and T163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The CK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ inputs are active on low logic level.

Presetting of these IC's is synchronous to the rising edge of CK.

The clear function of the TC74ACT163 is synchronous to CK, while the TC74ACT161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

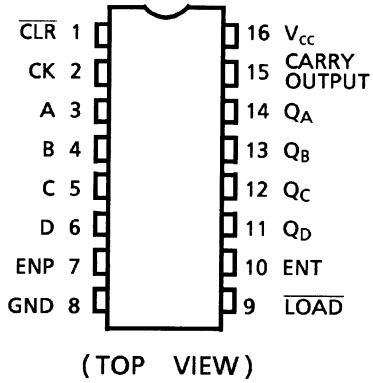
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} = 110 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- Compatible with TTL outputs: V_{IL} = 0.8 V (max)
  V_{IH} = 2.0 V (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F161/163

Start of commercial production
1989-11

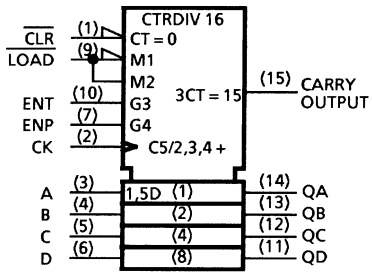
Pin Assignment



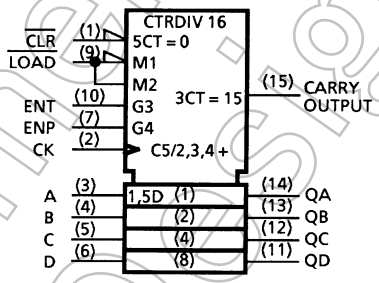
(TOP VIEW)

IEC Logic Symbol

TC74ACT161



TC74ACT163



Truth Table

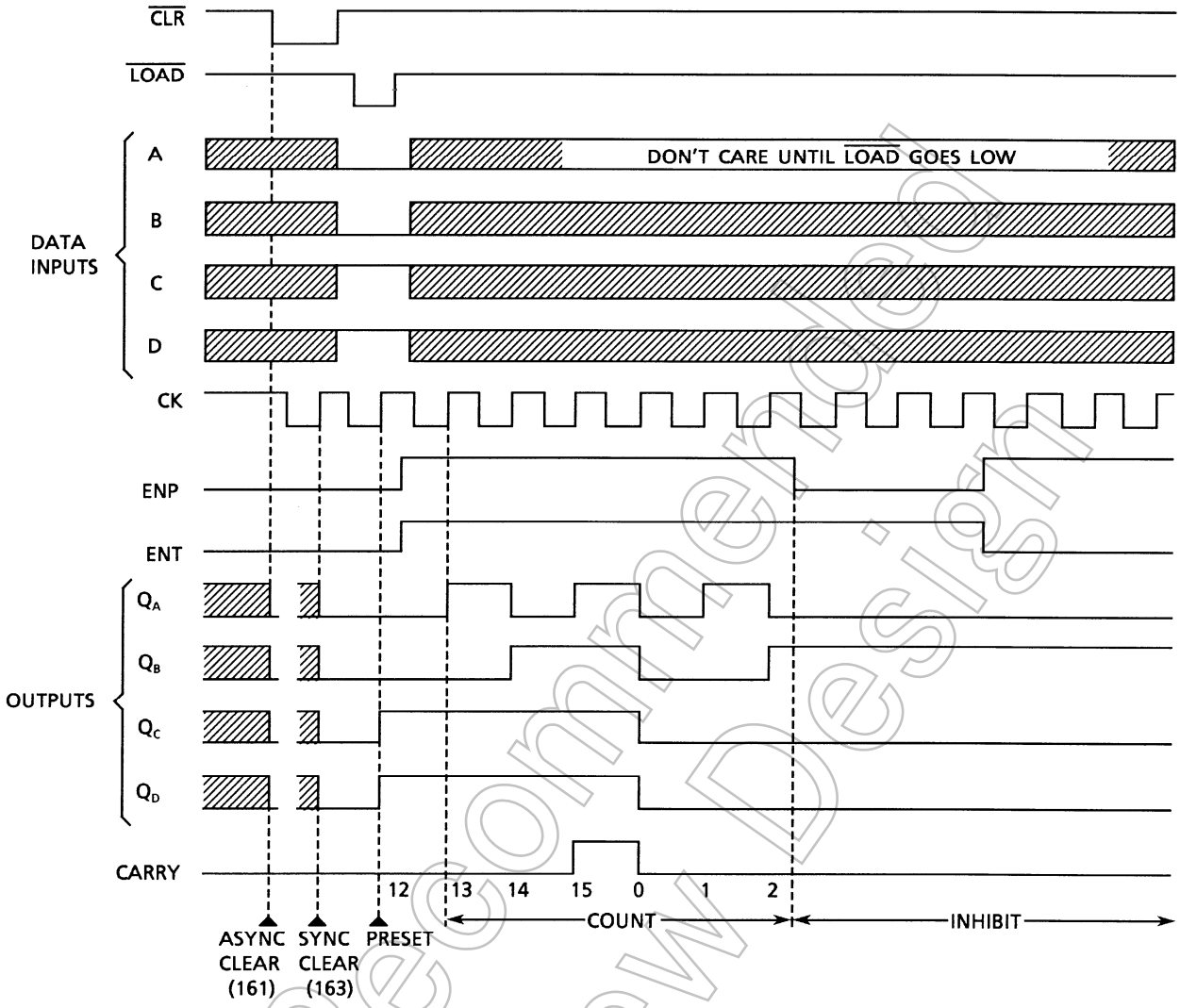
Inputs							Outputs				Function
$\overline{CLR}$ (161)	$\overline{CLR}$ (163)	$\overline{LOAD}$	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X	↑	L	L	L	L	Reset to “0”
H	H	L	X	X	↑	↑	A	B	C	D	Preset Data
H	H	H	X	L	↑	↑	No Change				No Count
H	H	H	L	X	↑	↑	No Change				No Count
H	H	H	H	H	↑	↑	Count Up				Count
H	X	X	X	X	↓	↓	No Change				No Count

X: Don’t care

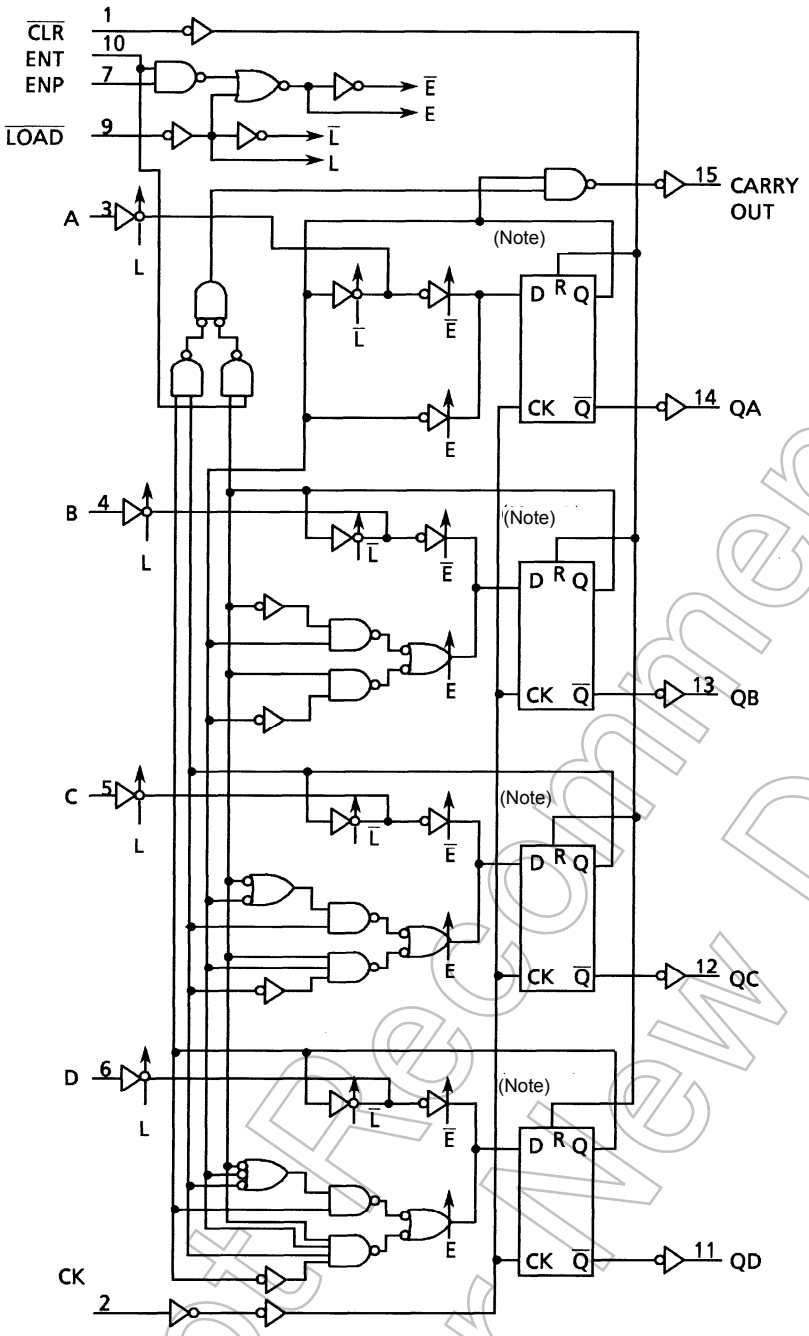
A, B, C, D: Logic level of data inputs

Carry: Carry = ENT·QA·QB·QC·QD

Timing Chart



System Diagram (Note)



Note: Truth table of internal F/F

TC74ACT161					TC74ACT163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	X	↑	L	H	L
X	↓	L	No Change		X	↓	L	No Change	

X: Don't care

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±125	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −24 mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA
	I_C	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width (CK)	$t_{W(L)}$ $t_{W(H)}$	Figure 1	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width ($\overline{CLR}$) (Note1)	$t_{W(L)}$	Figure 4	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width ($\overline{LOAD}$, ENP, ENT)	t_s	Figure 2, Figure 3	5.0 ± 0.5	6.0	6.0	ns
Minimum set-up time (A, B, C, D)	t_s	Figure 2	5.0 ± 0.5	4.0	4.0	ns
Minimum set-up time ($\overline{CLR}$) (Note 2)	t_s	Figure 5	5.0 ± 0.5	3.0	3.0	ns
Minimum hold time ($\overline{LOAD}$, ENP, ENT)	t_h	Figure 2, Figure 3	5.0 ± 0.5	1.0	1.0	ns
Minimum hold time (A, B, C, D)	t_h	Figure 2	5.0 ± 0.5	2.0	2.0	ns
Minimum hold time ($\overline{CLR}$) (Note 2)	t_h	Figure 5	5.0 ± 0.5	2.0	2.0	ns
Minimum removal time ($\overline{CLR}$) (Note 1)	t_{rem}	Figure 4	5.0 ± 0.5	1.0	1.0	ns

Note 1: For TC74ACT161 only

Note 2: For TC74ACT163 only

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	Figure 1	5.0 ± 0.5	—	7.2	10.5	1.0	12.0	ns
Propagation delay time (CK-CARRY, count mode)	t_{pLH} t_{pHL}	Figure 1	5.0 ± 0.5	—	8.5	13.0	1.0	15.0	ns
Propagation delay time (CK-CARRY, preset mode)	t_{pLH} t_{pHL}	Figure 2	5.0 ± 0.5	—	9.7	15.0	1.0	17.0	ns
Propagation delay time (ENT-CARRY)	t_{pLH} t_{pHL}	Figure 6	5.0 ± 0.5	—	6.6	10.0	1.0	11.5	ns
Propagation delay time (Note 2) ($\overline{CLR}$ -Q)	t_{pHL}	Figure 4	5.0 ± 0.5	—	6.3	10.0	1.0	11.5	ns
Propagation delay time (Note 2) ($\overline{CLR}$ -CARRY)	t_{pHL}	Figure 4	5.0 ± 0.5	—	7.7	12.3	1.0	14.0	ns
Maximum clock frequency	f_{max}	—	5.0 ± 0.5	70	100	—	60	—	MHz
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note 1)	—		—	32	—	—	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and ΔI_{CC} which is obtained from the following formula:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16}\right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.

f_{CK} is the input frequency of the CK.

Note 2: for TC74ACT161 only

Switching Characteristics Test Waveform

Count Mode

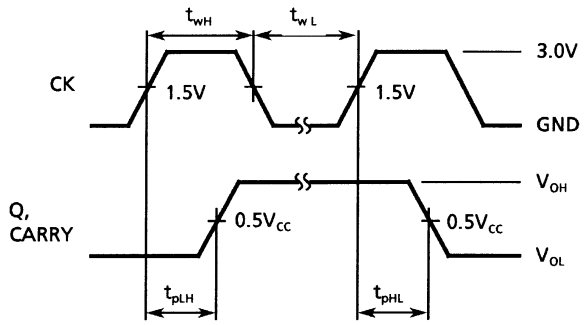


Figure 1

Preset Mode

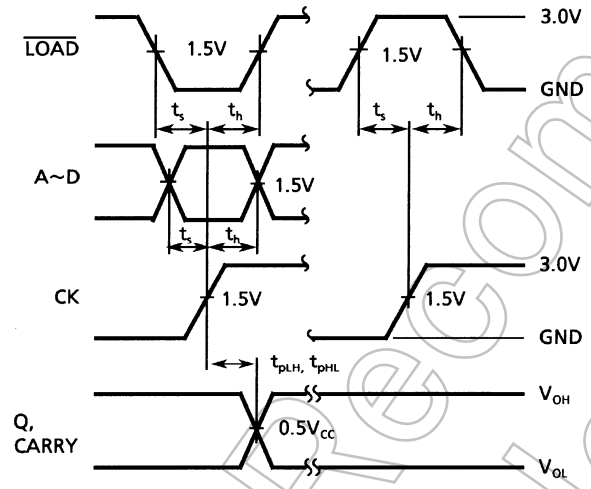


Figure 2

Count Enable Mode

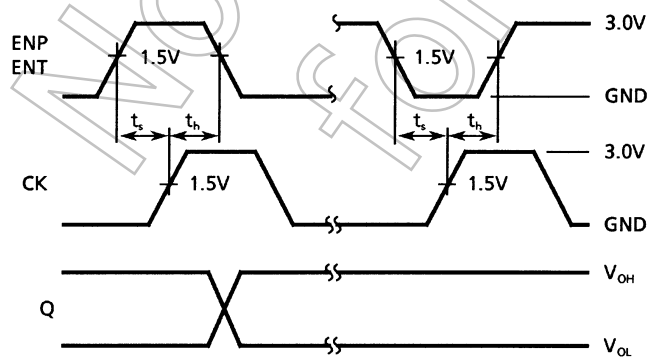


Figure 3

Clear Mode (TC74ACT161)

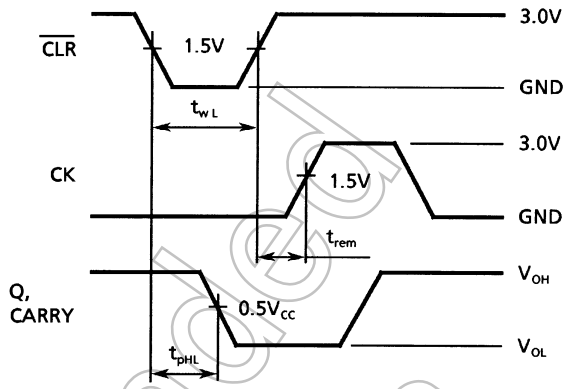


Figure 4

Clear Mode (TC74ACT163)

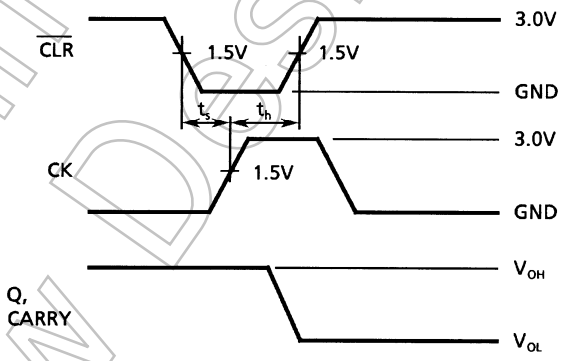


Figure 5

Cascade Mode (fix maximum count)

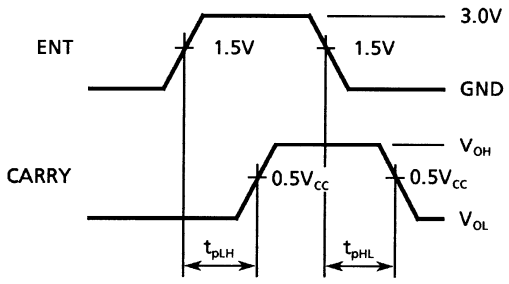
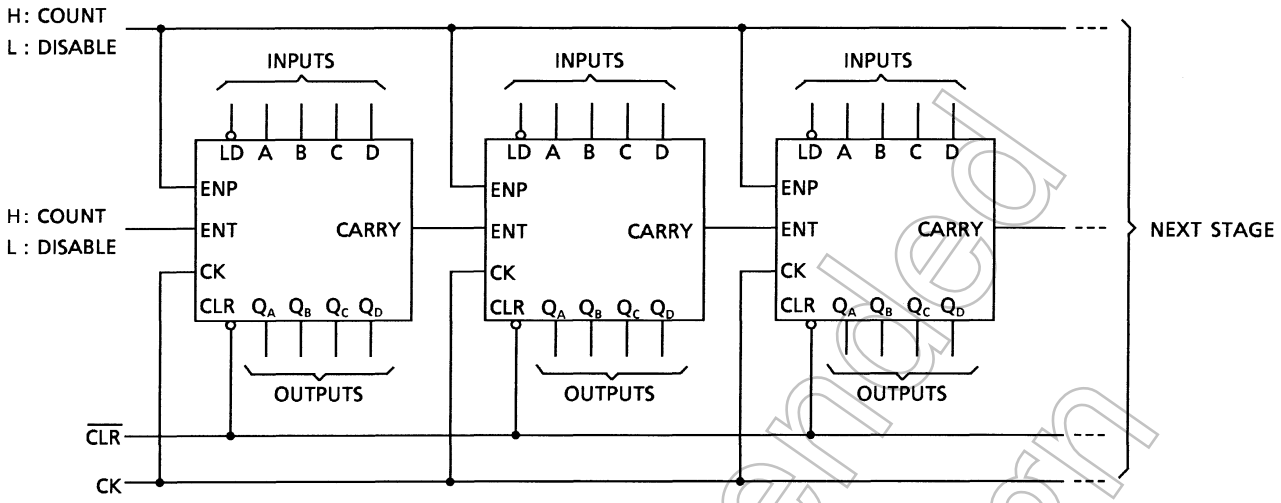


Figure 6

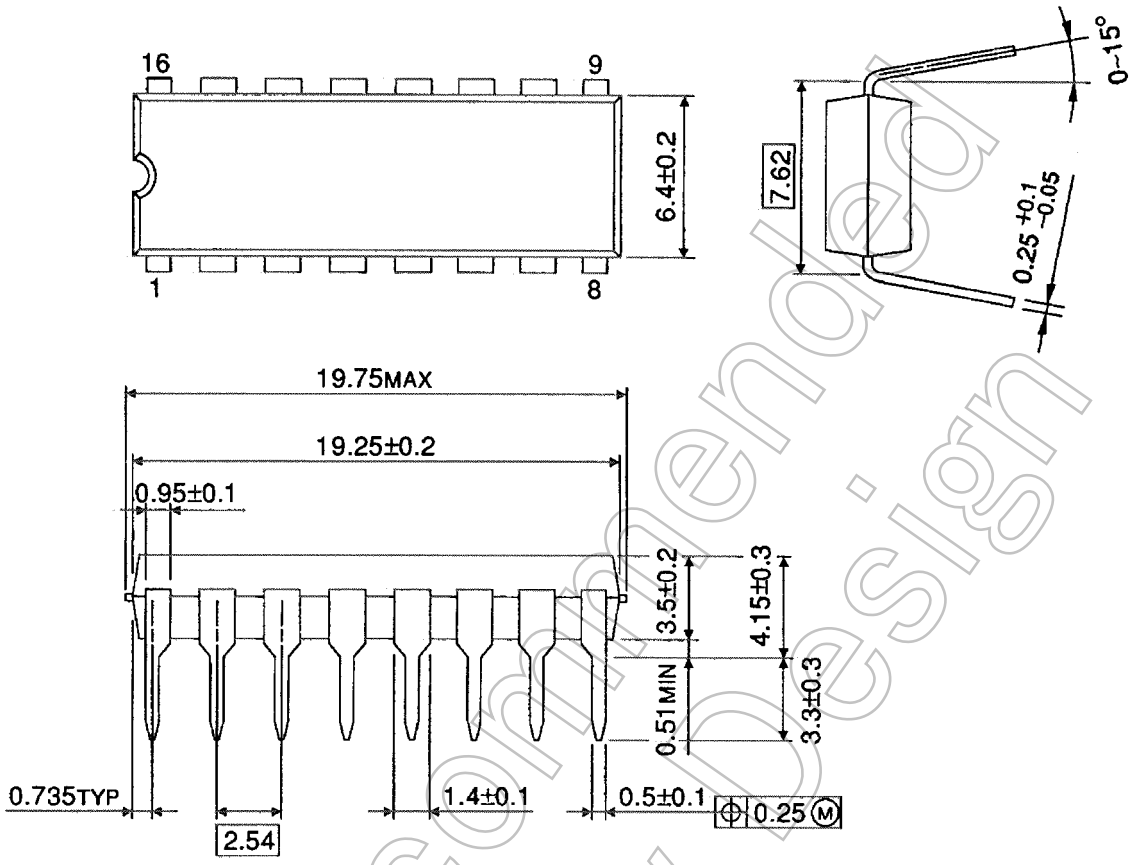
Typical Application

Parallel Carry N-Bit Counter



Package Dimensions

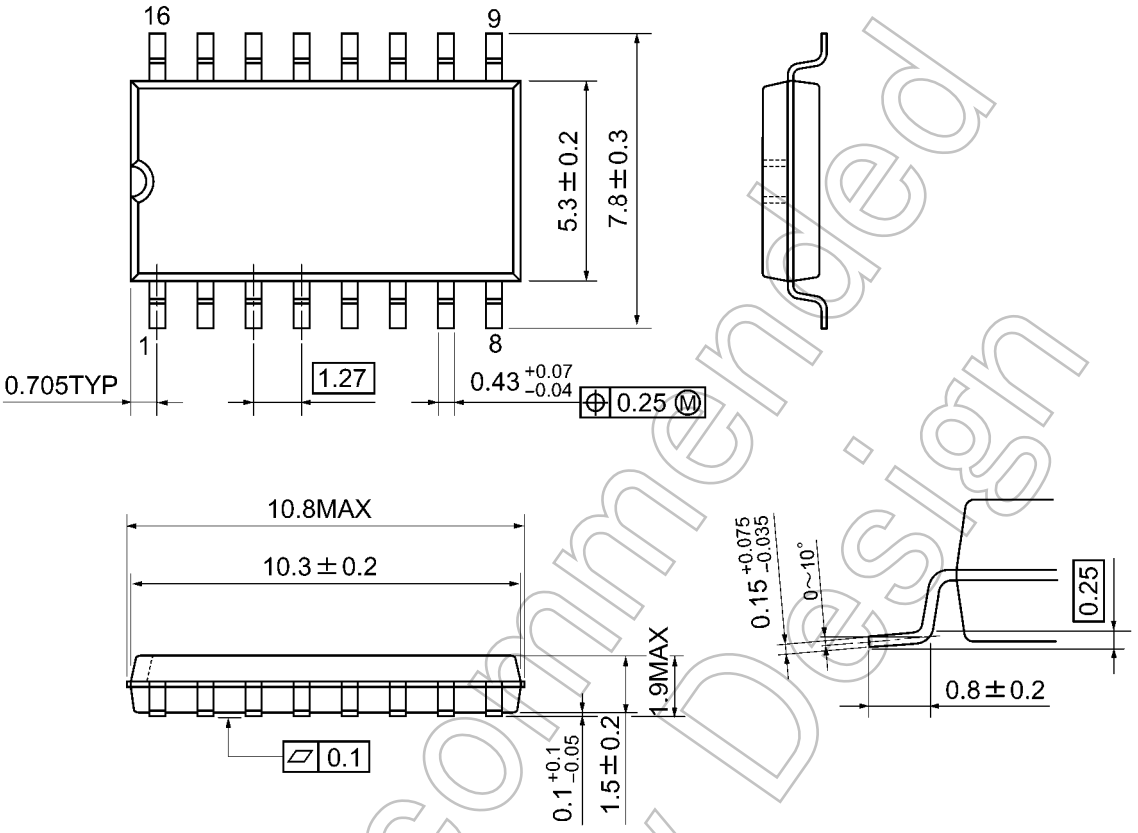
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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