TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74ACT86P, TC74ACT86F

## Quad Exclusive OR Gate

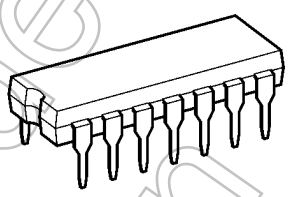
The TC74ACT86 is an advanced high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate and double-layer metal wiring $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. The internal circuit is includes on output buffer, which provide high noise immunity and stable output.

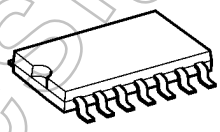
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74ACT86P



DIP14-P-300-2.54

TC74ACT86F



SOP14-P-300-1.27A

Weight

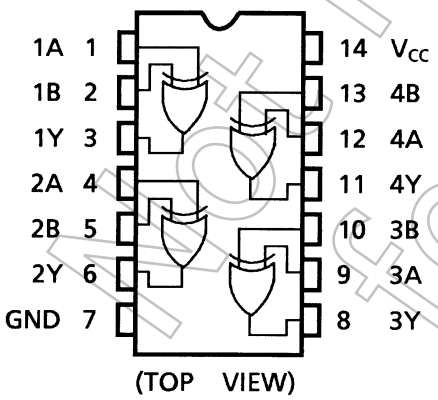
DIP14-P-300-2.54 : 0.96 g (typ.)

SOP14-P-300-1.27A : 0.18 g (typ.)

### Features

- High speed: $t_{pd}$ = 5.0 ns (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 4 μA (max) at Ta = 25°C
- Compatible with TTL outputs: $V_{IL}$ = 0.8 V (max)
  $V_{IH}$ = 2.0 V (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F86

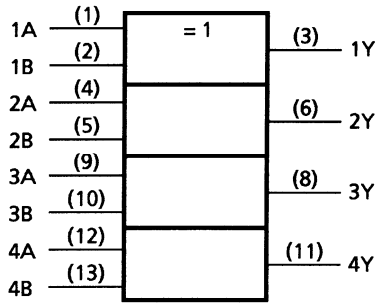
### Pin Assignment






Start of commercial production
1988-10

## IEC Logic Symbol




## Truth Table

| A | B | Y |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

## Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | ±20 | mA |
| Output diode current | $I_{OK}$ | ±50 | mA |
| DC output current | $I_{OUT}$ | ±50 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±100 | mA |
| Power dissipation | $P_D$ | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CC}$ or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 4.5 to 5.5 | 2.0 | — | — | 2.0 | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | $I_{OH}$ = −24 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | | | $I_{OH}$ = −75 mA (Note) | 5.5 | — | — | — | 3.85 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | $I_{OL}$ = 24 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 75 mA (Note) | 5.5 | — | — | — | — | 1.65 | |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |
| | $I_C$ | Per input: $V_{IN}$ = 3.4 V<br>Other input: $V_{CC}$ or GND | | 5.5 | — | — | 1.35 | — | 1.5 | mA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### AC Characteristics ($C_L$ = 50 pF, $R_L$ = 500 Ω, input: $t_r$ = $t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{pLH}$<br>$t_{pHL}$ | — | 5.0 ± 0.5 | — | 5.7 | 10.5 | 1.0 | 12.0 | ns |
| Input capacitance | $C_{IN}$ | — | | — | 5 | 10 | — | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ (Note) | — | | — | 23 | — | — | — | pF |

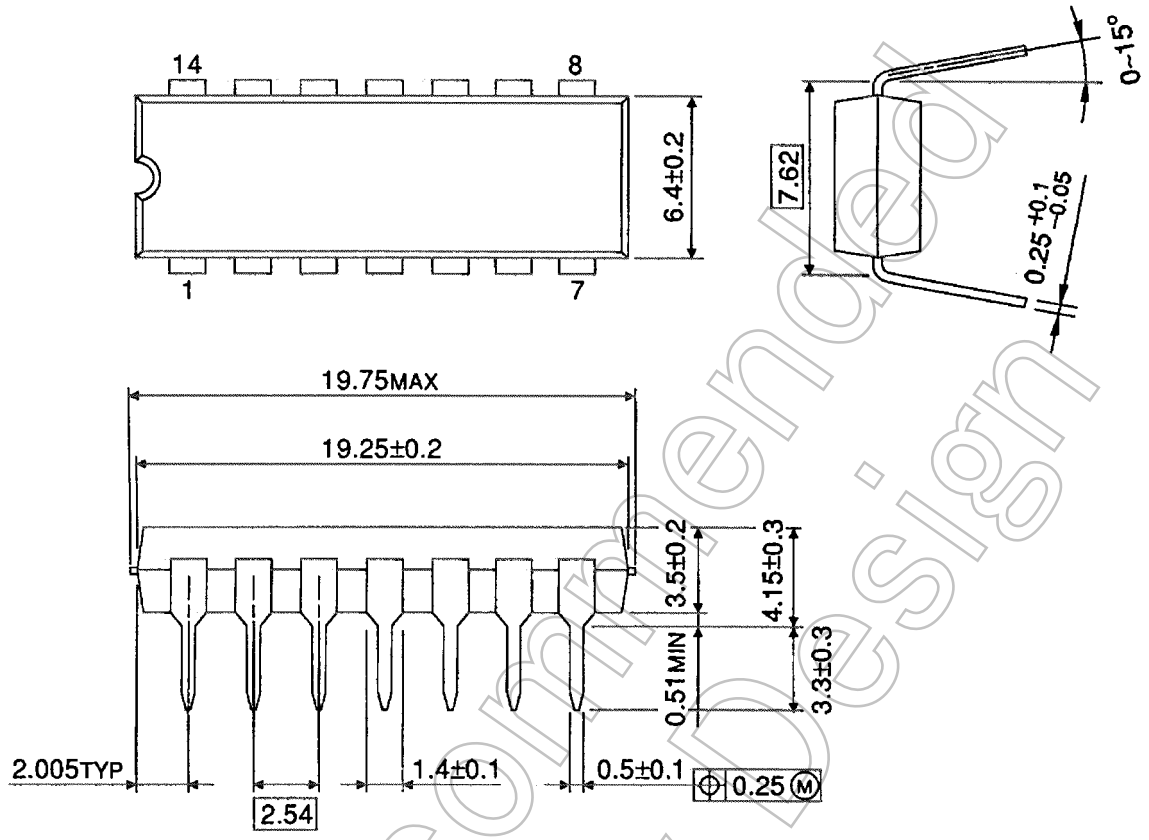
Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC}$ (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per gate)

## Package Dimensions

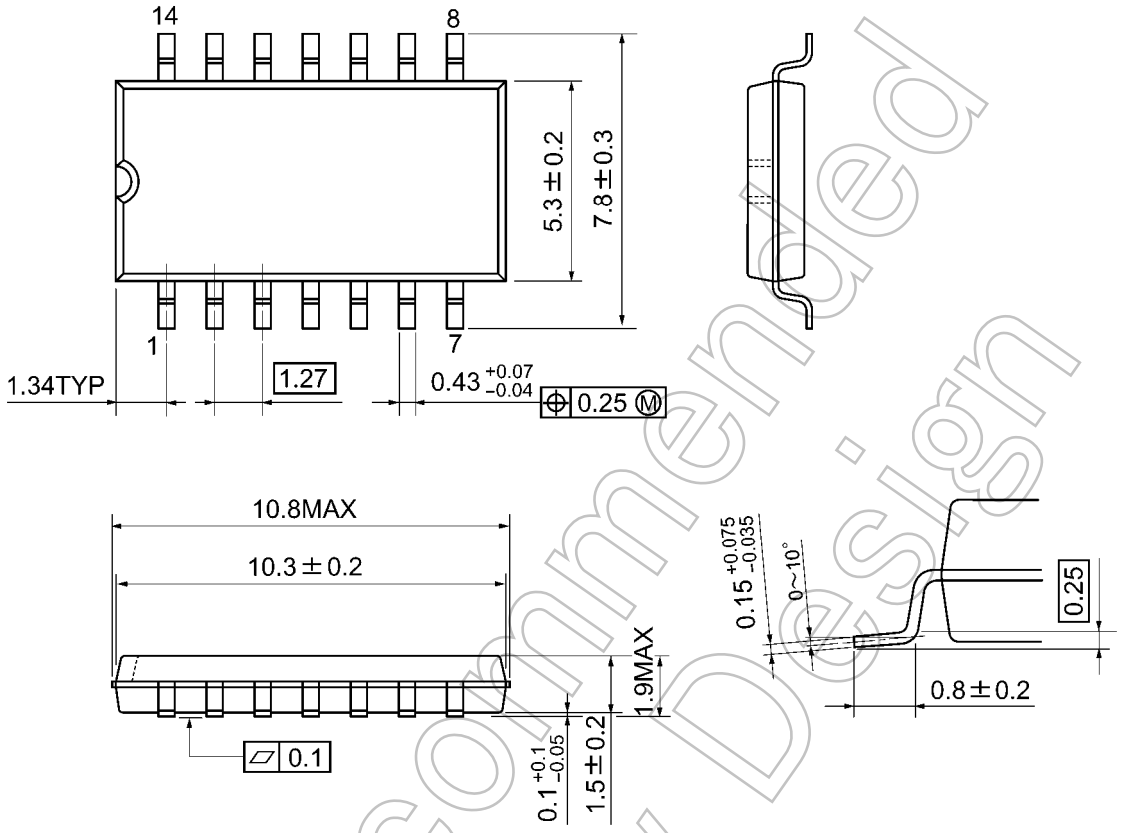
DIP14-P-300-2.54 Unit : mm




Weight: 0.96 g (typ.)

## Package Dimensions

SOP14-P-300-1.27A Unit: mm




Weight: 0.18 g (typ.)

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