

TC74HC112AP, TC74HC112AF

Dual J-K Flip Flop with Preset and Clear

The TC74HC112A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

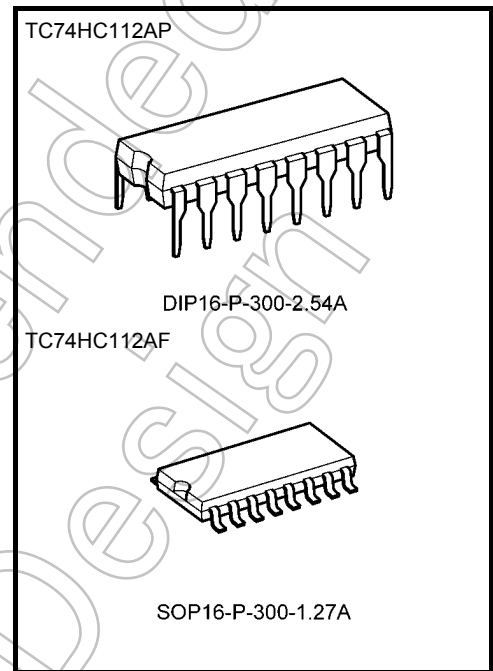
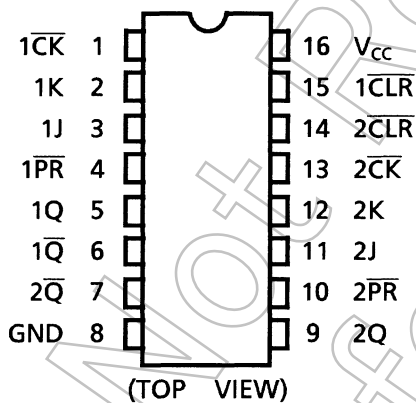
$\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the clock and are activated by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{\text{max}} = 67 \text{ MHz (typ.) at } V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 2 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA (min)}$
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: $V_{\text{CC}} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS112

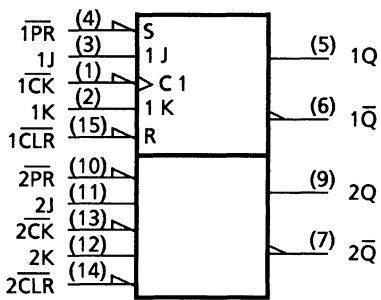
Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production
1988-05

IEC Logic Symbol

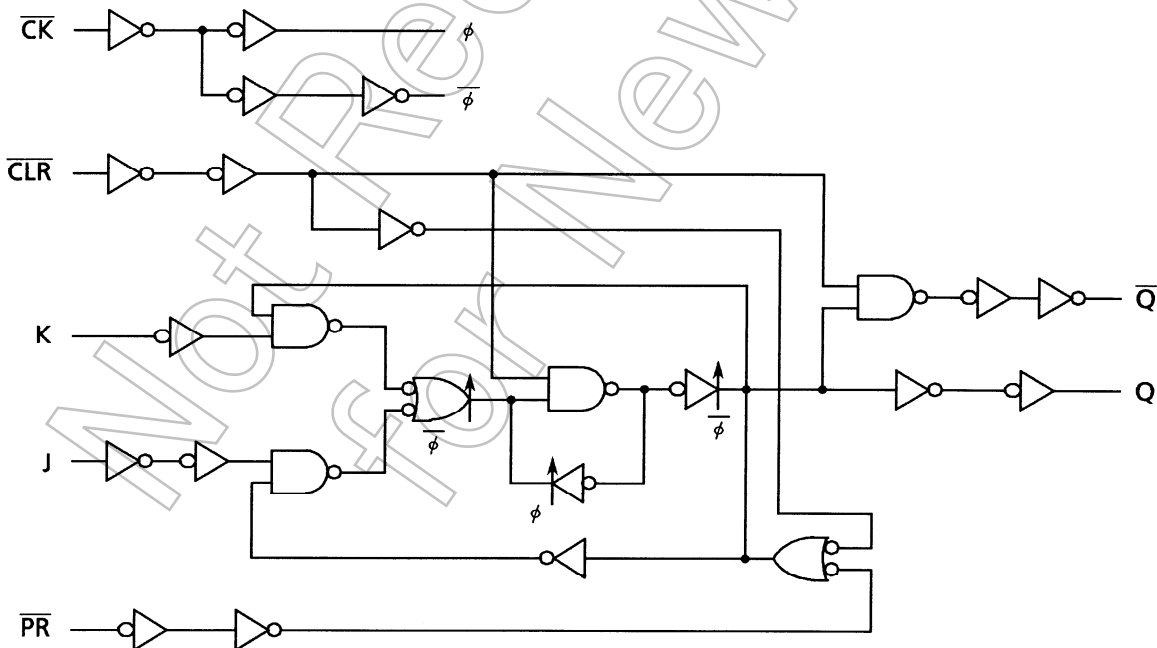


Truth Table

Inputs					Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	J	K	$\overline{\text{CK}}$	Q	$\overline{\text{Q}}$	
L	H	X	X	X	L	H	Clear
H	L	X	X	X	H	L	Preset
L	L	X	X	X	H	H	
H	H	L	L	\downarrow	Q_n	\overline{Q}_n	No Change
H	H	L	H	\downarrow	L	H	
H	H	H	L	\downarrow	H	L	
H	H	H	H	\downarrow	\overline{Q}_n	Q_n	Toggle
H	H	X	X	\uparrow	Q_n	\overline{Q}_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/ $^{\circ}\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—	
			I _{OH} = -5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I _{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	2.0	—	20.0	μA

Not Recommended for New

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit	
			V _{CC} (V)	Typ.	Limit		Limit
Minimum pulse width ($\overline{\text{CK}}$)	$t_W(L)$ $t_W(H)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	$t_W(L)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t_{rem}	—	2.0	—	50	60	ns
			4.5	—	10	12	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	4	MHz
			4.5	—	30	24	
			6.0	—	34	28	

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH}	—	—	4	8	ns
	t_{THL}	—	—	4	8	
Propagation delay time ($\overline{\text{CK}} - Q$, \overline{Q})	t_{pLH}	—	—	13	21	ns
	t_{pHL}	—	—	13	21	
Propagation delay time ($\overline{\text{CLR}}$, $\overline{\text{PR}} - Q$, \overline{Q})	t_{pLH}	—	—	15	22	ns
	t_{pHL}	—	—	15	22	
Maximum clock frequency	f_{max}	—	32	67	—	MHz

AC Characteristics (C_L = 50 pF, input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	T _a = 25°C			T _a = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t _{TLH} t _{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (\overline{CK} -Q, \overline{Q})	t _{pLH} t _{pHL}	—	2.0	—	52	125	—	155	ns
			4.5	—	16	25	—	31	
			6.0	—	14	21	—	26	
Propagation delay time (\overline{CLR} , \overline{PR} -Q, \overline{Q})	t _{pLH} t _{pHL}	—	2.0	—	68	135	—	170	ns
			4.5	—	17	27	—	34	
			6.0	—	15	23	—	29	
Maximum clock frequency	f _{max}	—	2.0	6	19	—	4	—	MHz
			4.5	30	63	—	24	—	
			6.0	34	71	—	28	—	
Input capacitance	C _{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C _{PD} (Note)	—	—	—	35	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

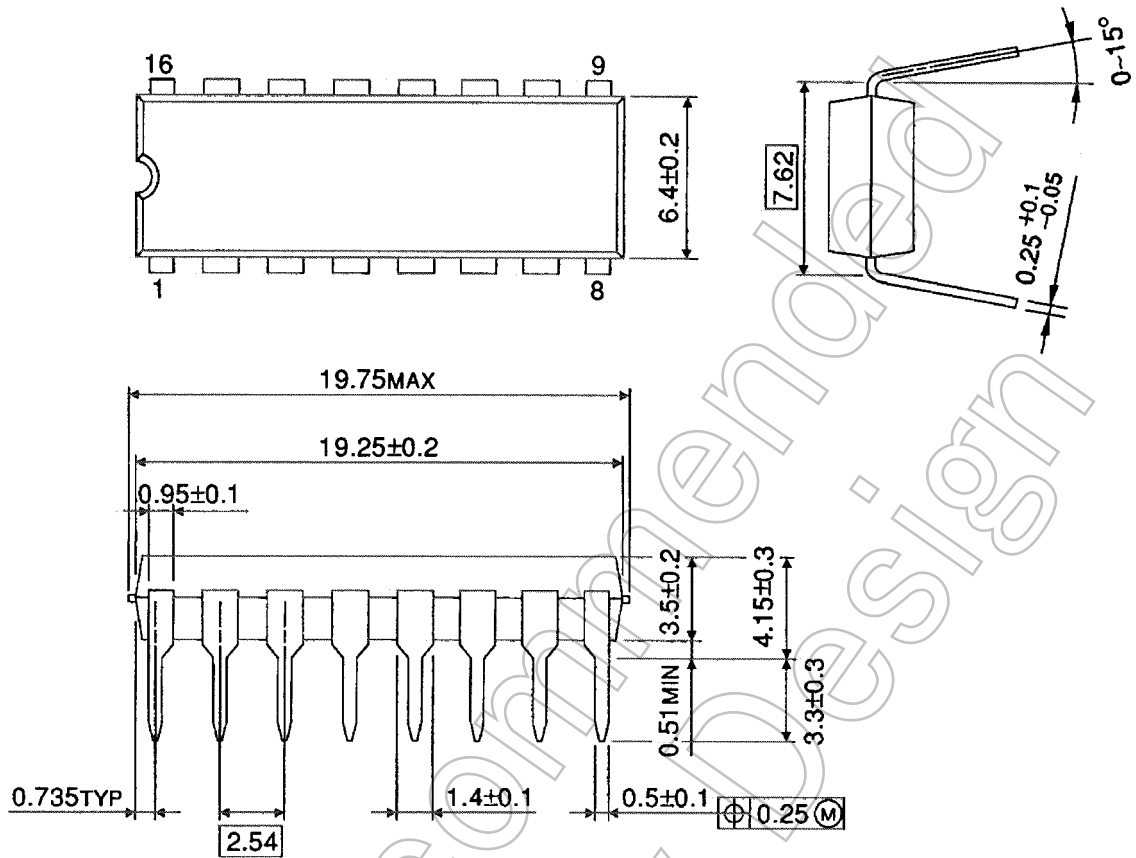
$$I_{CC} \text{ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

Not Recommended for New Design

Package Dimensions

DIP16-P-300-2.54A

Unit : mm



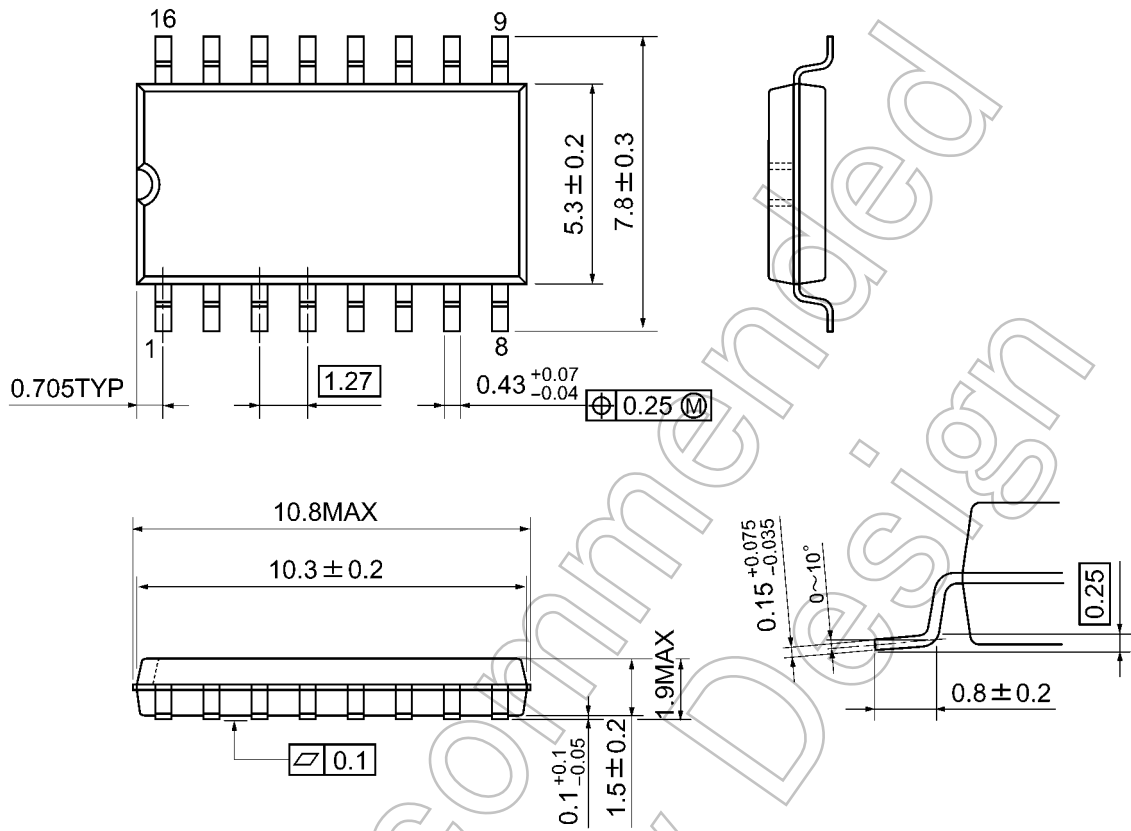
Weight: 1.00 g (typ.)

Not Recommended for New Design

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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