

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74HC161AP, TC74HC161AF TC74HC163AP, TC74HC163AF

### Synchronous Presetable 4-Bit Counter

TC74HC161AP/AF Binary, Asynchronous Clear

TC74HC163AP/AF Binary, Synchronous Clear

The TC74HC161A and 163A are high speed CMOS BINARY PRESETTABLE COUNTERS fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

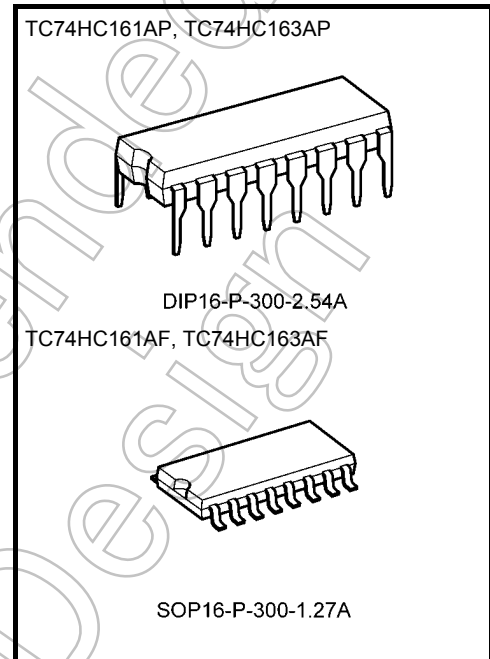
The CK input is active on the rising edge. Both  $\overline{\text{LOAD}}$  and  $\overline{\text{CLR}}$  inputs are active on low logic level.

Presetting of their IC's is synchronous to the rising edge of CK.

The clear function of the TC74HC163A is synchronous to CK, while the TC74HC161A is cleared asynchronously.

Two enable inputs (ENP and ENT) and CO are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



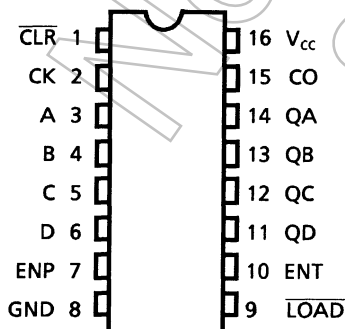
### Features

- High speed:  $f_{\text{max}} = 63 \text{ MHz (typ.) at } V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC}} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS161, 163

Weight

DIP16-P-300-2.54A : 1.00 g (typ.)  
SOP16-P-300-1.27A : 0.18 g (typ.)

### Pin Assignment

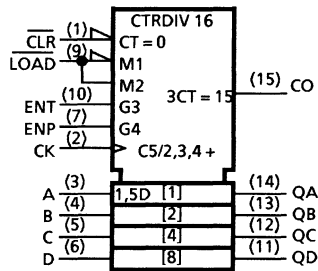


(TOP VIEW)

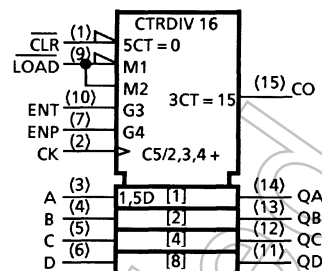
Start of commercial production  
1986-05

## IEC Logic Symbol

### TC74HC161A



### TC74HC163A



## Truth Table

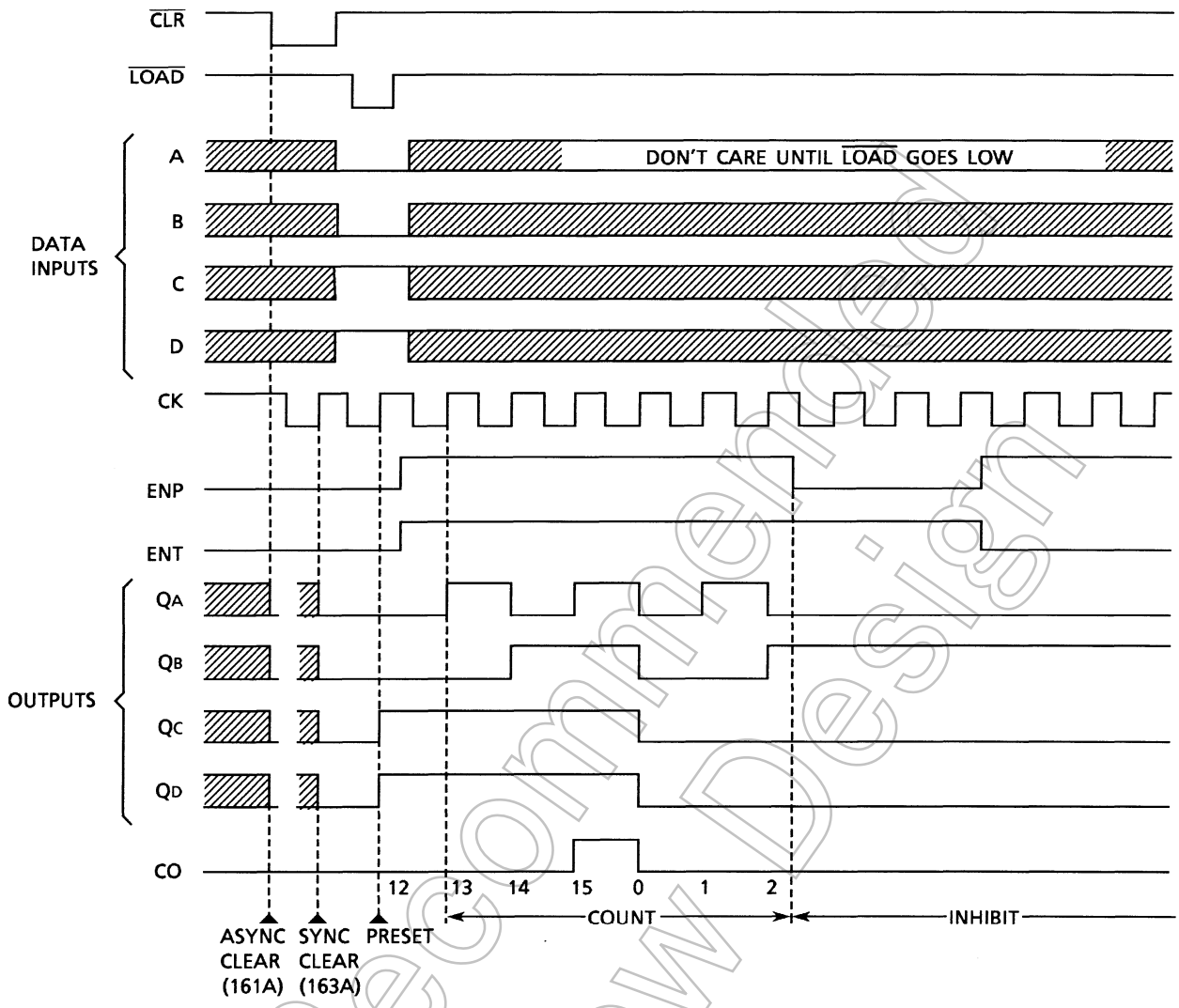
TC74HC161A					TC74HC163A					Outputs				Function
Inputs					Inputs					QA	QB	QC	QD	
$\overline{\text{CLR}}$	$\overline{\text{LD}}$	ENP	ENT	CK	$\overline{\text{CLR}}$	$\overline{\text{LD}}$	ENP	ENT	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	$\uparrow$	L	L	L	L	Reset to "0"
H	L	X	X	$\uparrow$	H	L	X	X	$\uparrow$	A	B	C	D	Preset Data
H	H	X	L	$\uparrow$	H	H	X	L	$\uparrow$	No Change				No Count
H	H	L	X	$\uparrow$	H	H	L	X	$\uparrow$	No Change				No Count
H	H	H	H	$\uparrow$	H	H	H	H	$\uparrow$	Count Up				Count
H	X	X	X	$\downarrow$	X	X	X	X	$\downarrow$	No Change				No Count

X: Don't care

A, B, C, D: Logic level of data inputs

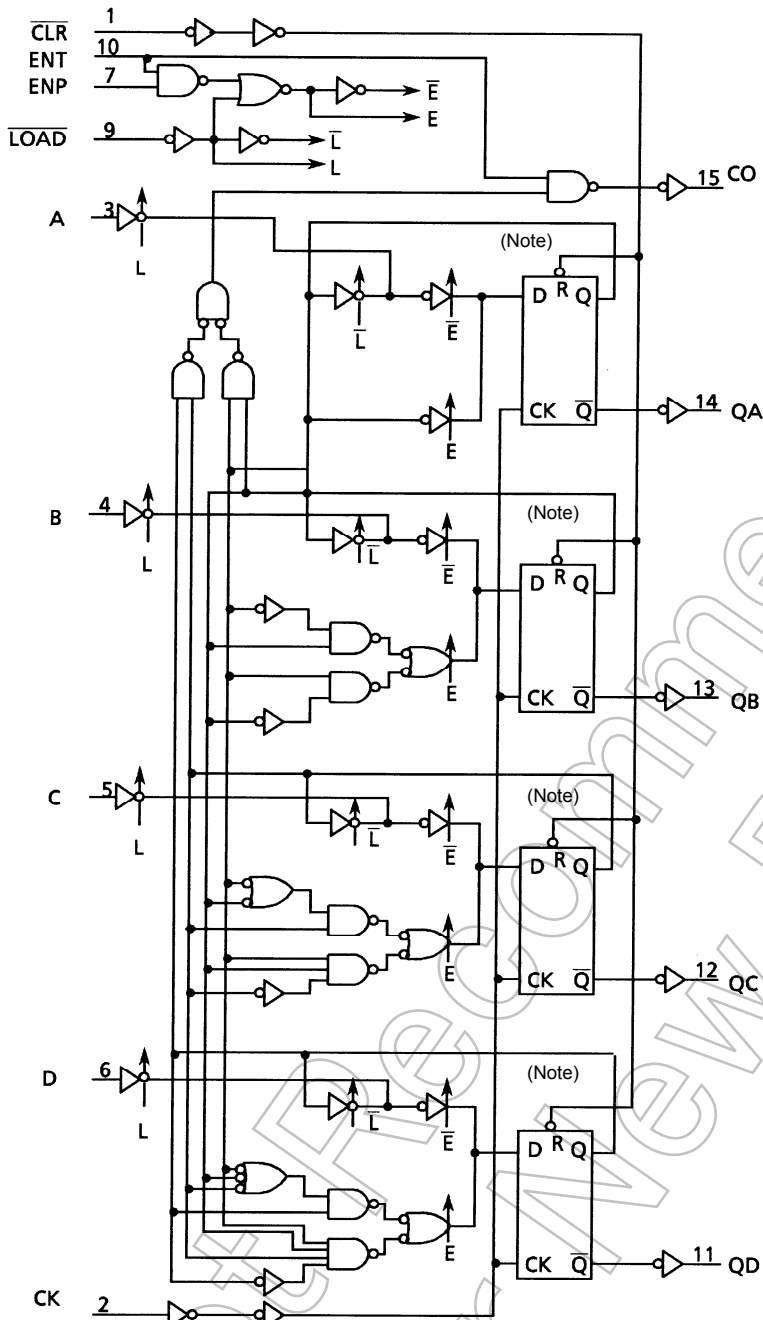
Carry: Carry = ENT · QA · QB · QC · QD

**Timing Chart**



Not Recommended for New Design

**System Diagram**



Note: Truth table of internal F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	L	L	H	X	$\uparrow$	L	L	H
L	$\uparrow$	H	L	H	L	$\uparrow$	H	L	H
H	$\uparrow$	H	H	L	H	$\uparrow$	H	H	L
X	$\downarrow$	H	No Change		L	$\downarrow$	H	No Change	

X: Don't care

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics**

**DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V	
				4.5	3.15	—	—	3.15	—		
				6.0	4.20	—	—	4.20	—		
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V	
				4.5	—	—	1.35	—	1.35		
				6.0	—	—	1.80	—	1.80		
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
				I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—	
					6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V
					4.5	—	0.0	0.1	—	0.1	
					6.0	—	0.1	0.1	—	0.1	
				I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33	
					6.0	—	0.18	0.26	—	0.33	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	μA	

Not Recommended for New

**Timing Requirements (input:  $t_r = t_f = 6$  ns)**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit	
			VCC (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	$t_W$ (H) $t_W$ (L)	Figure 1	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{CLR}}$ ) (Note 1)	$t_W$ (L)	Figure 4	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ( $\overline{\text{LOAD}}$ , ENP, ENT)	$t_s$	Figure 2, Figure 3	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (A, B, C, D)	$t_s$	Figure 2	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ( $\overline{\text{CLR}}$ ) (Note 2)	$t_s$	Figure 5	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	$t_h$	Figure 2, Figure 3, Figure 5	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ( $\overline{\text{CLR}}$ ) (Note 1)	$t_{rem}$	Figure 4	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

Note 1: For TC74HC161A only

Note 2: For TC74HC163A only

Not Recommended for New Design

**AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	Figure 1	—	4	8	ns
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	Figure 1	—	13	21	ns
Propagation delay time (CK-CO) [count mode]	$t_{pLH}$ $t_{pHL}$	Figure 1	—	16	26	ns
Propagation delay time (CK-CO) [preset mode]	$t_{pLH}$	Figure 2	—	18	30	ns
	$t_{pHL}$		—	20	35	
Propagation delay time (ENT-CO)	$t_{pLH}$ $t_{pHL}$	Figure 6	—	10	17	ns
Propagation delay time ( $\overline{\text{CLR}} - Q$ ) (Note)	$t_{pHL}$	Figure 4	—	17	26	ns
Propagation delay time ( $\overline{\text{CLR}} - CO$ ) (Note)	$t_{pHL}$	Figure 4	—	20	35	ns
Maximum clock frequency	$f_{max}$	—	36	63	—	MHz

Note: For TC74HC161A only

Not Recommended for New Design



## AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation delay time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1	2.0	—	48	125	—	155	ns
			4.5	—	16	25	—	31	
			6.0	—	14	21	—	26	
Propagation delay time (CK-CO) [count mode]	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1	2.0	—	57	150	—	190	ns
			4.5	—	19	30	—	38	
			6.0	—	16	26	—	33	
Propagation delay time (CK-CO) [preset mode]	t <sub>pLH</sub>	Figure 2	2.0	—	66	175	—	220	ns
			4.5	—	22	35	—	44	
			6.0	—	19	30	—	37	
	t <sub>pHL</sub>		2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Propagation delay time (ENT-CO)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 6	2.0	—	39	100	—	125	ns
			4.5	—	13	20	—	25	
			6.0	—	11	17	—	21	
Propagation delay time ( $\overline{\text{CLR}}$ -Q) (Note 2)	t <sub>pHL</sub>	Figure 4	2.0	—	60	150	—	190	ns
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	33	
Propagation delay time ( $\overline{\text{CLR}}$ -CO) (Note 2)	t <sub>pHL</sub>	Figure 4	2.0	—	72	200	—	250	ns
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Maximum clock frequency	f <sub>max</sub>	—	2.0	6	18	—	5	—	MHz
			4.5	31	53	—	25	—	
			6.0	36	62	—	29	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note 1)	—	—	34	—	—	—	pF	

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C<sub>PD</sub>, and ΔI<sub>CC</sub> which is obtained from the following formula:

In case of TC74HC161A/163A:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

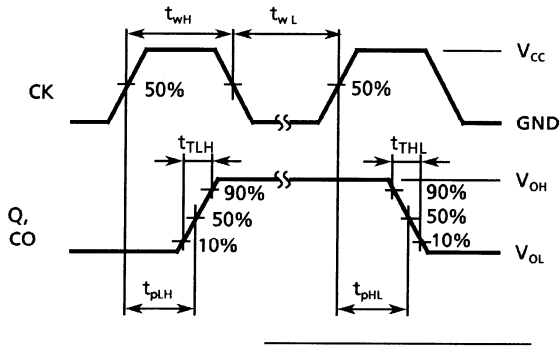
C<sub>QA</sub>~C<sub>QD</sub> and C<sub>CO</sub> are the capacitances at QA~QD and CO, respectively.

f<sub>CK</sub> is the input frequency of the CK.

Note 2: For TC74HC161A only

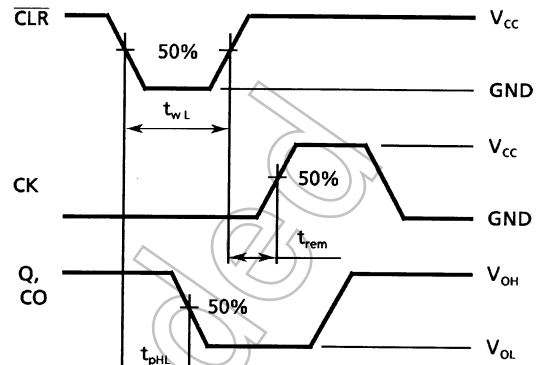
**Switching Characteristics Test Waveform**

**Count Mode**



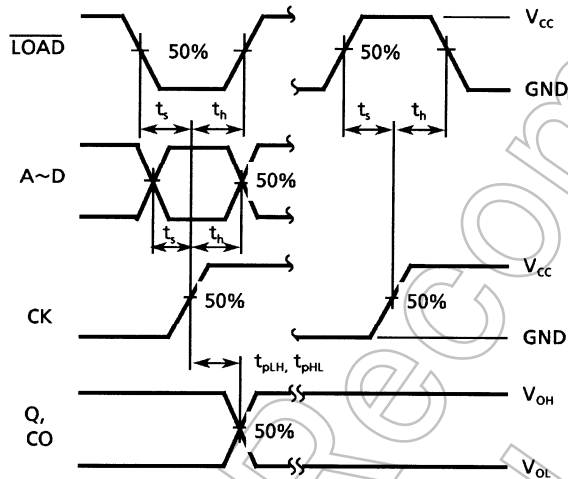
**Figure 1**

**Clear Mode (TC74HC161A)**



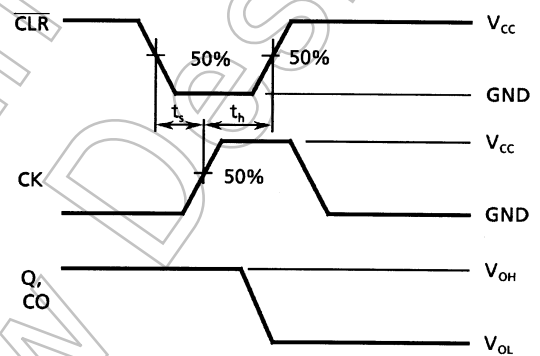
**Figure 4**

**Preset Mode**



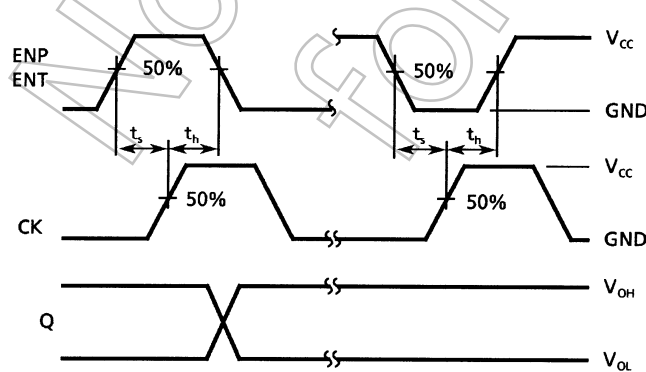
**Figure 2**

**Clear Mode (TC74HC163A)**



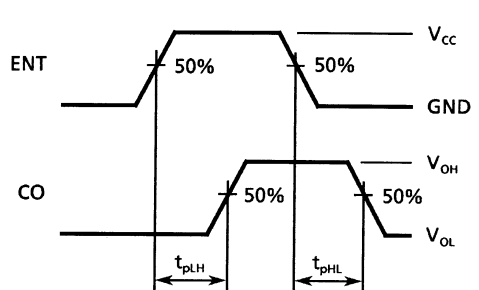
**Figure 5**

**Count Enable Mode**



**Figure 3**

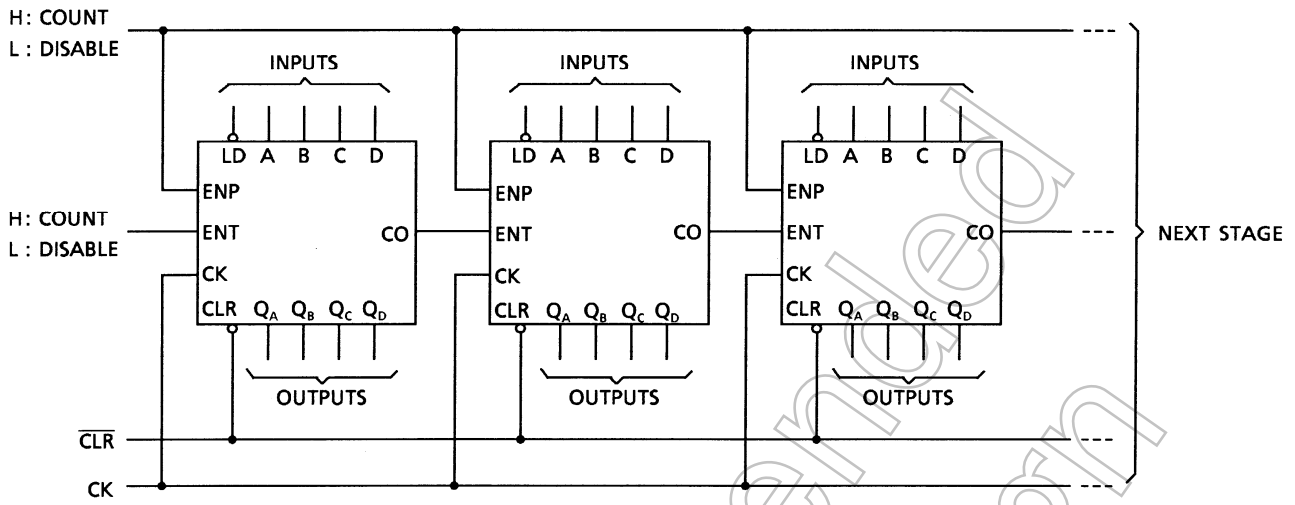
**Cascade Mode (fix maximum count)**



**Figure 6**

**Typical Application**

**Parallel Carry N-Bit Counter**

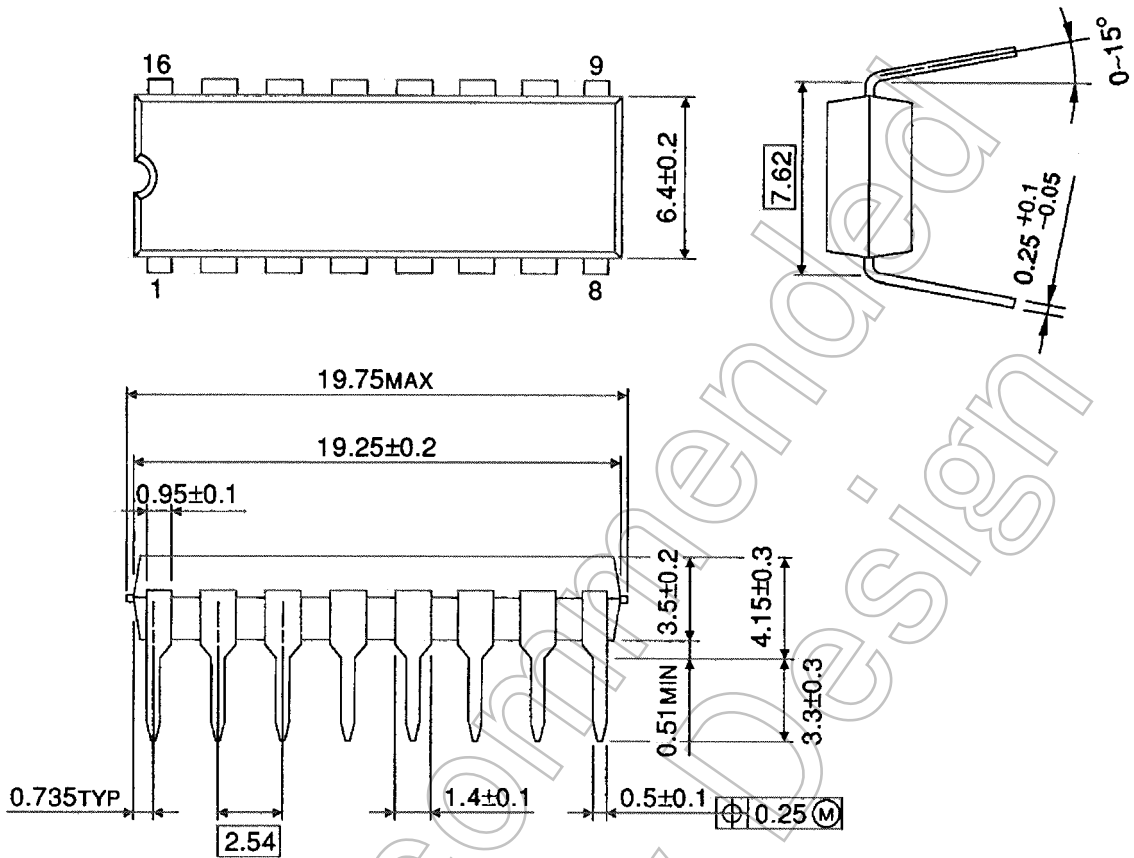


Not Recommended for New Designs

**Package Dimensions**

DIP16-P-300-2.54A

Unit : mm



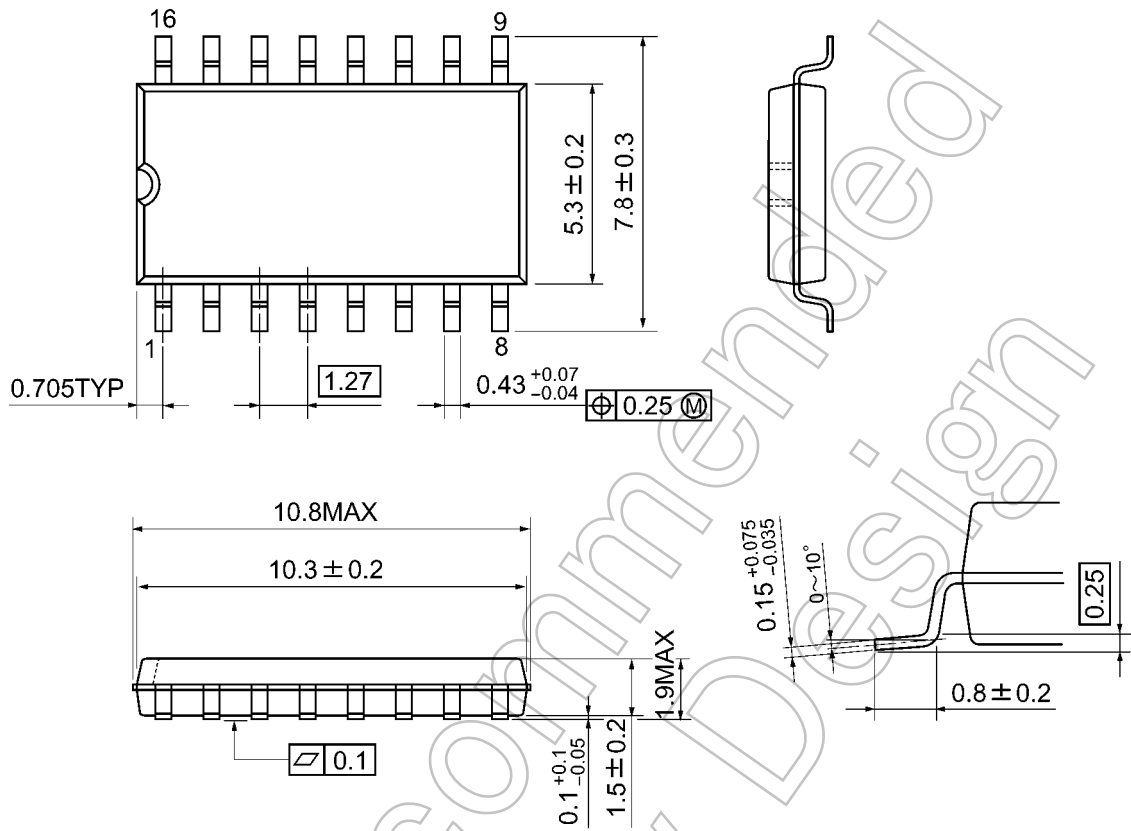
Weight: 1.00 g (typ.)

Not Recommended for New Design

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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