TC74HC7643AP/AF

Octal Bus Transceiver (with Schmitt Trigger Inputs)
TC74HC7643 3-State, Inverting and Non-Inverting

The TC74HC7643A is a high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

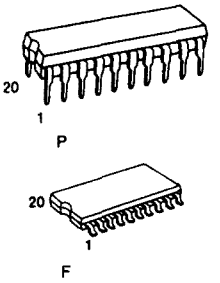
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC7643A has the same configuration and function as the TC74HC643A. It differs in that the former has Schmitt trigger inputs, making it ideal for such applications as line receivers, etc.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



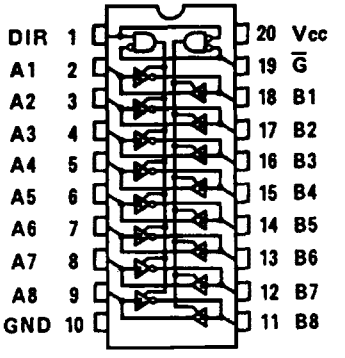
Features

- High Speed: t_{pd} = 14ns(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Output Drive Capability: 15 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS643

Application Notes

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator ICs such as the Toshiba TC40117BP.

TC74HC7643A

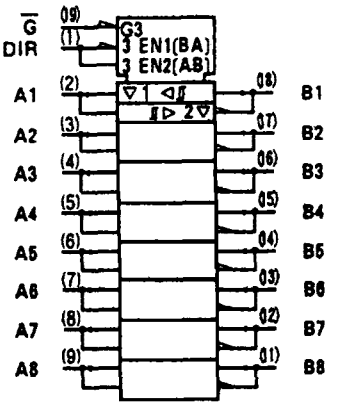


Pin Assignment

Truth Table

Inputs		Function	
$\overline{G}$	DIR	A Bus	B Bus
L	L	Output	Input
L	H	Input	Output
H	X	High Impedance	

X: "H" or "L"
Z: High Impedance



IEC Logic Symbol

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
Positive Threshold Voltage	V_P	–		2.0 4.5 6.0	1.0 2.3 3.5	1.25 2.7 3.5	1.5 3.15 4.2	1.0 2.3 3.0	1.5 3.15 4.2	V
Negative Threshold Voltage	V_N	–		2.0 4.5 6.0	0.3 1.13 1.5	0.65 1.6 2.3	0.9 2.0 2.6	0.3 1.13 1.5	0.9 2.0 2.6	V
Hysteresis Voltage	V_H	–		2.0 4.5 6.0	0.3 0.6 0.8	0.6 1.1 1.2	1.0 1.4 1.7	0.3 0.6 0.8	1.0 1.4 1.7	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -6 mA I_{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 6 mA I_{OL} = -7.8mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	–	–	±0.5	–	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			CL	V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	50	2.0 4.5 6.0	– – –	25 7 6	60 12 10	– – –	75 15 13	ns
Propagation Delay Time	t_{pLH} t_{pHL}	–	50	2.0 4.5 6.0	– – –	50 17 15	125 25 21	– – –	155 31 26	
			150	2.0 4.5 6.0	– – –	63 22 18	150 30 26	– – –	205 41 35	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L = 1k Ω	50	2.0 4.5 6.0	– – –	50 17 15	150 30 26	– – –	190 38 32	
			150	2.0 4.5 6.0	– – –	63 22 19	180 36 31	– – –	225 45 38	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1k Ω	50	2.0 4.5 6.0	– – –	45 20 19	150 30 26	– – –	190 38 32	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			–	5	10	–	10	pF
Bus Input Capacitance	C_{OUT}	An, Bn			–	13	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC7640A/7643A			–	48	–	–	–	
		TC74HC7645A			–	45	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$(per bit)

Notes