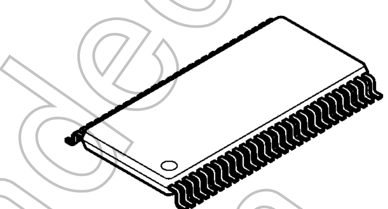
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX162834FT

Low-Voltage 18-Bit Universal Bus Driver with 3.6-V Tolerant Inputs and Outputs



TSSOP56-P-0061-0.50A

Weight: 0.25 g (typ.)

The TC74VCX162834FT is a high-performance CMOS 18-bit universal bus driver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low.

When LE is high, the A data is latched if the clock (CK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CK.

When $\overline{OE}$ is high, the outputs are in a high-impedance state. The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.

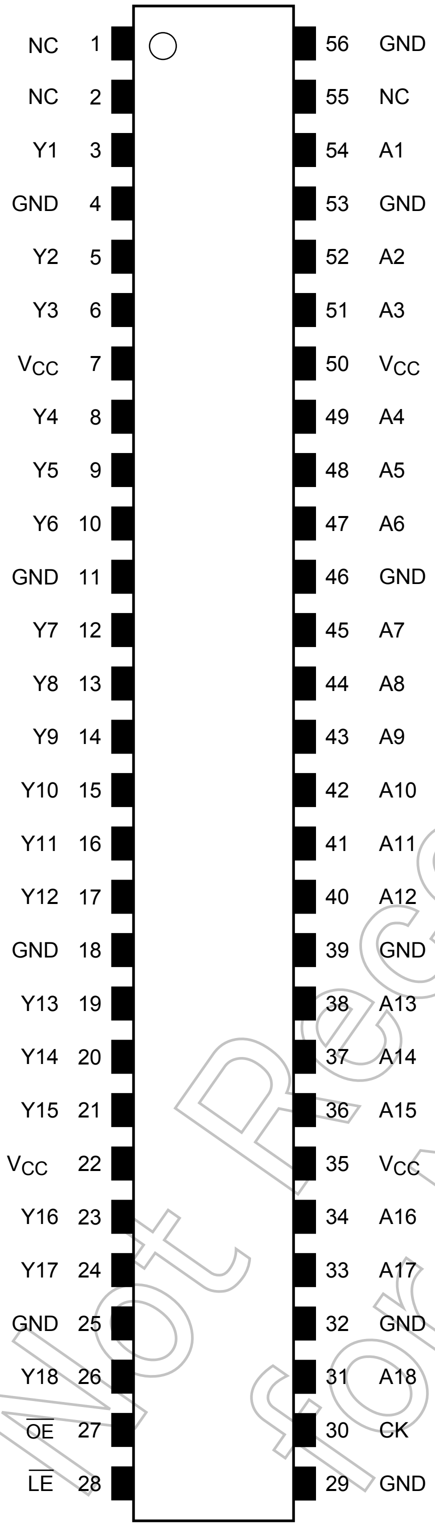
All inputs are equipped with protection circuits against static discharge.

Features

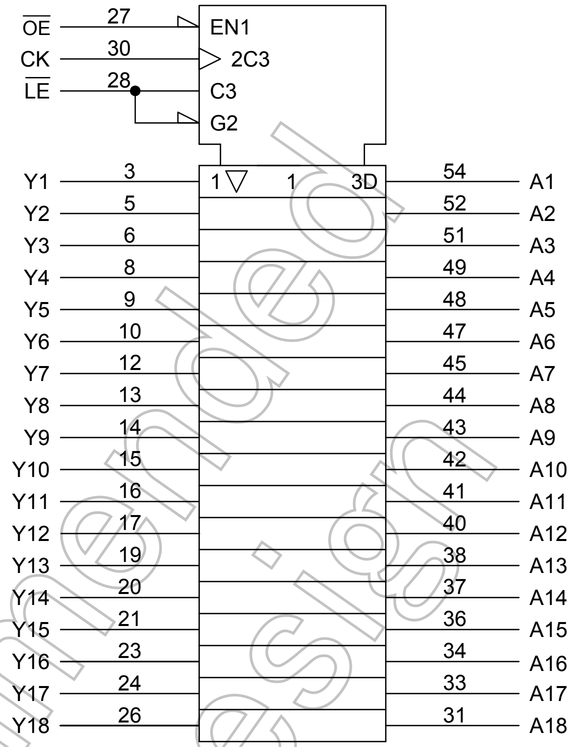
- 26-Ω series resistors on outputs
- Low-voltage operation: V_{CC} = 1.8 to 3.6 V
- High-speed operation: t_{pd} = 3.9 ns (max) (V_{CC} = 3.0 to 3.6 V)
  : t_{pd} = 5.0 ns (max) (V_{CC} = 2.3 to 2.7 V)
  : t_{pd} = 9.8 ns (max) (V_{CC} = 1.8 V)
- Output current: I_{OH}/I_{OL} = ±12 mA (min) (V_{CC} = 3.0 V)
  : I_{OH}/I_{OL} = ±8 mA (min) (V_{CC} = 2.3 V)
  : I_{OH}/I_{OL} = ±4 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: −300 mA
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package: TSSOP
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Start of commercial production
1998-08

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

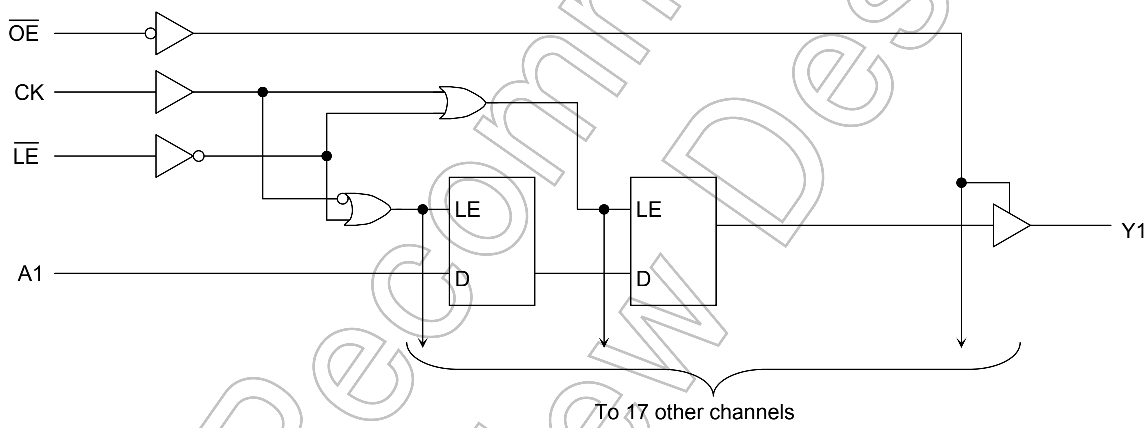
Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y0 (Note)
L	H	L	X	Y0 (Note)

X: Don't care

Z: High impedance

Note : Output level before the indicated steady-state input conditions were established, provided that CK was high or low before $\overline{LE}$ went high.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 4.6	V
DC input voltage	V_{IN}	−0.5 to 4.6	V
DC output voltage	V_{OUT}	−0.5 to 4.6 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6	V
		1.2 to 3.6 (Note 2)	
Input voltage	V_{IN}	−0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note 3)	V
		0 to V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	±12 (Note 5)	mA
		±8 (Note 6)	
		±4 (Note 7)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.3 to 2.7 V

Note 7: V_{CC} = 1.8 V

Note 8: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C, 2.7 V < V_{CC} ≤ 3.6 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.7 to 3.6	V_{CC} – 0.2	—	V
				I_{OH} = –6 mA	2.7	2.2	—	
				I_{OH} = –8 mA	3.0	2.4	—	
				I_{OH} = –12 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 6 mA	2.7	—	0.4	
				I_{OL} = 8 mA	3.0	—	0.55	
				I_{OL} = 12 mA	3.0	—	0.8	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	20.0	μA
			V_{CC} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} – 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = –40 to 85°C, 2.3 V ≤ V_{CC} ≤ 2.7 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V_{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.3 to 2.7	V_{CC} – 0.2	—	V
				I_{OH} = –4 mA	2.3	2.0	—	
				I_{OH} = –6 mA	2.3	1.8	—	
				I_{OH} = –8 mA	2.3	1.7	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I_{OL} = 6 mA	2.3	—	0.4	
				I_{OL} = 8 mA	2.3	—	0.6	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.3 to 2.7	—	20.0	μA
			V_{CC} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = –40 to 85°C, 1.8 V ≤ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	0.7 × V_{CC}	—	V
	L-level	V_{IL}	—		1.8 to 2.3	—	0.2 × V_{CC}	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	1.8	V_{CC} – 0.2	—	V
				I_{OH} = –4 mA	1.8	1.4	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	
				I_{OL} = 4 mA	1.8	—	0.3	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.8	—	±20.0	

AC Characteristics (Ta = –40 to 85°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$) (Note 1)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{max}	Figure 1, Figure 3	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation delay time (An-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.0	
			3.3 ± 0.3	0.6	3.9	
Propagation delay time (CK-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 3	1.8	1.5	9.2	ns
			2.5 ± 0.2	0.8	5.2	
			3.3 ± 0.3	0.6	4.2	
Propagation delay time ($\overline{LE}$-Yn)	t_{pLH} t_{pHL}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	6.3	
			3.3 ± 0.3	0.6	5.1	
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 5	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 5	1.8	1.5	7.9	ns
			2.5 ± 0.2	0.8	4.7	
			3.3 ± 0.3	0.6	4.2	
Minimum pulse width	$t_{W (H)}$ $t_{W (L)}$	Figure 1, Figure 3, Figure 4	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time (An-CK, An-$\overline{LE}$)	t_s	Figure 1, Figure 3, Figure 4	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time (An-CK, An-$\overline{LE}$)	t_h	Figure 1, Figure 3, Figure 4	1.8	1.0	—	ns
			2.5 ± 0.2	0.6	—	
			3.3 ± 0.3	0.7	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics
(Ta = 25°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note)	1.8	0.25	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note)	2.5	0.35	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note)	3.3	0.45	
Quiet output minimum dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note)	1.8	−0.25	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note)	2.5	−0.35	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note)	3.3	−0.45	
Quiet output minimum dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note)	1.8	1.35	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note)	2.5	1.85	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note)	3.3	2.45	

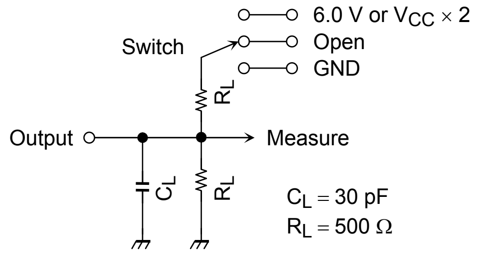
Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C_{OUT}	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	$f_{IN} = 10$ MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18$ (per bit)

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @V_{CC} = 3.3 ± 0.3 V V_{CC} × 2 @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

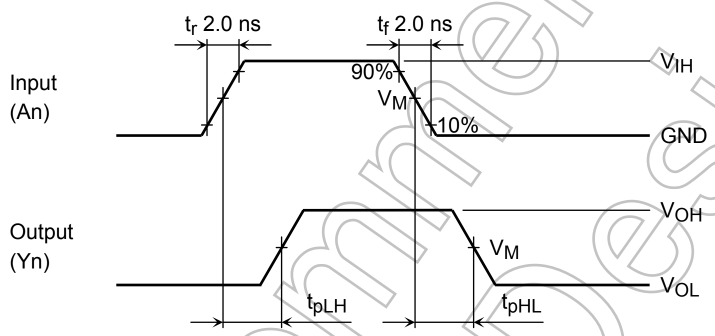


Figure 2 t_{pLH}, t_{pHL}

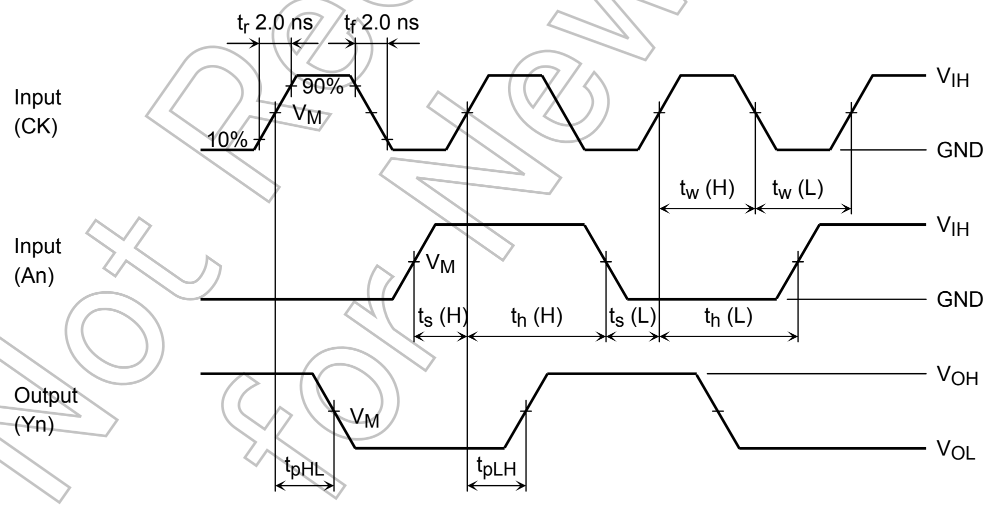


Figure 3 t_{pLH}, t_{pHL}, t_w, t_s, t_h

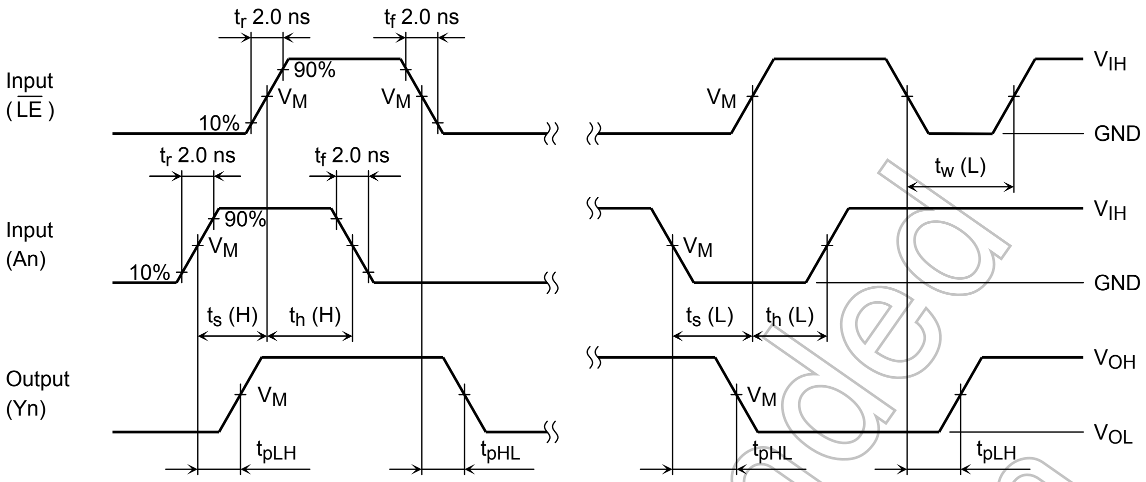


Figure 4 t_{pLH}, t_{pHL}, t_w, t_s, t_h

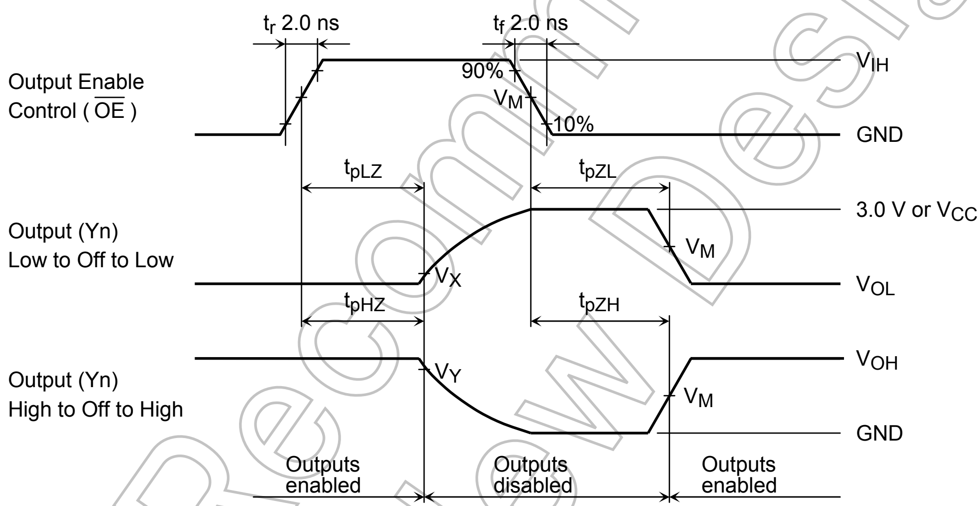
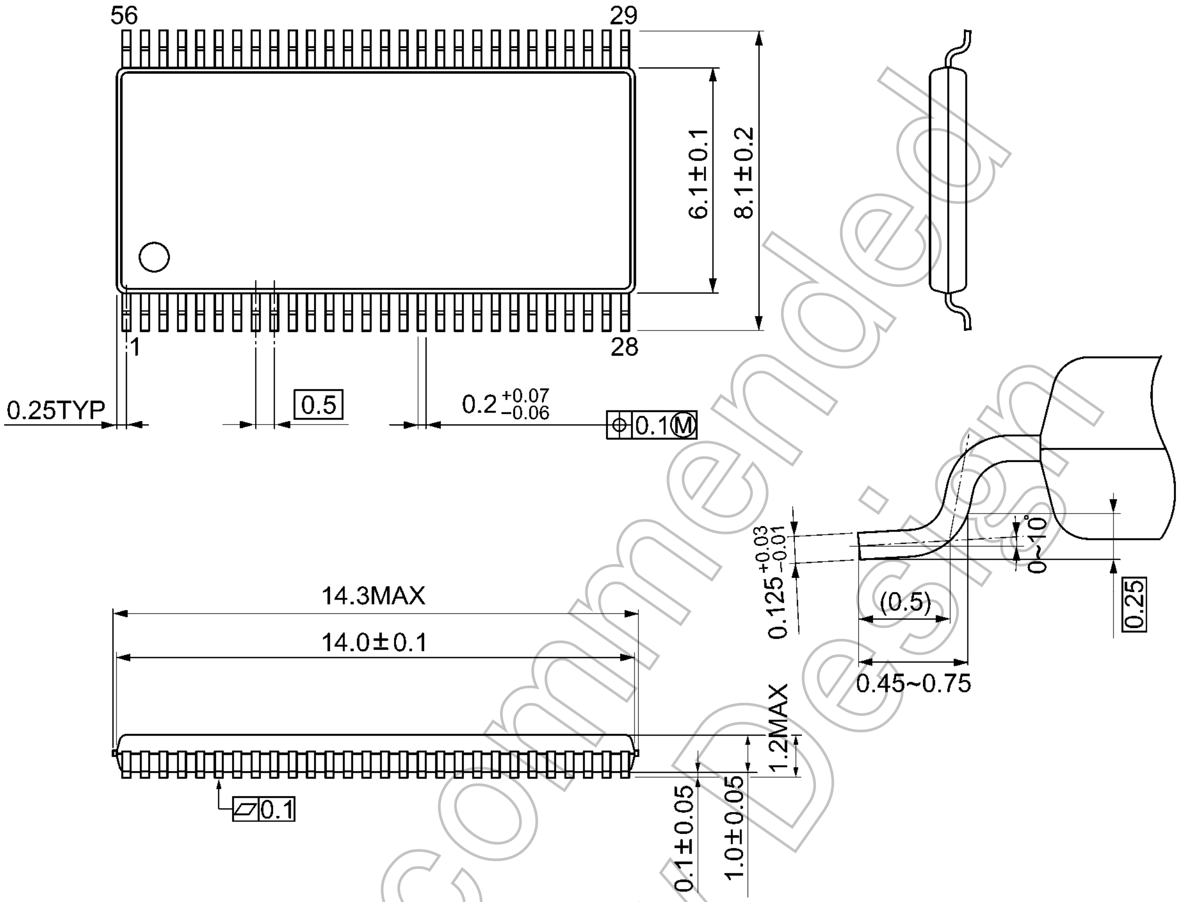


Figure 5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Package Dimensions

TSSOP56-P-0061-0.50A Unit: mm



Weight: 0.25 g (typ.)

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