

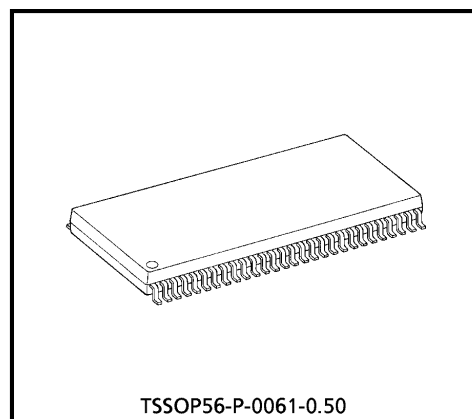
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16501FT**LOW-VOLTAGE 18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3.6 V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16501FT is a high performance CMOS 18-bit UNIVERSAL BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CKAB and CKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch / flip-flop on the low-to-high transition of CKAB.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CKBA. When the \overline{OE} input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc. All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25 g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6 V$
- High Speed Operation : $t_{pd} = 2.9 ns (max)$ at $V_{CC} = 3.0 \sim 3.6 V$
 : $t_{pd} = 3.5 ns (max)$ at $V_{CC} = 2.3 \sim 2.7 V$
 : $t_{pd} = 7.0 ns (max)$ at $V_{CC} = 1.8 V$
- 3.6 V Tolerant inputs and outputs.
- Output Current : $I_{OH} / I_{OL} = \pm 24 mA (min)$ at $V_{CC} = 3.0 V$
 : $I_{OH} / I_{OL} = \pm 18 mA (min)$ at $V_{CC} = 2.3 V$
 : $I_{OH} / I_{OL} = \pm 6 mA (min)$ at $V_{CC} = 1.8 V$
- Latch-up Performance : $\pm 300 mA$
- ESD Performance : Human Body Model $> \pm 2000 V$
 : Machine Model $> \pm 200 V$
- Package : TSSOP
 (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5 V and 3.3 V signals.
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 3)

(Note 1) : Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

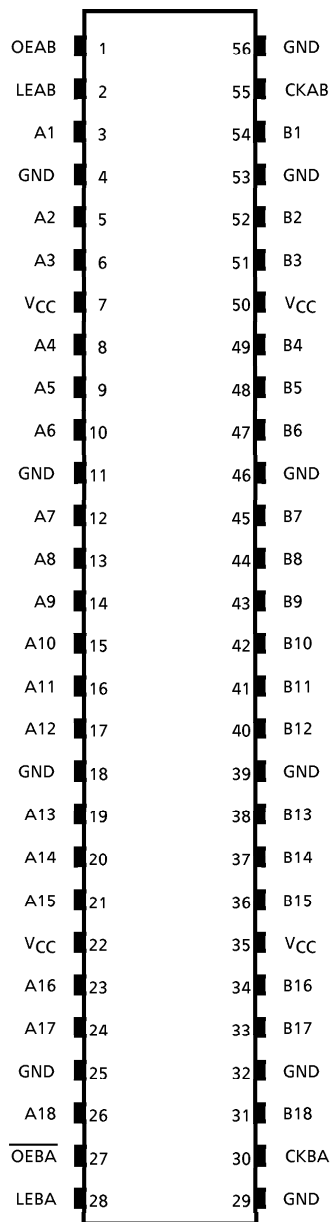
(Note 2) : All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

(Note 3) : To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

980910EBA2

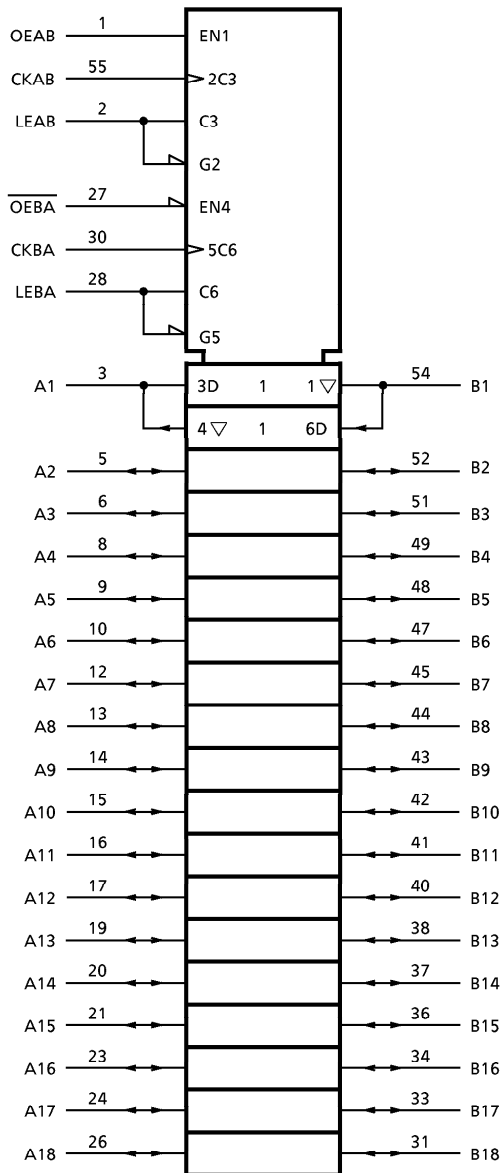
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PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



980910EBA2'

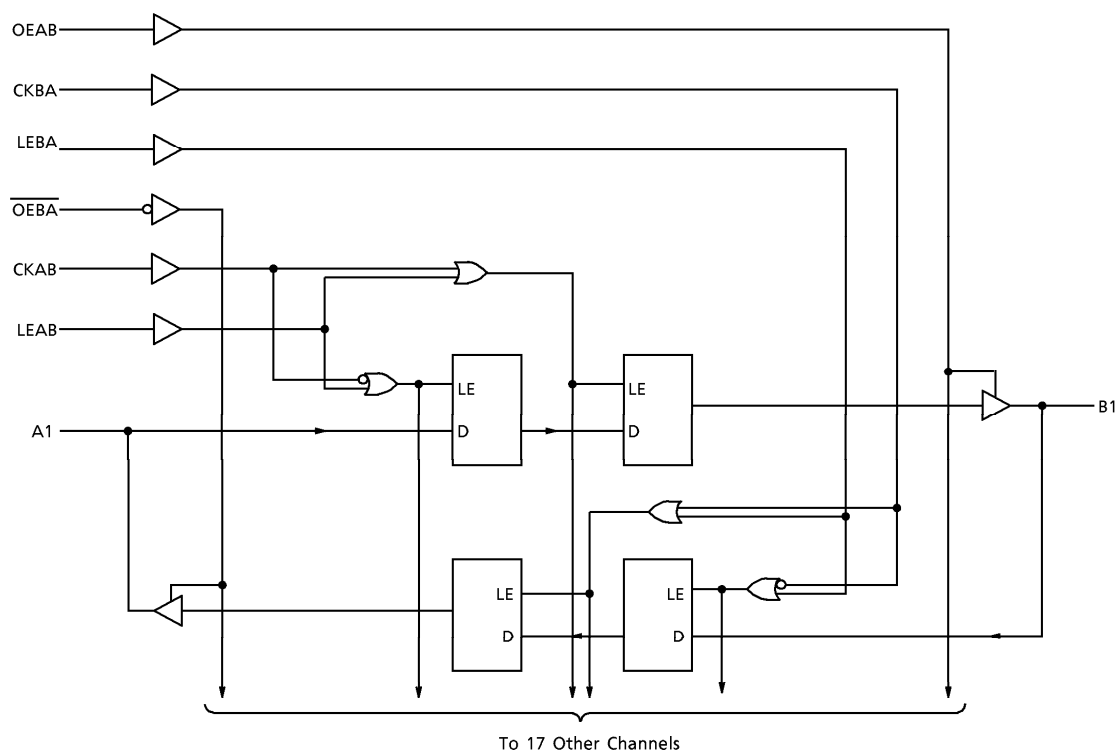
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TRUTH TABLE *

INPUTS				OUTPUTS
OEAB	LEAB	CKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	\uparrow	L	L
H	L	\downarrow	H	H
H	L	H	X	B0**
H	L	L	X	B0**

- * A-to-B data flow is shown: B-to-A flow is similar but uses \overline{OEBA} , LEBA, and CKBA.
- ** Output level before the indicated steady-state input conditions were established, provided that CKAB was low or high before LEAB went low.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~4.6	V
DC Input Voltage (OEAB, \overline{OEBA} , LEAB, LEBA, CKAB, CKBA)	V_{IN}	-0.5~4.6	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5~4.6 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} /Ground Current Per Supply Pin	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

(Note 1) : Off-State

(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (OEAB, \overline{OEBA} , LEAB, LEBA, CKAB, CKBA)	V_{IN}	-0.3~3.6	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	± 24 (Note 7)	mA
		± 18 (Note 8)	
		± 6 (Note 9)	
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) : Data Retention Only

(Note 5) : Off-State

(Note 6) : High or Low State

(Note 7) : $V_{CC} = 3.0\sim 3.6$ V

(Note 8) : $V_{CC} = 2.3\sim 2.7$ V

(Note 9) : $V_{CC} = 1.8$ V

(Note 10) : $V_{IN} = 0.8\sim 2.0$ V, $V_{CC} = 3.0$ V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C, 2.7 V < VCC ≤ 3.6 V)

PARAMETER		SYMBOL	TEST CONDITION	VCC (V)	MIN	MAX	UNIT	
Input Voltage	"H" Level	V _{IH}		2.7~3.6	2.0	—	V	
	"L" Level	V _{IL}		2.7~3.6	—	0.8		
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = -12 mA	2.7	2.2	—	
				I _{OH} = -18 mA	3.0	2.4	—	
				I _{OH} = -24 mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7~3.6	—	0.2	
				I _{OL} = 12 mA	2.7	—	0.4	
				I _{OL} = 18 mA	3.0	—	0.4	
				I _{OL} = 24 mA	3.0	—	0.55	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V	2.7~3.6	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	2.7~3.6	—	20.0	μA	
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	2.7~3.6	—	± 20.0		
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V	2.7~3.6	—	750	μA	

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C, 2.3 V ≤ VCC ≤ 2.7 V)

PARAMETER		SYMBOL	TEST CONDITION	VCC (V)	MIN	MAX	UNIT	
Input Voltage	"H" Level	V _{IH}		2.3~2.7	1.6	—	V	
	"L" Level	V _{IL}		2.3~2.7	—	0.7		
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2	—	V
				I _{OH} = -6 mA	2.3	2.0	—	
				I _{OH} = -12 mA	2.3	1.8	—	
				I _{OH} = -18 mA	2.3	1.7	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3~2.7	—	0.2	
				I _{OL} = 12 mA	2.3	—	0.4	
				I _{OL} = 18 mA	2.3	—	0.6	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V	2.3~2.7	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V	2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	2.3~2.7	—	20.0	μA	
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	2.3~2.7	—	± 20.0		

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40\sim 85^\circ\text{C}$, $1.8\text{ V} \leq V_{CC} < 2.3\text{ V}$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	$0.7 \times V_{CC}$	—	V
	"L" Level	V_{IL}			1.8~2.3	—	$0.2 \times V_{CC}$	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\ \mu\text{A}$	1.8	$V_{CC} - 0.2$	—	V
				$I_{OH} = -6\ \text{mA}$	1.8	1.4	—	
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100\ \mu\text{A}$	1.8	—	0.2	
				$I_{OL} = 6\ \text{mA}$	1.8	—	0.3	
Input Leakage Current		I_{IN}	$V_{IN} = 0\sim 3.6\ \text{V}$		1.8	—	± 5.0	μA
3-State Output Off-State Current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim 3.6\ \text{V}$		1.8	—	± 10.0	μA
Power Off Leakage Current		I_{OFF}	$V_{IN}, V_{OUT} = 0\sim 3.6\ \text{V}$		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.8	—	20.0	μA
			$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6\ \text{V}$		1.8	—	± 20.0	

AC characteristics (Ta = -40~85°C, Input tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	MIN	MAX	UNIT
Maximum Clock Frequency	fMAX	(Fig.1, 2)	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (An, Bn-Bn, An)	tpLH tpHL	(Fig.1, 2)	1.8	1.5	7.0	ns
			2.5 ± 0.2	0.8	3.5	
			3.3 ± 0.3	0.6	2.9	
Propagation Delay Time (CKAB, CKBA-Bn, An)	tpLH tpHL	(Fig.1, 3)	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.4	
			3.3 ± 0.3	0.6	3.5	
Propagation Delay Time (LEAB, LEBA-Bn, An)	tpLH tpHL	(Fig.1, 4)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
Output Enable Time (OEAB, OEBA-Bn, An)	tpZL tpZH	(Fig.1, 5, 6)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
Output Disable Time (OEAB, OEBA-Bn, An)	tpLZ tpHZ	(Fig.1, 5, 6)	1.8	1.5	7.6	ns
			2.5 ± 0.2	0.8	4.2	
			3.3 ± 0.3	0.6	3.7	
Minimum Pulse Width	tw (H) tw (L)	(Fig.1, 3, 4)	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time	ts	(Fig.1, 3, 4)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Hold Time	th	(Fig.1, 3, 4)	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to Output Skew	tosLH tosHL	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For CL = 50 pF, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.

$$(tosLH = |tpLHm - tpLHn|, tosHL = |tpHLm - tpHLn|)$$

Dynamic switching characteristics (Ta = 25°C, Input tr = tf = 2.0 ns, CL = 30 pF)

PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	UNIT
Quiet Output Maximum Dynamic VOL	VOLP	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	0.25	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	0.6	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic VOL	VOLV	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	-0.25	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	-0.6	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	-0.8	
Quiet Output Minimum Dynamic VOH	VOHV	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	1.5	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	1.9	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	2.2	

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

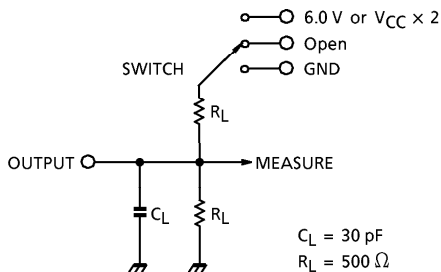
PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	UNIT
Input Capacitance	C _{IN}	(OEAB, OEBA, LEAB, LEBA, CKAB, CKBA)	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	C _{I/O}	(An, Bn)	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

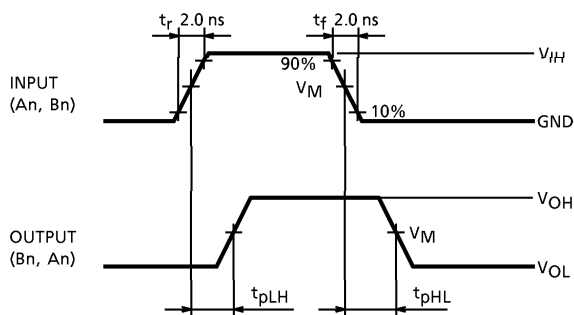
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 18 \text{ (per bit)}$$

TEST CIRCUIT
Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @ $V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$ @ $V_{CC} = 1.8 \text{ V}$
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM
Fig.2 t_{pLH}, t_{pHL}



SYMBOL	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC} / 2$	$V_{CC} / 2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

Fig.3 $t_{pLH}, t_{pHL}, t_w, t_s, t_h$

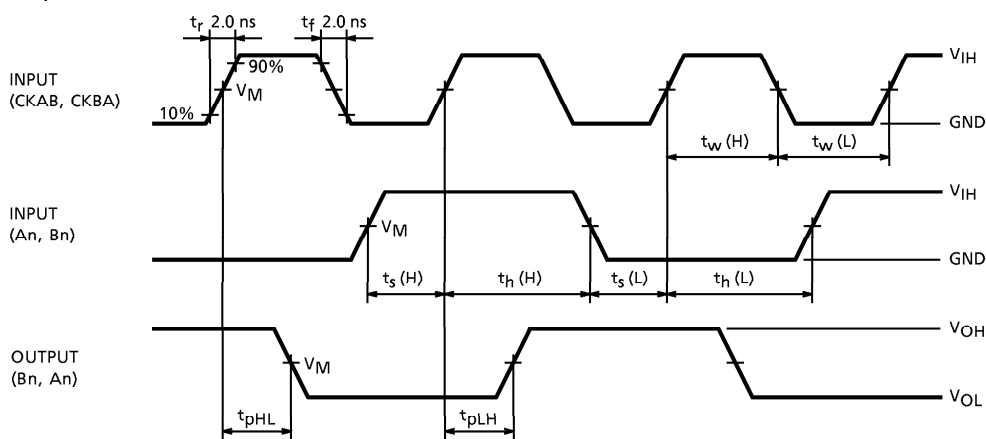


Fig.4 t_{pLH} , t_{pHL} , t_w , t_s , t_h

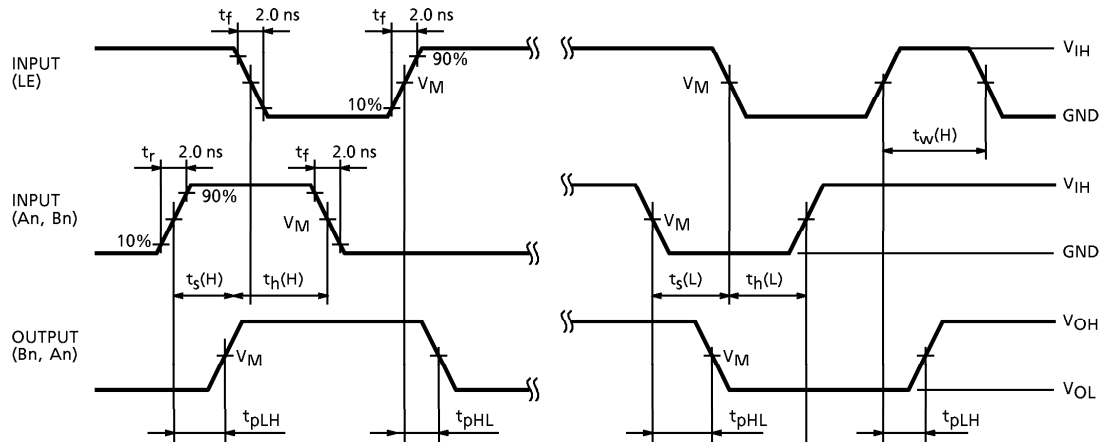


Fig.5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

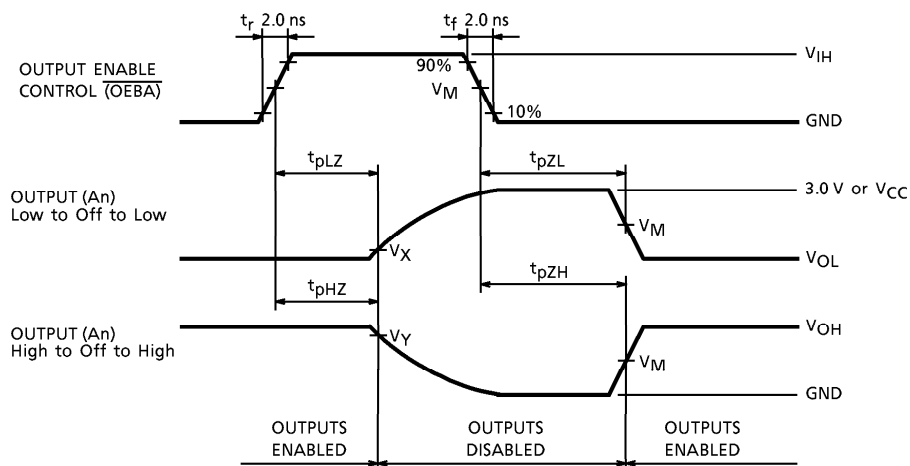
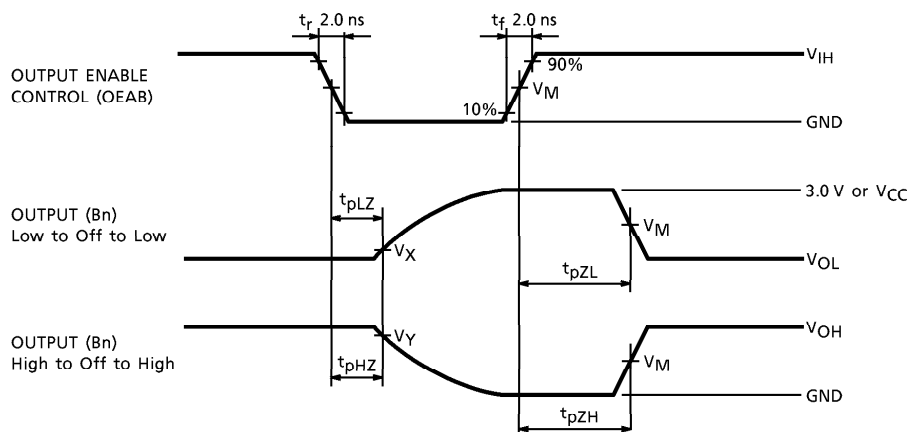
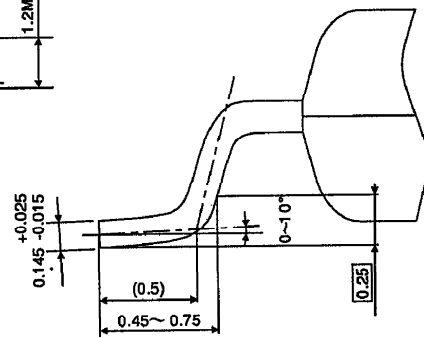
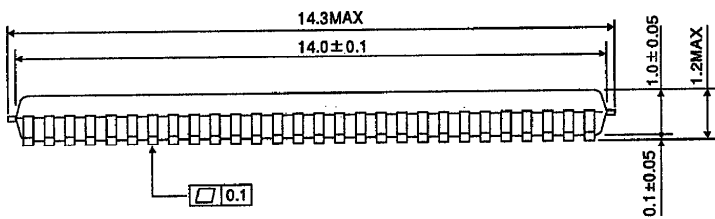
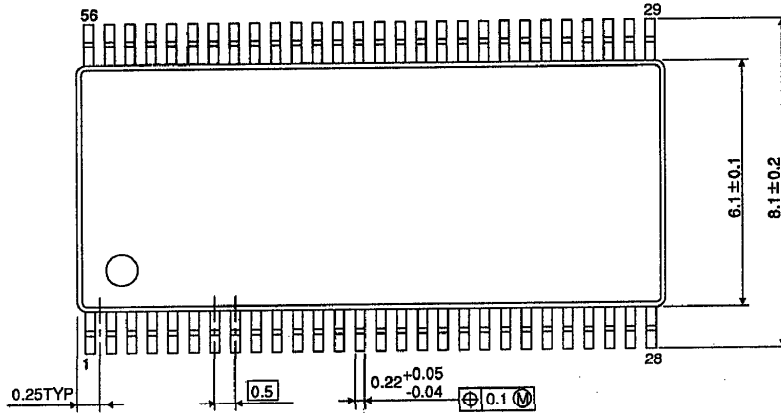


Fig.6 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



OUTLINE DRAWING
TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)