TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

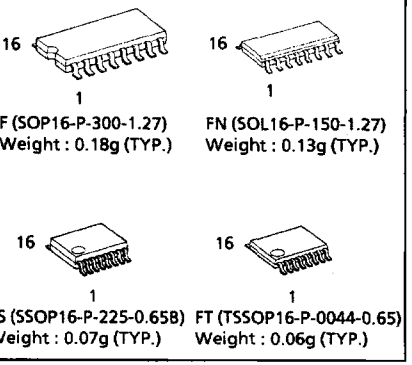
TC74VHC161F, TC74VHC161FN, TC74VHC161FS, TC74VHC161FT
TC74VHC163F, TC74VHC163FN, TC74VHC163FS, TC74VHC163FT

SYNCHRONOUS PRESETTABLE 4 - BIT COUNTER
TC74VHC161F / FN / FS / FT BINARY, ASYNCHRONOUS CLEAR
TC74VHC163F / FN / FS / FT BINARY, SYNCHRONOUS CLEAR

The TC74VHC 161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active on low logic level.
Presetting of each IC's is synchronous to the rising edge of CK.
The clear function of the TC74VHC163 is synchronous to CK, while the TC74VHC161 are cleared asynchronously.
Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n - bit counters without using external gates.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

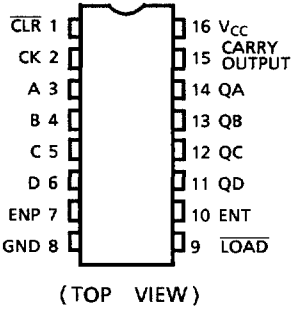
FEATURES:

- High Speed ..... f_{MAX} = 185MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ..... $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range .. V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ..... V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS161/163



F (SOP16-P-300-1.27) Weight : 0.18g (TYP.)
FN (SOL16-P-150-1.27) Weight : 0.13g (TYP.)
FS (SSOP16-P-225-0.65B) Weight : 0.07g (TYP.)
FT (TSSOP16-P-0044-0.65) Weight : 0.06g (TYP.)

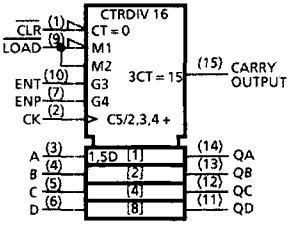
PIN ASSIGNMENT



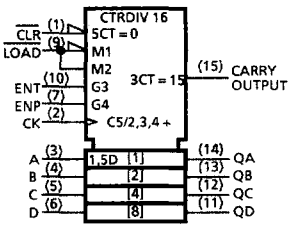
(TOP VIEW)

IEC LOGIC SYMBOL

TC74VHC161



TC74VHC163



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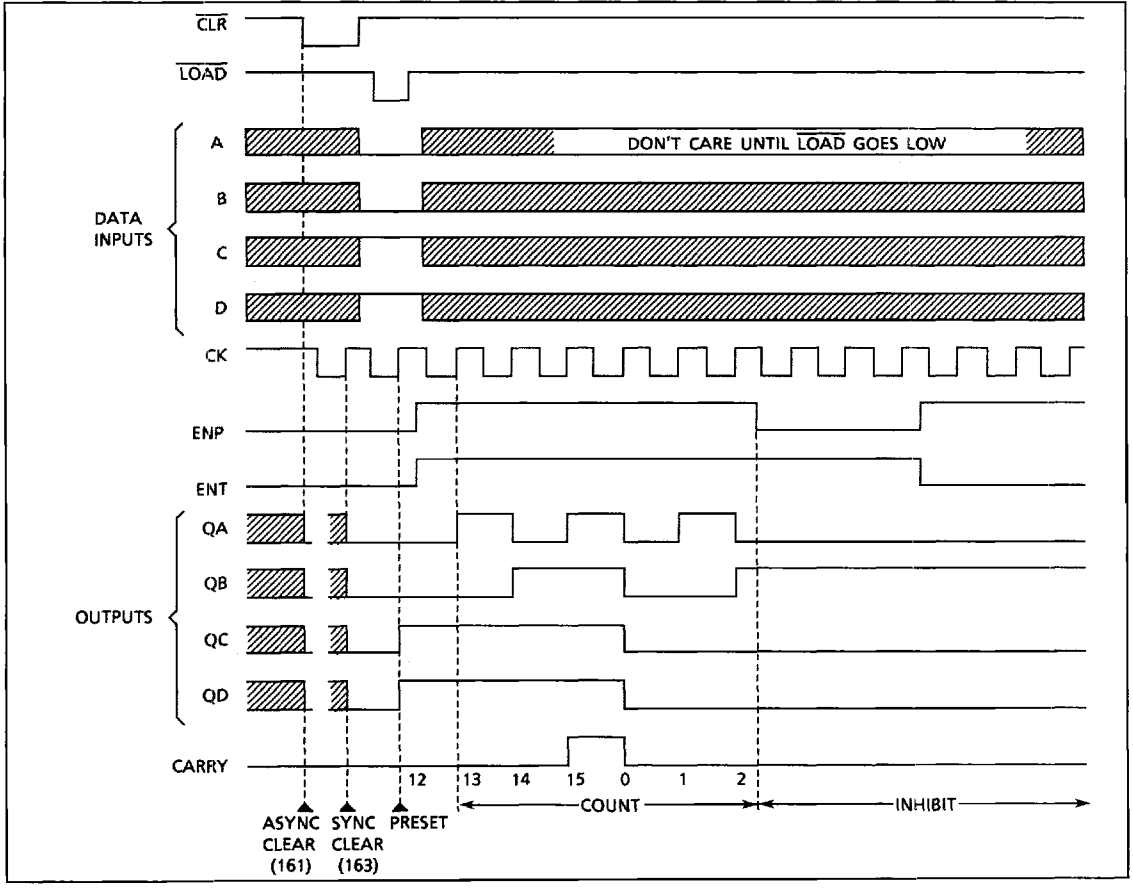
TRUTH TABLE

TC74VHC161 INPUTS					TC74VHC163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

Note X : Don't Care
A, B, C, D : Logic Level of Data Inputs
Carry : CARRY = ENT·QA·QB·QC·QD

TIMING CHART



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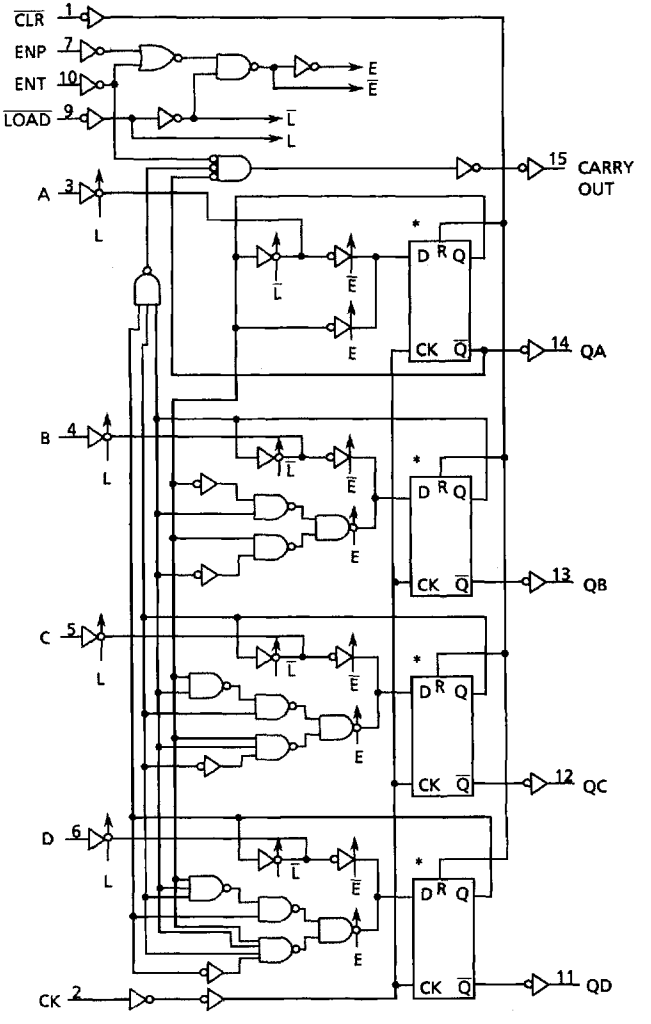
SYSTEM DIAGRAM



* TRUTH TABLE OF INTERNAL F/F

TC74VHC161					TC74VHC163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↓	H	L	H
L	↓	L	L	H	L	↓	L	L	H
H	↓	L	H	L	H	↓	L	H	L
X	↑	L	NO CHANGE		X	↑	X	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V_{CC}×0.7	—	—	V_{CC}×0.7	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V_{CC}×0.3	—	V_{CC}×0.3	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = −40~85°C	UNIT
			V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig. 1	3.3 ± 0.3 5.0 ± 0.5	5.0 5.0	5.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$	Fig. 4	3.3 ± 0.3 5.0 ± 0.5	5.0 5.0	5.0 5.0	
Minimum Set - up Time (A, B, C, D)	t_s	Fig. 2	3.3 ± 0.3 5.0 ± 0.5	5.5 4.5	6.5 4.5	
Minimum Set - up Time ($\overline{LOAD}$)	t_s	Fig. 2	3.3 ± 0.3 5.0 ± 0.5	8.0 5.0	9.5 6.0	
Minimum Set - up Time (ENT, ENP)	t_s	Fig. 3	3.3 ± 0.3 5.0 ± 0.5	7.5 5.0	9.0 6.0	
Minimum Set - up Time ($\overline{CLR}$)**	t_s	Fig. 5	3.3 ± 0.3 5.0 ± 0.5	4.0 3.5	4.0 3.5	
Minimum Hold Time	t_h	Fig. 2, 3	3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	
Minimum Hold Time ($\overline{CLR}$)**	t_h	Fig. 5	3.3 ± 0.3 5.0 ± 0.5	1.0 1.5	1.0 1.5	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}	Fig. 4	3.3 ± 0.3 5.0 ± 0.5	2.5 1.5	2.5 1.5	

* for TC74VHC161 only
** for TC74VHC163 only

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK - Q)	t_{pLH} t_{pHL}	Fig. 1, 2	3.3 ± 0.3	15	−	8.3	12.8	1.0	15.0	ns
				50	−	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	−	4.9	8.1	1.0	9.5	
				50	−	6.4	10.1	1.0	11.5	
Propagation Delay Time (CK - CARRY, Count Mode)	t_{pLH} t_{pHL}	Fig. 1	3.3 ± 0.3	15	−	8.7	13.6	1.0	16.0	
				50	−	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	−	4.9	8.1	1.0	9.5	
				50	−	6.4	10.1	1.0	11.5	
Propagation Delay Time (CK - CARRY, Preset Mode)	t_{pLH} t_{pHL}	Fig. 2	3.3 ± 0.3	15	−	11.0	17.2	1.0	20.0	
				50	−	13.5	20.7	1.0	23.5	
			5.0 ± 0.5	15	−	6.2	10.3	1.0	12.0	
				50	−	7.7	12.3	1.0	14.0	
Propagation Delay Time (ENT - CARRY)	t_{pLH} t_{pHL}	Fig. 6	3.3 ± 0.3	15	−	7.5	12.3	1.0	14.5	
				50	−	10.5	15.8	1.0	18.0	
			5.0 ± 0.5	15	−	4.9	8.1	1.0	9.5	
				50	−	6.4	10.1	1.0	11.5	
Propagation Delay Time ($\overline{CLR}$ - Q)*	t_{pHL}	Fig. 4	3.3 ± 0.3	15	−	8.9	13.6	1.0	16.0	
				50	−	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	−	5.5	9.0	1.0	10.5	
				50	−	7.0	11.0	1.0	12.5	
Propagation Delay Time ($\overline{CLR}$ - CARRY)*	t_{pHL}	Fig. 4	3.3 ± 0.3	15	−	8.4	13.2	1.0	15.5	
				50	−	10.9	16.7	1.0	19.0	
			5.0 ± 0.5	15	−	5.0	8.6	1.0	10.0	
				50	−	6.5	10.6	1.0	12.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	80	130	−	70	−	MHZ
				50	55	85	−	50	−	
			5.0 ± 0.5	15	135	185	−	115	−	
				50	95	125	−	85	−	
Input Capacitance	C_{IN}				−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			−	23	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

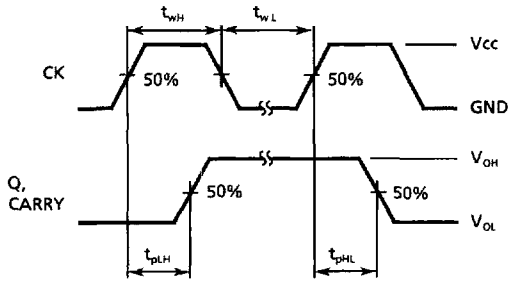
$$\triangle I_{cc} = f_{CK} \cdot V_{cc} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CK.

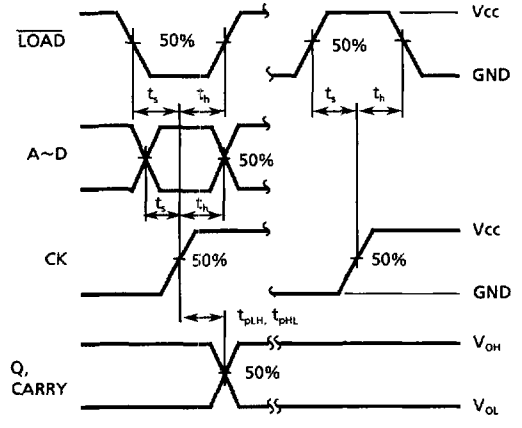
(2) * for TC74VHC161 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

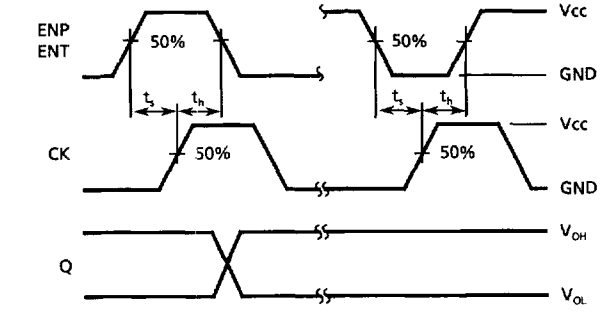
COUNT MODE (Fig. 1)



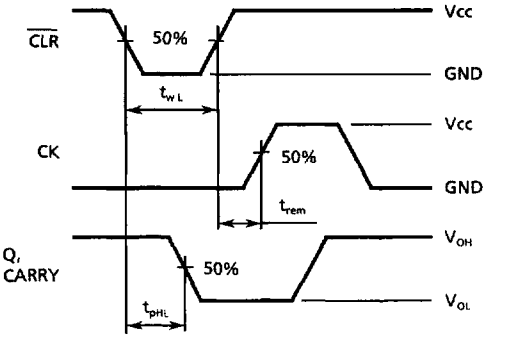
PRESET MODE (Fig. 2)



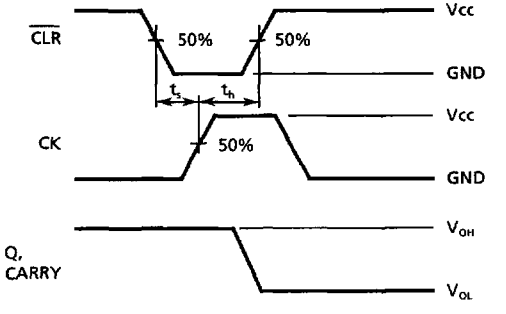
COUNT ENABLE MODE (Fig. 3)



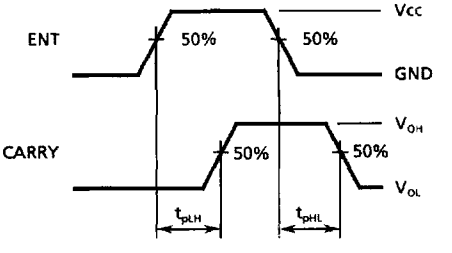
CLEAR MODE (TC74VHC161) (Fig. 4)



CLEAR MODE (TC74VHC163) (Fig. 5)



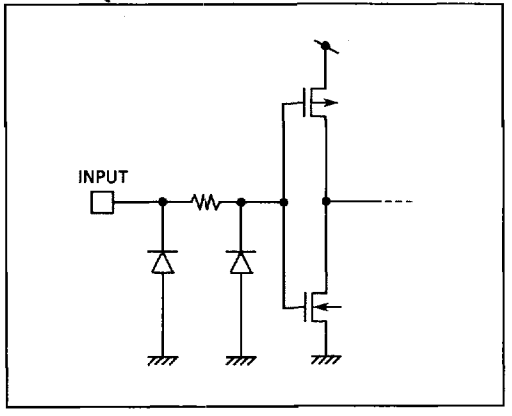
CASCADE MODE (Fix Maximum Count) (Fig. 6)



NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	−0.4	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	−	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	−	1.5	V

INPUT EQUIVALENT CIRCUIT



TYPICAL APPLICATION