TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC9125P, TC74VHC9125FK
TC74VHC9126P, TC74VHC9126FK

TC74VHC9125P/FK 5-bit Universal Schmitt Buffer with 3-State Outputs
TC74VHC9126P/FK 5-bit Universal Schmitt Buffer with 3-State Outputs

The TC74VHC9125/9126 are an ultra-high-speed 5-bit Schmitt buffer fabricated using silicon-gate CMOS technology. The TC74VHC9125/9126 combines low power consumption of CMOS with Schottky TTL speeds.

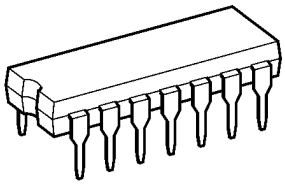
Y1 to Y4 outputs can be put in the high-impedance state by placing a logic HIGH on the Enable ($\overline{G}$) input. The CONT input determines the logical inversion of data. A logic LOW on the CONT input configures the TC74VHC9125/9126 as an inverter; a logic HIGH on the CONT input configures the TC74VHC9125/9126 as a buffer.

TC74VHC9125 Y5 output is an inverting type, and the TC74VHC9126 Y5 output is a non-inverting type.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9125/9126 are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

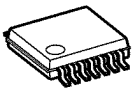
Additionally, all the inputs have a newly developed protection circuit without a diode returned to V_{CC}. This enables the inputs to be tolerant of up to 5 volts even when power supply is down. The input power-down protection capability makes the TC74VHC9125/9126 ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

TC74VHC9125P, TC74VHC9126P



DIP14-P-300-2.54

TC74VHC9125FK, TC74VHC9126FK



VSSOP14-P-0030-0.50

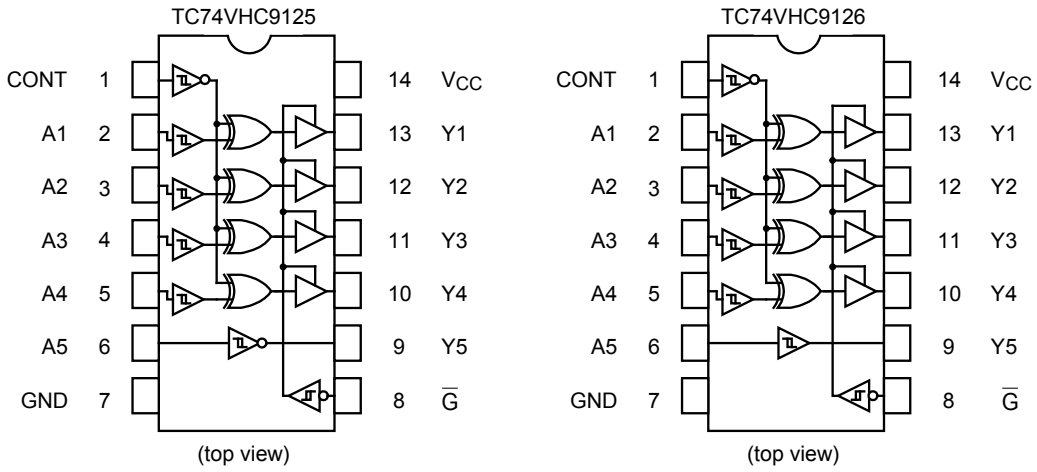
Weight
DIP14-P-300-2.54: 0.96 g (typ.)
VSSOP14-P-0030-0.50: 0.02 g (typ.)

Features

- High speed: t_{pd} = 5.0 ns (typ.) (V_{CC} = 5 V)
- Low supply current: I_{CC} = 2 μA (max) (Ta = 25°C)
- All inputs are provided with power-down protection.
- Symmetrical rise and fall delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V

Start of commercial production
2009-04

Pin Assignment



Truth Table

Inputs			Outputs
$\overline{G}$	CONT	A1 to A4	Y1 to Y4
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

Inputs	Outputs	
A5	Y5(9125)	Y5(9126)
L	H	L
H	L	H

X : Don't care

Z : High impedance

Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180(VSSOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
Positive threshold voltage	V_P	—		3.0	—	—	2.20	—	2.20	V
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	—	0.90	—	
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V_H	—		3.0	0.30	—	1.20	0.30	1.20	V
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (A1 to 4 - Y1 to 4)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	6.0	8.0	1.0	10.0	ns
				50	—	9.0	12.5	1.0	15.0	
			5.0 ± 0.5	15	—	5.0	5.5	1.0	7.0	
				50	—	7.0	8.5	1.0	10.0	
Propagation delay time (CONT-Y1 to 4)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.5	11.5	1.0	13.5	ns
				50	—	13.0	17.0	1.0	20.5	
			5.0 ± 0.5	15	—	6.5	8.0	1.0	9.5	
				50	—	10.5	12.5	1.0	15.0	
Propagation delay time (A5 – Y5)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	6.0	8.0	1.0	10.0	ns
				50	—	9.0	12.5	1.0	15.0	
			5.0 ± 0.5	15	—	5.0	5.5	1.0	7.0	
				50	—	7.0	8.5	1.0	10.0	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	3.3 ± 0.3	15	—	6.0	8.0	1.0	9.5	ns
				50	—	10.5	13.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.5	5.5	1.0	6.5	
				50	—	9.0	10.5	1.0	12.5	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	3.3 ± 0.3	50	—	12.5	13.5	1.0	16.0	ns
			5.0 ± 0.5	50	—	9.0	9.5	1.0	11.0	
Output to output skew (A1 to 4 - Y1 to 4)	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—	—	—	—	4	10	—	10	pF
Output capacitance	C_{OUT}	—	—	—	—	6	—	—	—	pF
Power dissipation capacitance (Note 2)	C_{PD}	f_{IN} = 1 MHz	—	—	—	10	—	—	—	pF

Note 1: Parameter guaranteed by design.

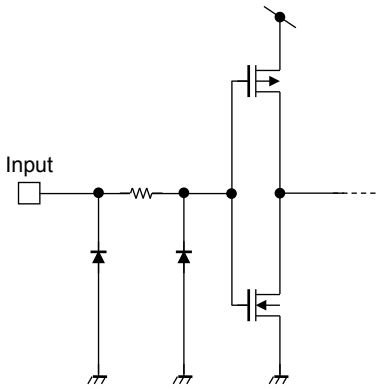
$$t_{osLH} = |t_{pLHm} - t_{pLHn}|,\ t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

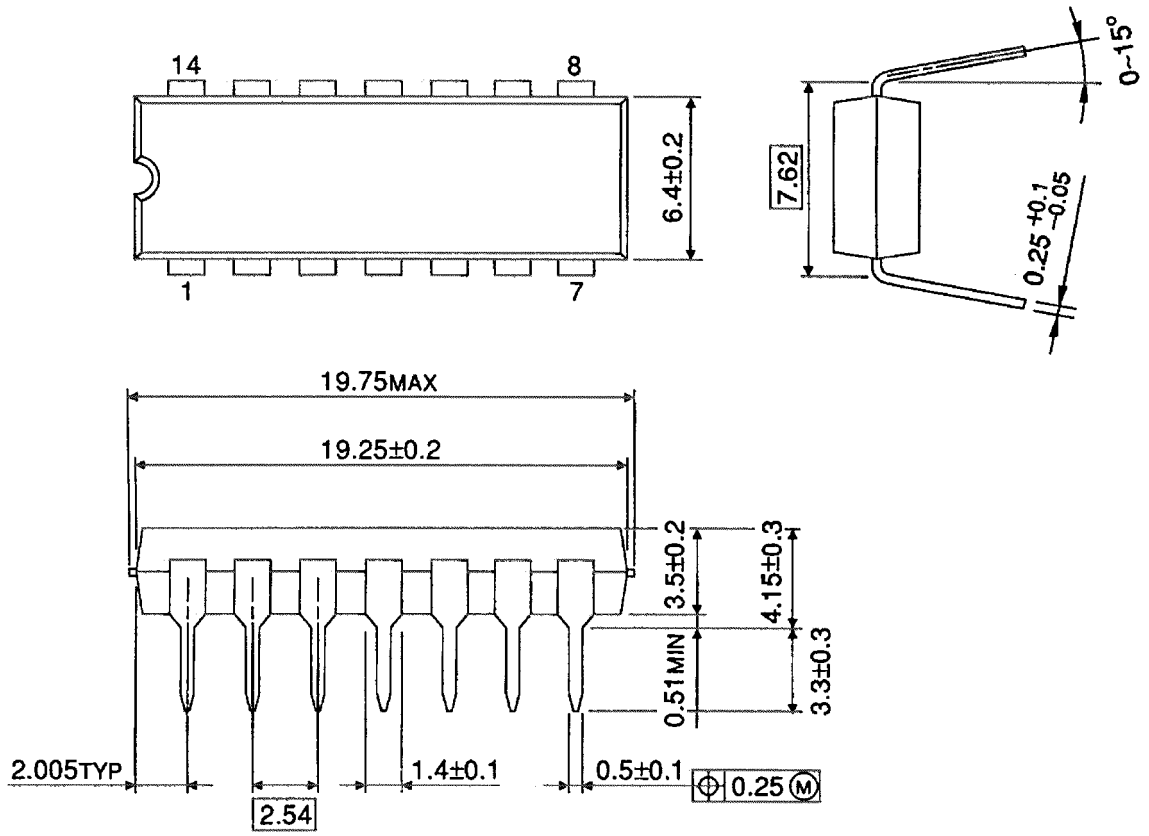
$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 5 \text{ (per bit)}$$

Input Equivalent Circuit



Package Dimensions

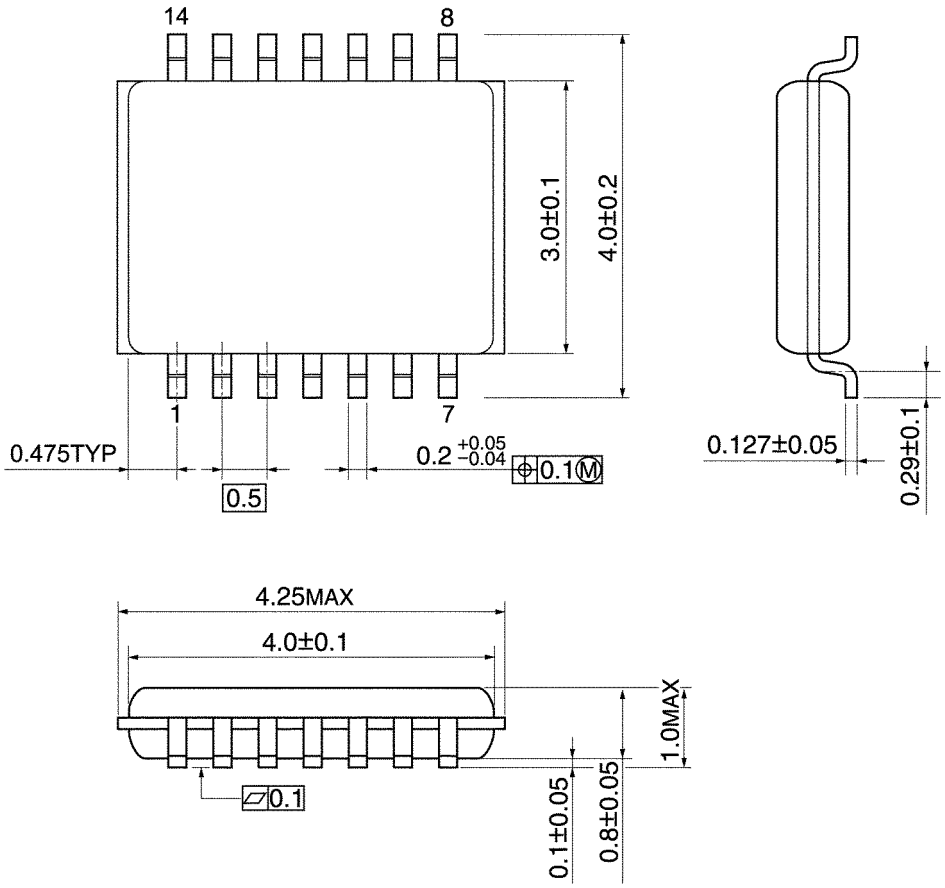
DIP14-P-300-2.54 Unit : mm



Weight: 0.96 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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