TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCT9273P, TC74VHCT9273FK

Octal D-Type Flip Flop with Clear

The TC74VHCT9273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

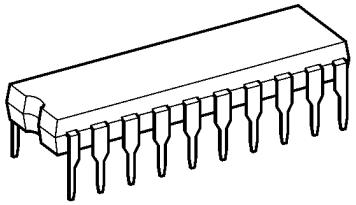
When the $\overline{CLR}$ input is held “L”, the Q outputs are at a low logic level independent of the other inputs.

The $\overline{CLR}$ input and CK input have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCT9273 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

It is easy to wire on the board because Input terminals are at the opposite side of Output terminals.

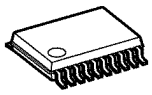
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage.

TC74VHCT9273P



DIP20-P-300-2.54A

TC74VHCT9273FK



VSSOP20-P-0030-0.50

Weight

DIP20-P-300-2.54A : 1.30 g (typ.)

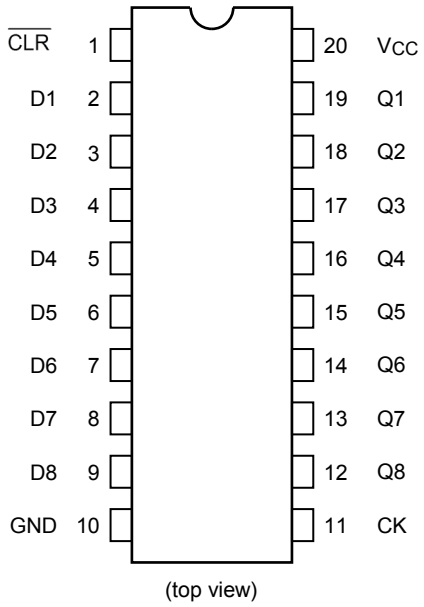
VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Features

- High speed: f_{max} = 185 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Compatible with TTL inputs
  : V_{IL} = 0.5 V (max)
  V_{IH} = 2.1 V (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Function compatible with 74VHC273
- Input terminals are at the opposite side of Output terminals

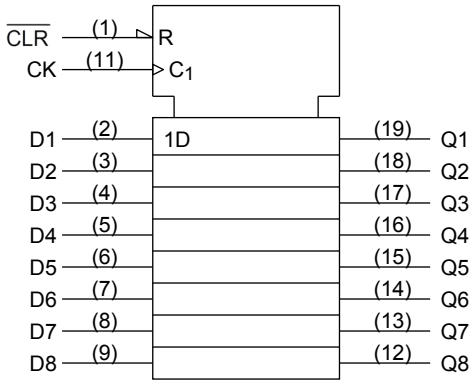
Start of commercial production
2009-04

Pin Assignment



(top view)

IEC Logic Symbol

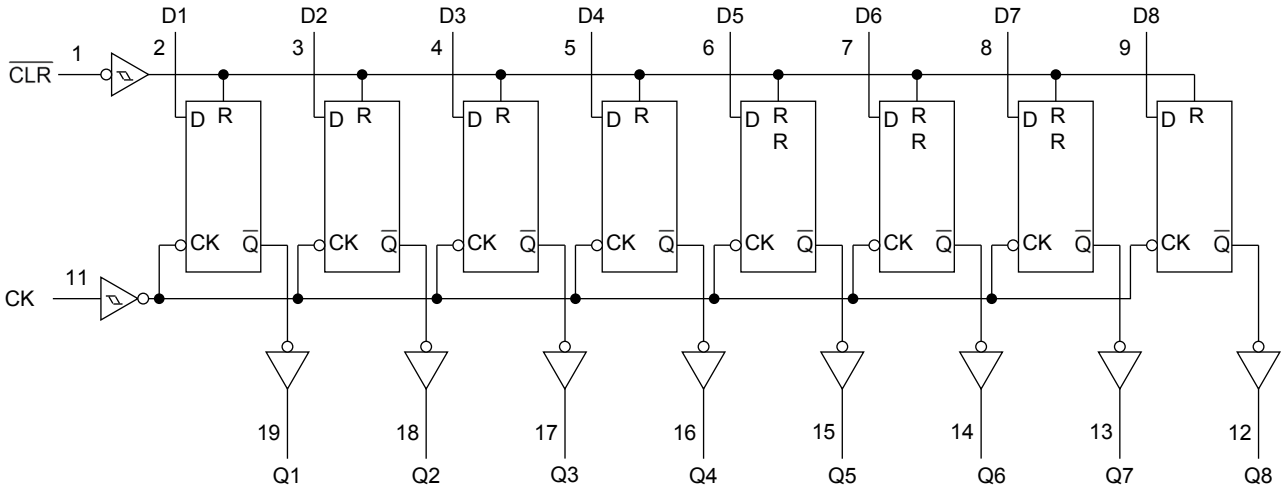


Truth Table

Inputs			Output	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180(VSSOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Positive threshold voltage	V_P	—		4.5 5.5	— —	— —	1.90 2.10	— —	1.90 2.10	V
Negative threshold voltage	V_N	—		4.5 5.5	0.50 0.60	— —	— —	0.50 0.60	— —	V
Hysteresis voltage (CK、$\overline{CLR}$)	V_H	—		4.5 5.5	0.40 0.40	— —	1.40 1.50	0.40 0.40	1.40 1.50	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width (CK)	$t_{w\ (L)}$ $t_{w\ (H)}$	—	5.0 ± 0.5	—	5.0	5.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{w\ (L)}$	—	5.0 ± 0.5	—	5.0	5.0	ns
Minimum set-up time	t_s	—	5.0 ± 0.5	—	4.5	4.5	ns
Minimum hold time	t_h	—	5.0 ± 0.5	—	1.0	1.0	ns
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	5.0 ± 0.5	—	2.0	2.0	ns

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	4.7	8.9	1.0	10.2	ns
				50	—	7.6	14.1	1.0	16.1	
Propagation delay time ($\overline{CLR}$ -Q)	t_{pHL}	—	5.0 ± 0.5	15	—	7.5	14.4	1.0	16.4	ns
				50	—	10.4	19.6	1.0	22.3	
Maximum clock frequency	f_{max}	—	5.0 ± 0.5	15	110	185	—	95	—	MHz
				50	70	100	—	60	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note 2)			—	13	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|,\ t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

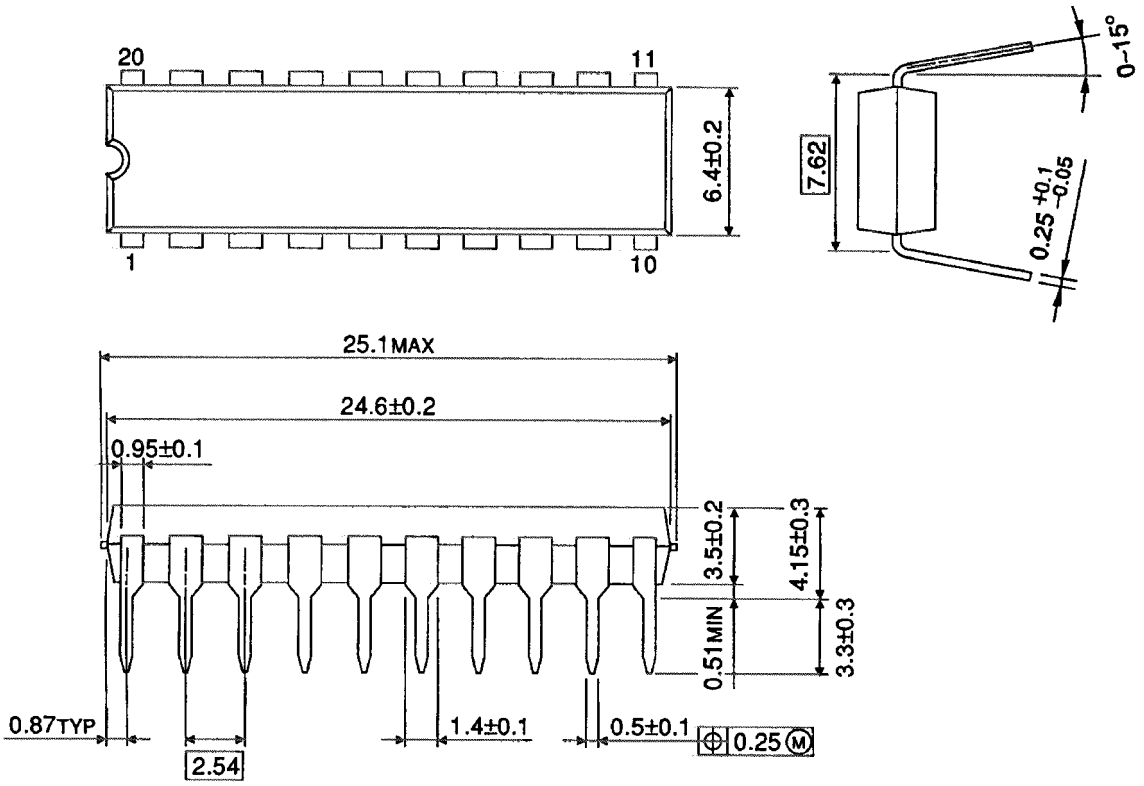
And the total C_{PD} when n pcs.of flip flop operate can be gained by the following equation:

$$C_{PD}\ (\text{total}) = 9 + 4 \cdot n$$

Package Dimensions

DIP20-P-300-2.54A

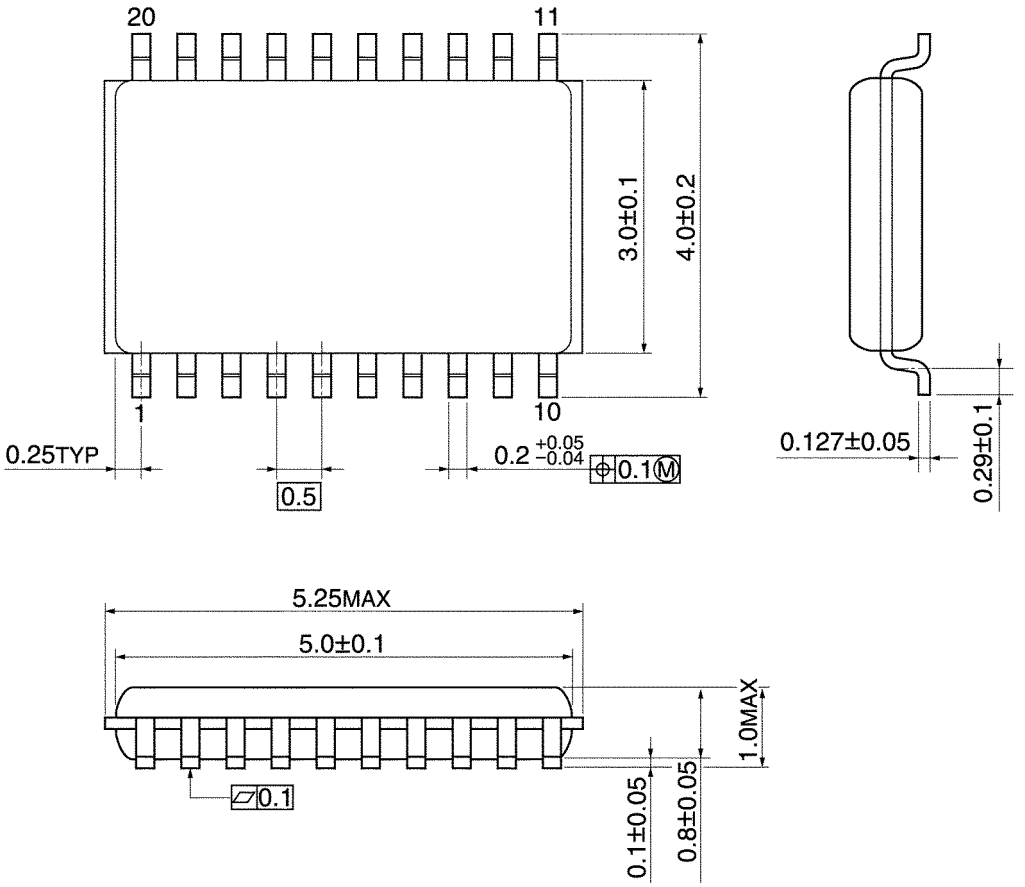
Unit : mm



Weight: 1.30 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)

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