TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

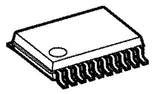
TC74VHCV574FK

Octal Schmitt D-Type Flip Flop with 3-State Output

The TC74VHCV574FK is advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate CMOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{\mathrm{OE}}$).
When the $\overline{\mathrm{OE}}$ input is high, the eight outputs are in a high impedance state.
Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCV574FK is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state.

TC74VHCV574FK



VSSOP20-P-0030-0.50

Weight
VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Features

- High speed: f_{max} = 180 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Wide operating voltage range: $V_{CC\ (opr)}$ = 1.8 V to 5.5 V
- Ouput current: $|I_{OH}|/I_{OL}$ = 16 mA (min) (V_{CC} = 4.5 V)
- Available in VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 574 type

Start of commercial production
2010-01

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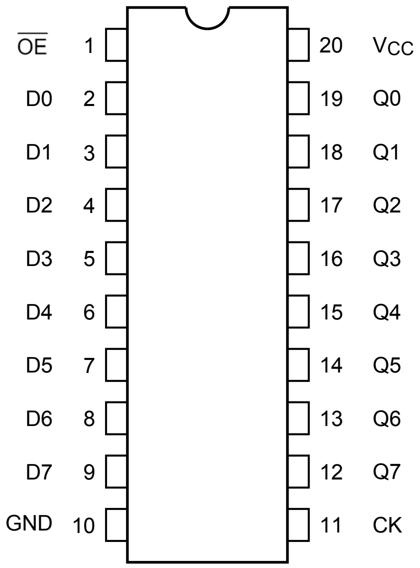
Pin Assignment



(top view)

Truth Table

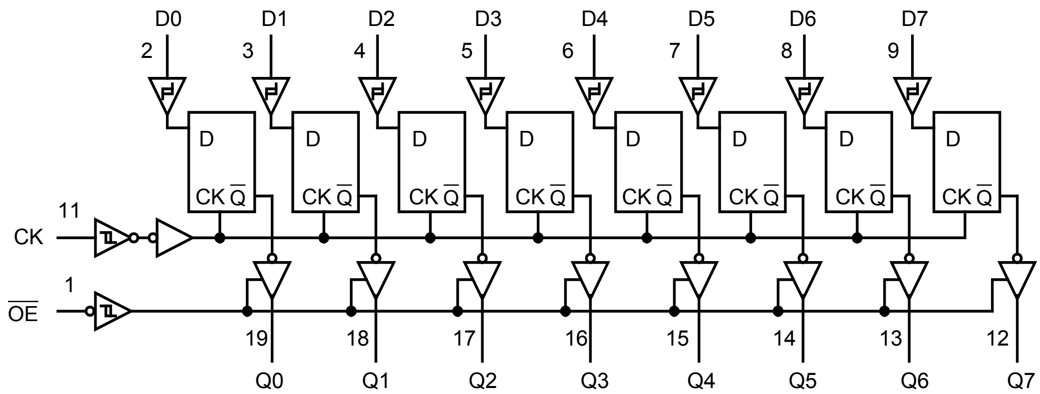
Inputs			Output
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Qn: No change

System Diagram



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Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to 7.0 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 5.5	V
Input voltage (DIR, $\overline{OE}$)	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 2)	V
		0 to V_{CC} (Note 3)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 20 (V_{CC} = 3.3 ± 0.3V) 0 to 1 (V_{CC} = 5 ± 0.5V)	ms/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in off-state

Note 3: High or low state.

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Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Positive threshold voltage	V_P	—		1.8	—	—	1.65	—	1.65	V
				2.3	—	—	1.85	—	1.85	
				3.0	—	—	2.20	—	2.20	
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	—	0.15	—	
				2.3	0.45	—	—	0.45	—	
				3.0	0.90	—	—	0.90	—	
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	—	1.05	0.15	1.05	V
				2.3	0.20	—	1.10	0.20	1.10	
				3.0	0.30	—	1.20	0.30	1.20	
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	1.8	1.7	1.8	—	1.7	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −8 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −16 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.8	—	0.0	0.1	—	0.1	
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 8 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 16 mA	4.5	—	—	0.44	—	0.55	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5V		1.8 to 5.5	—	—	±0.5	—	±5.0	μA
Power-off leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA

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Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{w (H)}$ $t_{w (L)}$	—	2.5 ± 0.2	—	7.0	7.0	ns
			3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t_s	—	2.5 ± 0.2	—	5.5	5.5	ns
			3.3 ± 0.3	—	3.5	3.5	
			5.0 ± 0.5	—	3.5	3.5	
Minimum hold time	t_h	—	2.5 ± 0.2	—	2.0	2.0	ns
			3.3 ± 0.3	—	1.5	1.5	
			5.0 ± 0.5	—	1.5	1.5	

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AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	2.5 ± 0.2	15	—	9.1	16.6	1.0	20.0	ns
				50	—	11.9	19.6	1.0	23.0	
			3.3 ± 0.3	15	—	6.7	13.2	1.0	15.5	
				50	—	8.9	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.0	8.6	1.0	10.0	
				50	—	6.7	10.6	1.0	12.0	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	2.5 ± 0.2	15	—	7.6	16.1	1.0	19.0	ns
				50	—	10.7	19.0	1.0	22.0	
			3.3 ± 0.3	15	—	5.7	12.8	1.0	15.0	
				50	—	8.1	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	4.2	9.0	1.0	10.5	
				50	—	6.1	11.0	1.0	12.5	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	2.5 ± 0.2	50	—	13.6	17.5	1.0	20.0	ns
			3.3 ± 0.3	50	—	10.5	15.0	1.0	17.0	
			5.0 ± 0.5	50	—	8.2	10.1	1.0	11.5	
Maximum clock frequency	f_{max}	—	2.5 ± 0.2	15	60	95	—	50	—	MHz
				50	50	75	—	40	—	
			3.3 ± 0.3	15	80	135	—	65	—	
				50	55	100	—	45	—	
			5.0 ± 0.5	15	130	180	—	110	—	
				50	85	135	—	75	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	2.5 ± 0.2	50	—	—	2.0	—	2.0	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	6	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)			—	26	—	—	—	pF

Note 1: Parameter guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

C_{PD} (total) = 14 + 12·n

Noise Characteristics (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Max	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	3.3 5.0	0.4 0.8	— —	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	3.3 5.0	-0.1 -0.4	— —	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

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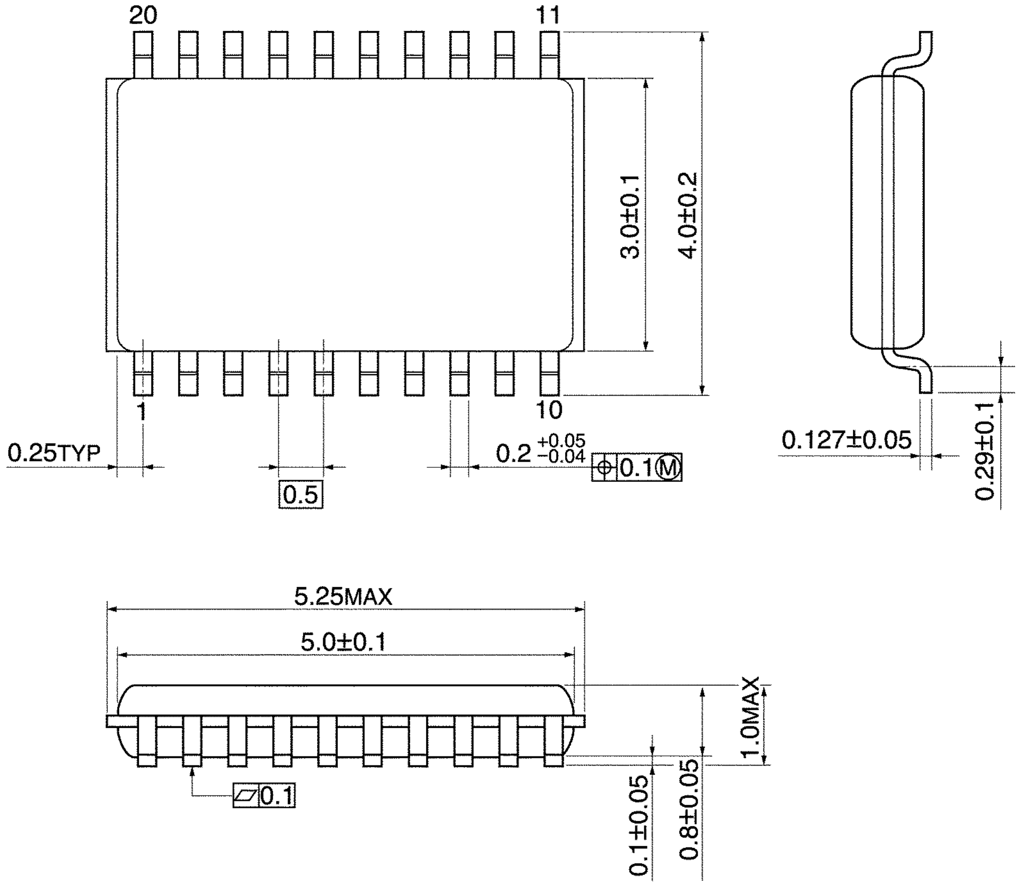
Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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