MICROCHIP

EVALUATION KIT AVAILABLE

TC7662B

CHARGE PUMP DC-TO-DC VOLTAGE CONVERTER

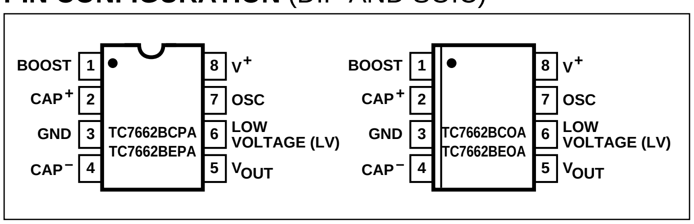
FEATURES

- **Wide Operating Voltage Range: 1.5V to 15V**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- **High Power Efficiency is 96%**
- **Easy to Use – Requires Only 2 External Non-Critical Passive Components**
- **Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices**

APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems and Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

PIN CONFIGURATION (DIP AND SOIC)



GENERAL DESCRIPTION

The TC7662B is a pin-compatible upgrade to the Industry standard TC7660 charge pump voltage converter. It converts a +1.5V to +15V input to a corresponding – 1.5 to – 15V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI.

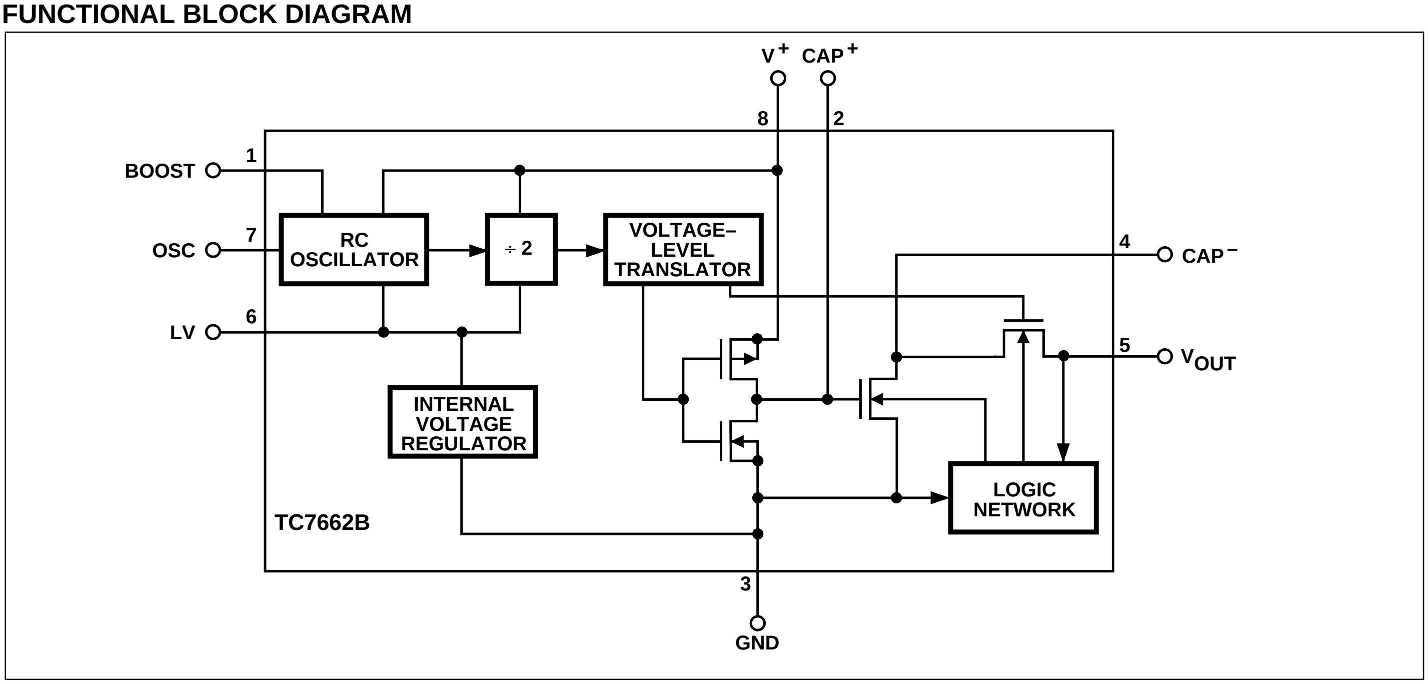
The on-board oscillator operates at a nominal frequency of 10kHz. Frequency is increased to 35kHz when pin 1 is connected to V^+, allowing the use of smaller external capacitors. Operation below 10kHz (for lower supply current applications) is also possible by connecting an external capacitor from OSC to ground (with pin 1 open).

The TC7662B is available in both 8-pin DIP and 8-pin small outline (SO) packages in commercial and extended temperature ranges.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7662BCOA	8-Pin SOIC	0°C to +70°C
TC7662BCPA	8-Pin Plastic DIP	0°C to +70°C
TC7662BEOA	8-Pin SOIC	– 40°C to +85°C
TC7662BEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660EV	***Evaluation Kit for Charge Pump Family***	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage .... +16.5V
LV, Boost and OSC Inputs Voltage (Note 1)
  $V+<5.5V$ .... – 0.3V to (V^+ + 0.3V)
  $>5.5V$ .... (V^+ – 5.5V) to (V^+ + 0.3V)
Current Into LV (Note 1)
  V^+ >3.5V 20µA
Output Short Duration
  ($V_{SUPPLY} \le 5.5V$) .... Continuous
Power Dissipation ($T_A \le$ **70°C)** (Note 2)
  Plastic DIP 730mW
  SO 470mW
Operating Temperature Range
  C Suffix .... 0°C to +70°C
  E Suffix .... – 40°C to +85°C
Storage Temperature Range .... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V^+ = 5V, T_A = +25°C, OSC = Free running, Test Circuit Figure 2, Unless Otherwise Specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current (Note 3)	$R_L = \infty$, +25°C	—	80	160	µA
	(Boost pin OPEN OR GND)	$0°C \le T_A \le +70°C$	—	—	180	µA
		$-40°C \le T_A \le +85°C$	—	—	180	µA
		$-55°C \le T_A \le +125°C$	—	—	200	µA
I^+	Supply Current (Boost pin = V+)	$0°C \le T_A \le +70°C$ $-40°C \le T_A \le +85°C$ $-55°C \le T_A \le +125°C$	—	—	300 350 400	µA
V^+_H	Supply Voltage Range, High (Note 4)	R_L = 10 kΩ, LV Open, $T_{MIN} \le T_A \le T_{MAX}$	3.0	—	15	V
V^+_L	Supply Voltage Range, Low	R_L = 10 kΩ, LV to GND, $T_{MIN} \le T_A \le T_{MAX}$	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA, $0°C \le T_A \le +70°C$	—	65	100	Ω
		I_{OUT} = 20mA, $-40°C \le T_A \le +85°C$	—	—	120	Ω
		I_{OUT} = 20mA, $-55°C \le T_A \le +125°C$	—	—	150	Ω
		I_{OUT} = 3mA, V^+ = 2V, LV to GND , $0°C \le T_A \le +70°C$	—	—	250	Ω
		I_{OUT} = 3mA, V^+ = 2V, LV to GND , $-40°C \le T_A \le +85°C$	—	—	300	Ω
		I_{OUT} = 3mA, V^+ = 2V, LV to GND , $-55°C \le T_A \le +125°C$	—	—	400	Ω
f_{OSC}	Oscillator Frequency	C_{OSC} = 0,Pin 1 Open or GND Pin 1 = V^+	5	10 35	—	kHz
P_{Eff}	Power Efficiency	R_L = 5kΩ $T_{MIN} \le T_A \le T_{MAX}$	96 95	96 97	—	%
V_{OUT}Eff	Voltage Conversion Efficiency	$R_L = \infty$	99	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

NOTES:
1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the TC7662B.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The TC7662B can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

DETAILED DESCRIPTION

The TC7662B contains all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors which may be inexpensive 1μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage V^+ for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The TC7662B approaches this ideal situation more closely than existing non-mechanical circuits.

In the TC7662B, the four switches of Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

The problem is eliminated in the TC7662B by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TC7662B is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation, the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts, the LV terminal must be left open to insure latchup proof operation and prevent device damage.

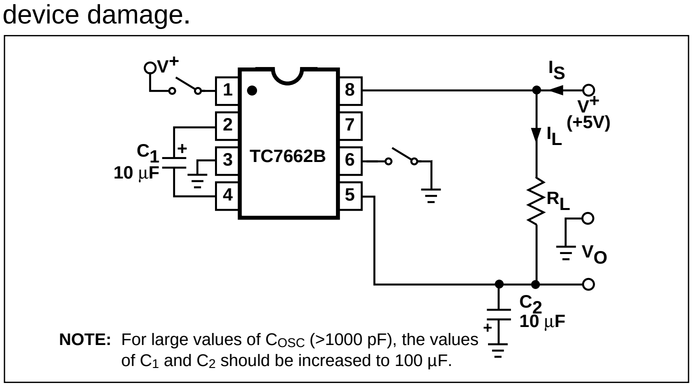


Figure 1. TC7662B Test Circuit

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

A. The drive circuitry consumes minimal power.

B. The output switches have extremely low ON resistance and virtually no offset.

C. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7662B approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect the LV terminal to GND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for voltages above 5.5 volts for extended periods; however, transient conditions including start-up are okay.

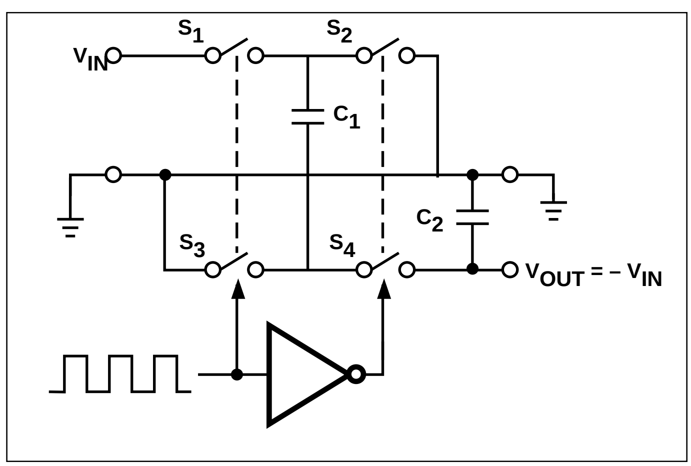


Figure 2. Idealized Negative Voltage Capacitor

4. When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7662B and the – terminal of C_2 must be connected to GND.
5. If the voltage supply driving the TC7662B has a large source impedance (25-30 ohms), then a 2.2µF capacitor from pin 8 to ground may be required to limit the rate of rise of the input voltage to less than 2V/µsec.

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the TC7662B for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply where a positive supply of +1.5V to +15V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

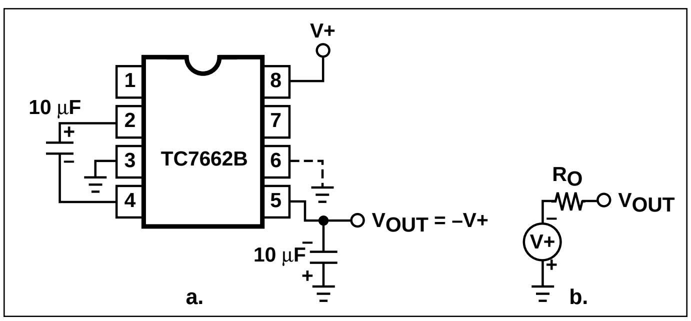


Figure 3. Simple Negative Converter and its Output Equivalent

The output characteristics of the circuit in Figure 3 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3b. The voltage source has a value of–(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, \ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 >$ 10µF and there is not enough time to fully charge the capacitors every cycle. In a typical application when f_{OSC} = 10kHz and $C = C_1 = C_2$ = 10µF:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_O \cong (46 + 20 + 5 \times ESR_C)\ \Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is $2 \times I_{OUT}$, hence the total drop is $2 \times I_{OUT} \times ESR_{C2}$ volts. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is $I_{OUT} \times t_2/C_2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + ESR_{C2} \times I_{OUT} \right)$$

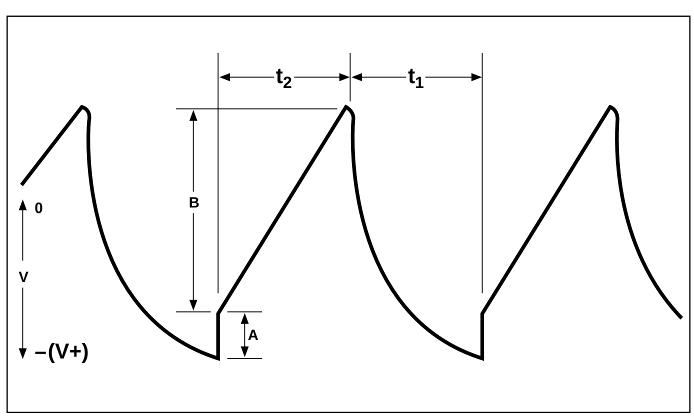


Figure 4. Output Ripple

Paralleling Devices

Any number of TC7662B voltage converters may be paralleled to reduce output resistance (Figure 5). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of TC7662B)}}{n \text{ (number of devices)}}$$

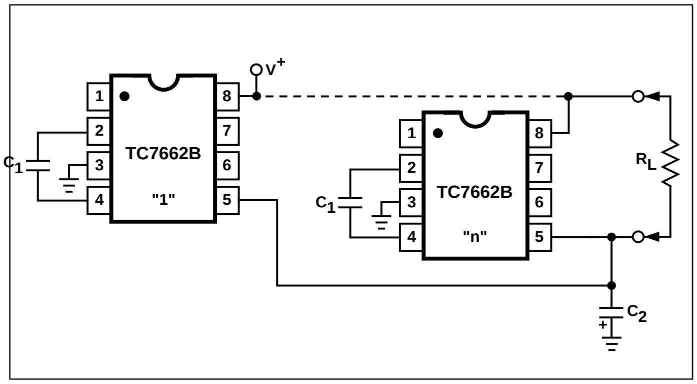


Figure 5. Paralleling Devices

Cascading Devices

The TC7662B may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -\,n(V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7662B R_{OUT} values.

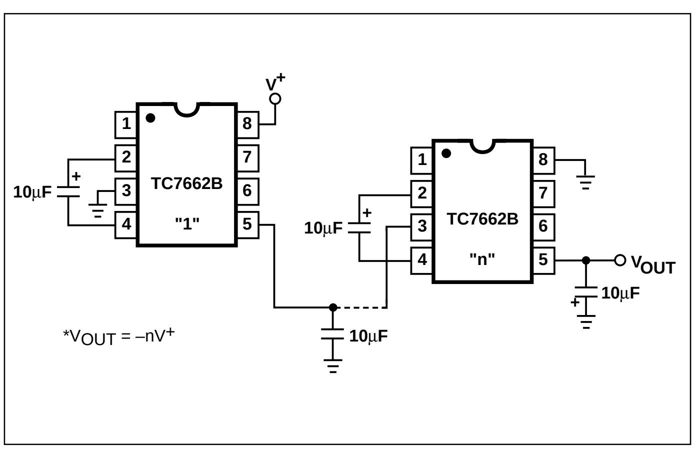


Figure 6. Cascading Devices for Increased Output Voltage

Changing the TC7662B Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by one of several methods described below:

By connecting the BOOSTPin (Pin 1) to V^+, the oscillator charge and discharge current is increased and, hence the oscillator frequency is increased by approximately 3-1/2 times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, e.g., 0.1µF, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 1\mu F$ or 10µF. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock as shown in Figure 7. In order to prevent device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

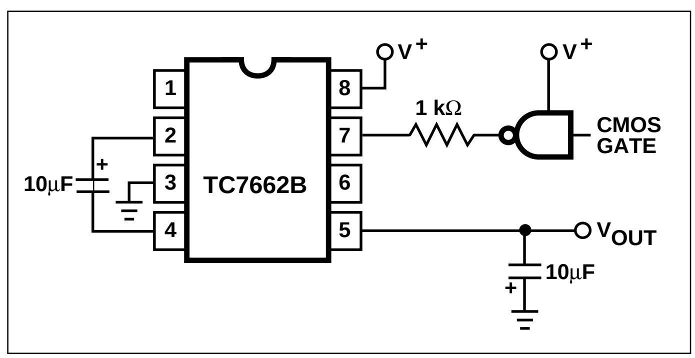


Figure 7. External Clocking

It is also possible to increase the conversion efficiency of the TC7662B at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

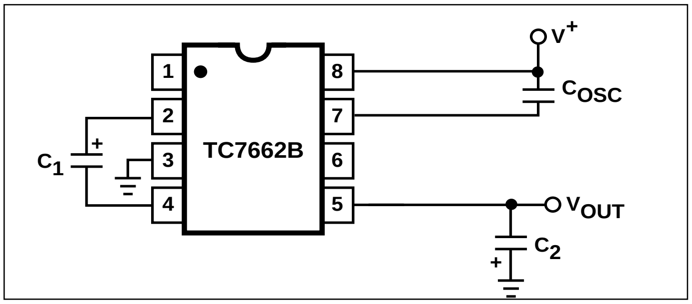


Figure 8. Lowering Oscillator Frequency

Positive Voltage Doubling

The TC7662B may be employed to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the TC7662B are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage on C_1 plus the supply voltage (V^+) applied through diode D_2 to capacitor C_2). The voltage thus created on C_2 becomes $(2\,V^+) - (2\,V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

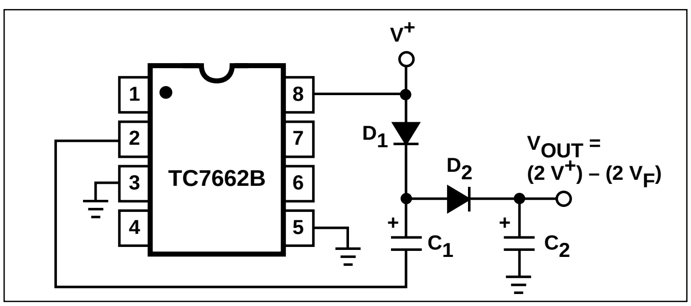


Figure 9. Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 3 and 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

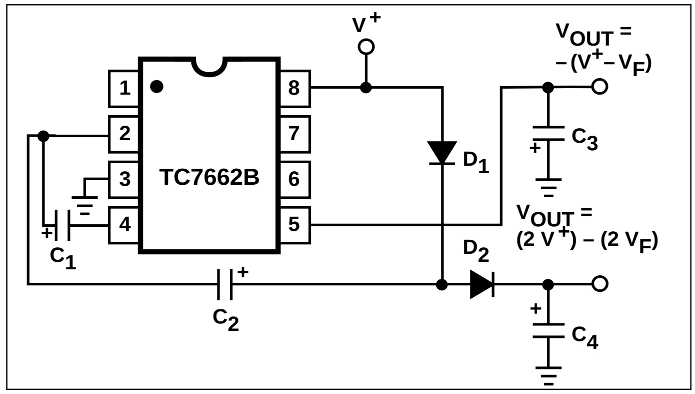


Figure 10. Combined Negative Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

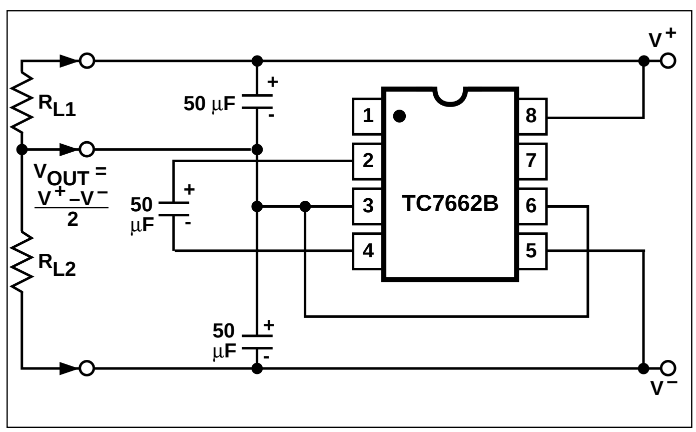


Figure 11. Splitting a Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the TC7662B can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is advisable, since the TC7662B's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the TC7662B, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provide an output impedance of less than 5Ω to a load of 10mA.

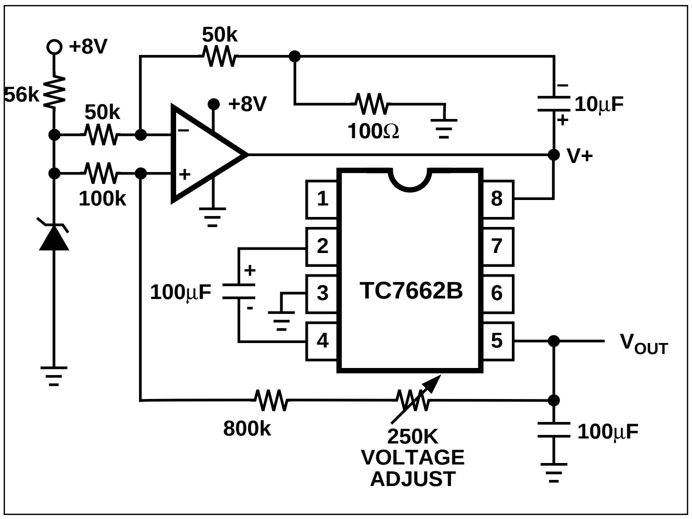


Figure 12. Regulating the Output Voltage

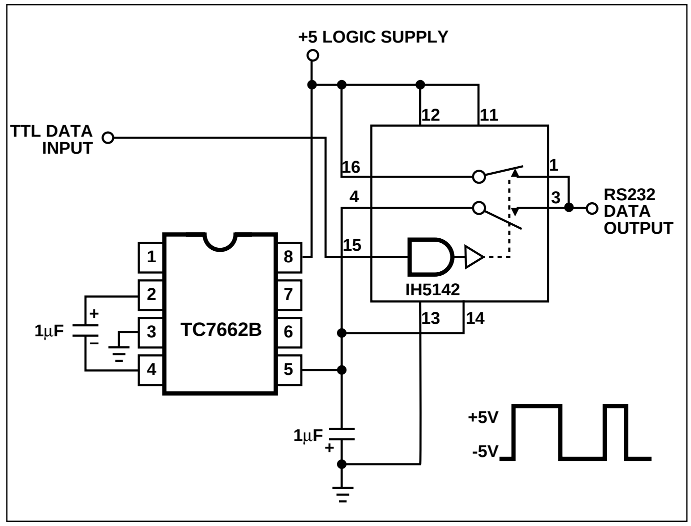
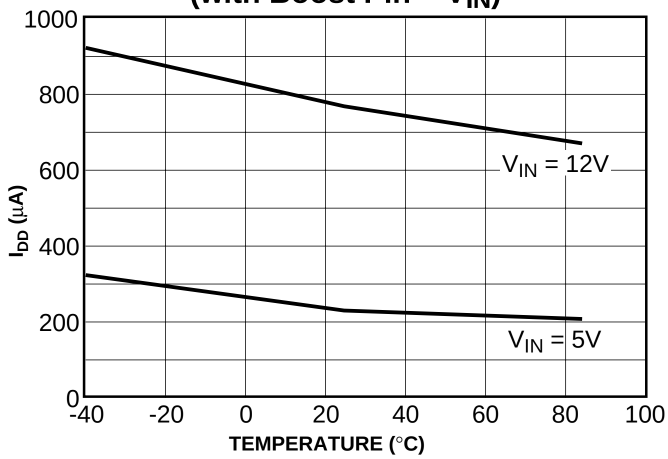


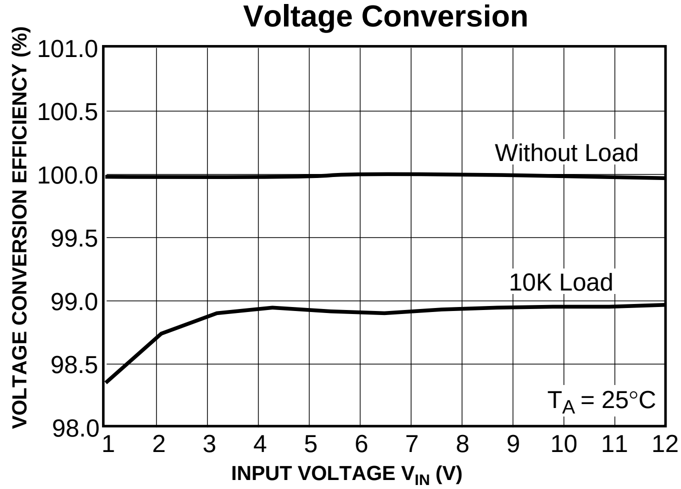
Figure 13. RS232 Levels from a Single 5V Supply

TYPICAL CHARACTERISTICS

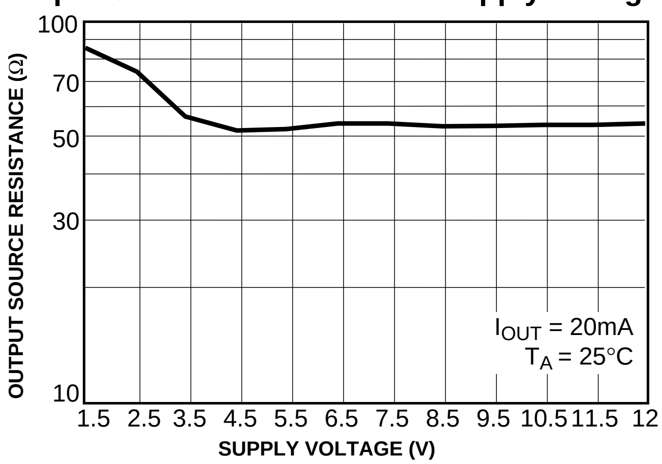
Supply Current vs. Temperature (with Boost Pin = V_{IN})



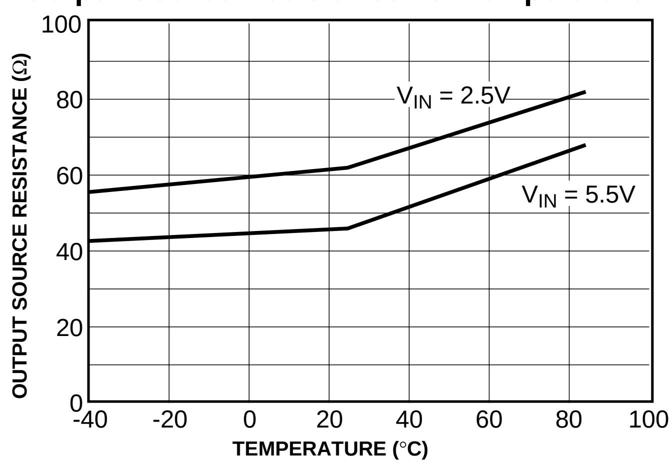
Voltage Conversion



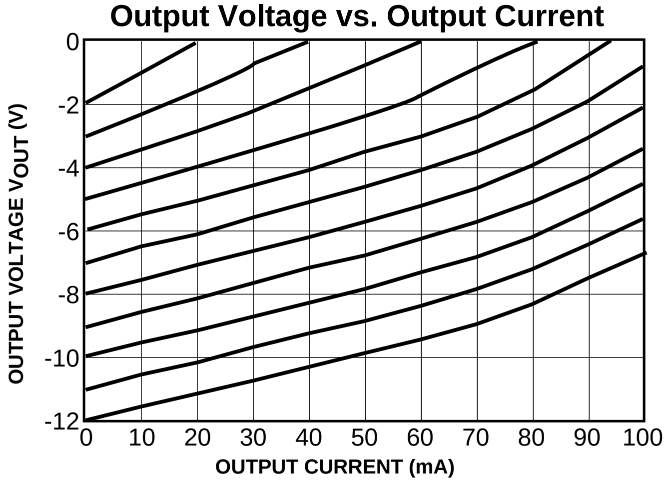
Output Source Resistance vs. Supply Voltage



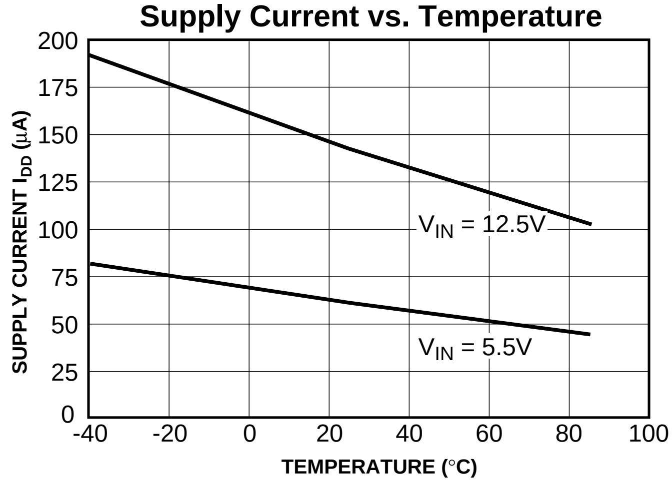
Output Source Resistance vs. Temperature



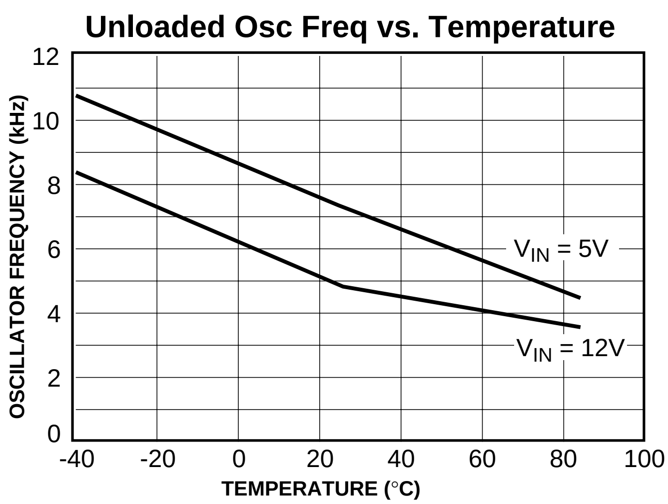
Output Voltage vs. Output Current

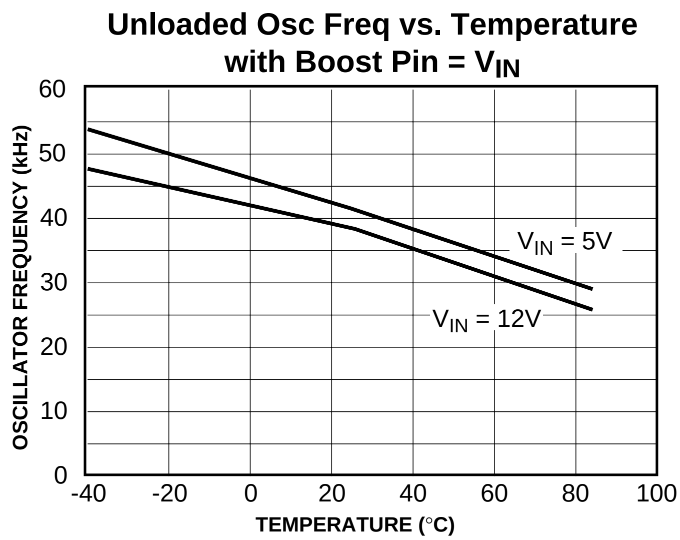


Supply Current vs. Temperature



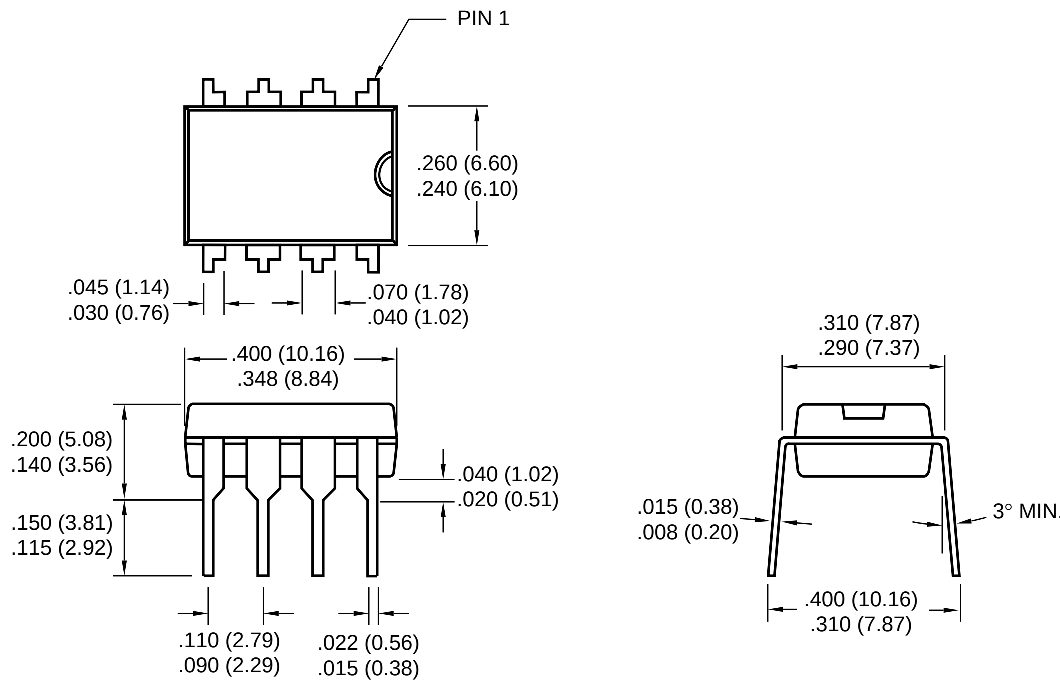
TYPICAL CHARACTERISTICS *(cont.)*





PACKAGE DIMENSIONS

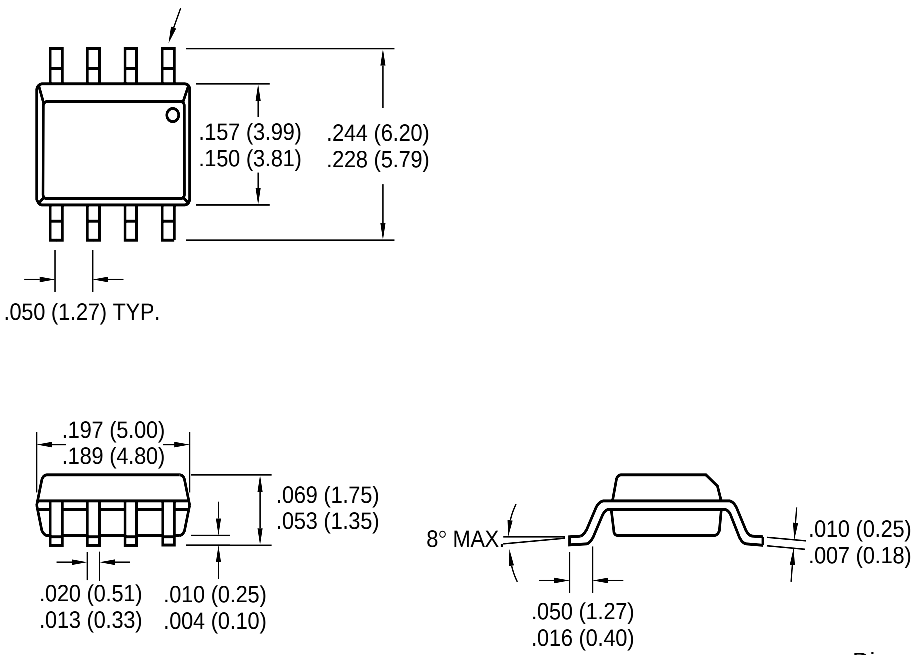
8-Pin Plastic DIP



Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

8-Pin SOIC



Dimensions: inches (mm)

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