

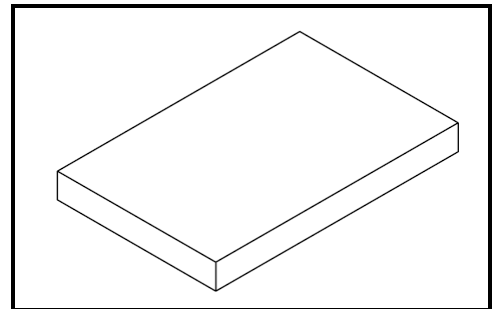
TOSHIBA CDMOS Integrated Silicon Monolithic Circuit

TC7763WBG

Qi Compliant Wireless Power Receiver Controller IC

1. Outline

The TC7763WBG is wireless power receiver (RX) IC compliant to the Qi low power v1.1 standard of the Wireless Power Consortium (WPC). The TC7763WBG includes a rectifier circuit, a digital control circuit, a modulation circuit, a regulator circuit which controls the supply voltage to the load, and a load switch controller to detect and select an external power supply. A digital control circuit realizes little heat generation and guarantees voltage stabilization during load changes. The IC includes all RX functions needed to construct a standalone wireless power system. The integrated loadswitch driver for external loadswitch allows to bypass the wireless power function when a USB or AC power source is connected to the mobile device.



S-XFLGA28-0304-0.50-001

2. Applications

Mobile communication devices (Smartphone, Featurephone, tablet), battery pack, mobile accessory etc.

3. Features

- Full bridge rectifier circuit
 - Auto switch for 3 modes : Synchronous rectification / Diode rectification / Diode bridge
 - Low ON resistance : Hi Side 45mΩ(Typ.) / Low side 30mΩ(Typ.)
 - Under Voltage Lockout (UVLO) / Over Voltage Detection (OVP) function
- 5V-output LDO
 - Maximum output current : 1.0A
 - 2 step Over Current Detection (OCL) function
- Qi Low Power v1.1 compliant
 - Foreign Object Detection (FOD) function
- External load switch driver for supply selector
- Current drive type startup function
- Under voltage lockout (UVLO) / Over voltage detection (OVLO) function
- Thermal shutdown function (TSD)
- Package : S-XFLGA28-0304-0.50-001 (2.40mm*3.67mm*0.5mm, 0.5mm pitch)

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

4. Block diagram

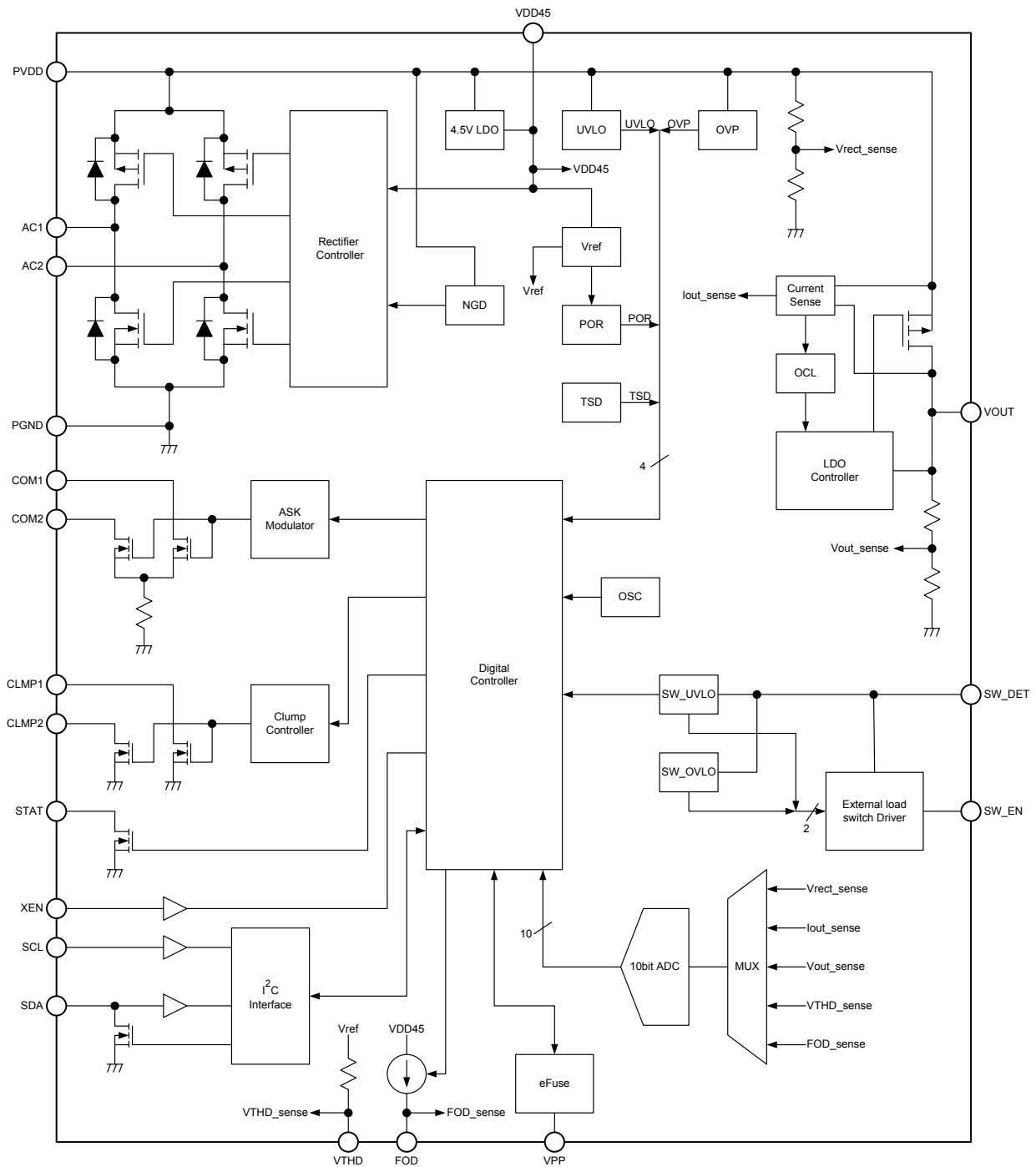


Figure 4.1 Block diagram

5. Pin assignment

| | 1 | 2 | 3 | 4 |
|---|-------|------|-------|--------|
| A | PGND | PGND | PGND | PGND |
| B | AC2 | AC2 | AC1 | AC1 |
| C | CLMP2 | PVDD | PVDD | CLMP1 |
| D | VOUT | VOUT | VOUT | VOUT |
| E | COM2 | SDA | SCL | COM1 |
| F | VDD45 | VPP | SW_EN | SW_DET |
| G | FOD | XEN | STAT | VTHD |

(Top View)

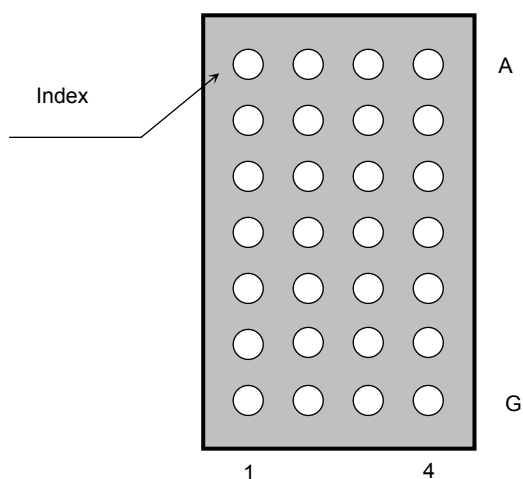


Figure 5.1 Ball assignment (Top View)

6. Pin function

Table 6.1 Pin function

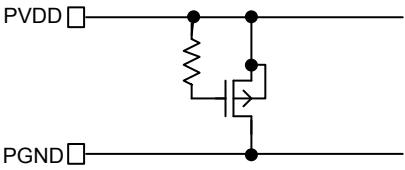
| Pin Number | Pin symbol | I/O | Description |
|------------------|------------|-----|---|
| A1, A2 A3, A4 | PGND | - | Power ground Connect to common ground (GND). |
| B1, B2 | AC2 | I | Antenna terminals for receiver 2 |
| B3, B4 | AC1 | I | Antenna terminals for receiver 1 |
| C1 | CLMP2 | O | Clamp terminal for over voltage protection 2 Open drain terminal. Connect capacitor of 0.47 μ F to AC2. |
| C2, C3 | PVDD | - | Rectifier output and power supply terminal Output of bridge rectifier circuit and IC power supply terminal. Connect smoothing capacitor between PVDD and PGND. |
| C4 | CLMP1 | O | Clamp terminal for over voltage protection 1 Open drain terminal. Connect capacitor of 0.47 μ F to AC1. |
| D1, D2 D3, D4 | VOUT | O | 5V LDO output terminals Connect capacitor of more than 1.0 μ F to GND. |
| E1 | COM2 | O | Capacitor connect for ASK modulation 2 Open drain terminal. Connect capacitor to AC2. |
| E2 | SDA | I/O | I ² C data I/O terminal for Toshiba tests Open drain terminal. Connect to GND. |
| E3 | SCL | I | I ² C clock input terminal for Toshiba tests Connect to GND. |
| E4 | COM1 | O | Capacitor connect for ASK modulation 3 Open drain terminal. Connect capacitor to AC2. |
| F1 | VDD45 | O | 4.5V- LDO output terminal 4.5V- LDO output terminal for internal circuit. Connect capacitor of more than 0.1 μ F to GND. |
| F2 | VPP | I | eFuse writing terminal Short to VDD45 in normal use. |
| F3 | SW_EN | O | External Load switch drive terminal Connect SW_EN to a gate of P-ch MOSFET for load switch. Please Open when you do not use it. |
| F4 | SW_DET | I | External Load switch power supply monitor terminal It monitors input power supply of load switch. Connect SW_DET to second input power supply. Connect to GND when not used. |
| G1 | FOD | I | Offset terminal for RX loss adjustments. Loss offset terminal for FOD Connect appropriate resistor to GND. |
| G2 | XEN | I | LDO enable input terminal When the terminal is "Open" or "L" level, LDO is tuned on. When the terminal is "H" level, LDO is turned off. |
| G3 | STAT | O | Status output terminal Open drain terminal. Connect pull-up resistor. |
| G4 | VTHD | I | Thermal detection terminal Thermistor connect terminal to monitor external temperature. Connect NTC thermistor to GND. Please connect resistance (51k Ω) when not used for temperature variation compensation. |

7. Equivalent circuits for input/output/power supply terminals

7.1 Power supply terminal

Table 7.1 Equivalent circuits for power supply terminals

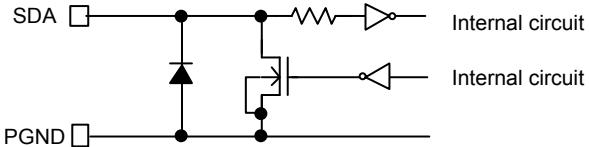
Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|-----------|---|
| PVDD-PGND |  <p>The diagram shows two horizontal lines representing the PVDD and PGND pins. A resistor is connected between the top line (PVDD) and the bottom line (PGND). A diode is also connected between the two lines, with its cathode pointing towards the PGND pin and its anode pointing towards the PVDD pin.</p> |

7.2 Input/output terminal

Table 7.2 Equivalent circuits for Input/output terminals

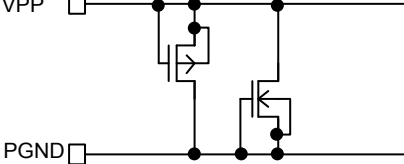
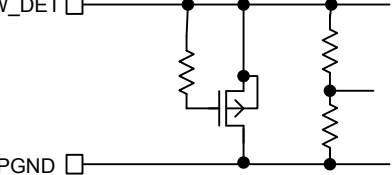
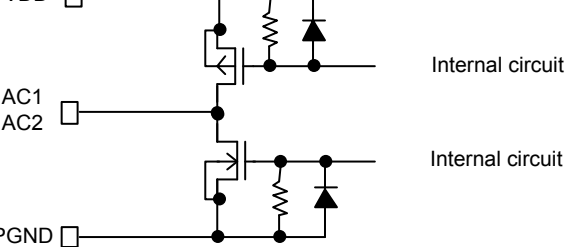
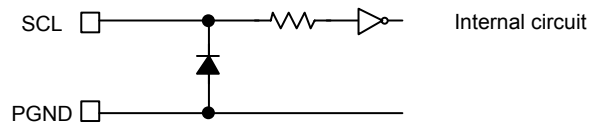
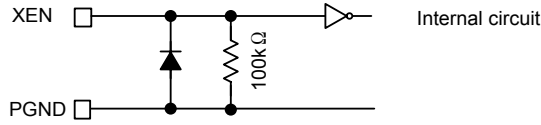
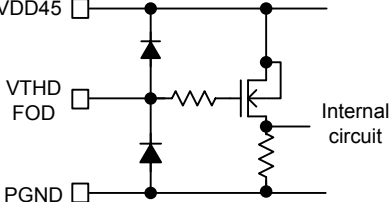
Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|----------|--|
| SDA |  <p>The diagram shows two horizontal lines representing the SDA and PGND pins. A diode is connected between the top line (SDA) and the bottom line (PGND), with its cathode pointing towards the PGND pin. From the SDA pin, a resistor is connected to a diode symbol labeled 'Internal circuit'. From the PGND pin, a diode is connected to another diode symbol labeled 'Internal circuit'.</p> |

7.3 Input terminal

Table 7.3 Equivalent circuits for input terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|-------------|--|
| VPP |  |
| SW_DET |  |
| AC1 AC2 |  |
| SCL |  |
| XEN |  |
| VTHD FOD |  |

7.4 Output terminal

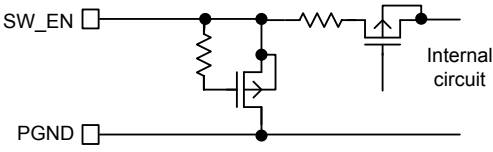
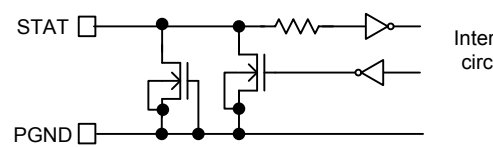
Table 7.4 Equivalent circuits for output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|----------------|--------------------|
| VDD45 | |
| VOUT | |
| COM1 COM2 | |
| CLMP1 CLMP2 | |

Table 7.5 Equivalent circuits for output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|----------|---|
| SW_EN |  <p>The diagram shows the equivalent circuit for the SW_EN pin. The SW_EN pin is connected to a resistor, which is in series with a PMOS transistor. The gate of this PMOS transistor is connected to the SW_EN pin. The source of the PMOS transistor is connected to the SW_EN pin, and the drain is connected to an internal circuit. The internal circuit is connected to a resistor, which is in series with an NPN transistor. The base of this NPN transistor is connected to the internal circuit, and the emitter is connected to the PGND pin. The collector of the NPN transistor is connected to the internal circuit. The PGND pin is connected to the source of the PMOS transistor and the emitter of the NPN transistor.</p> |
| STAT |  <p>The diagram shows the equivalent circuit for the STAT pin. The STAT pin is connected to a resistor, which is in series with a PMOS transistor. The gate of this PMOS transistor is connected to the STAT pin. The source of the PMOS transistor is connected to the STAT pin, and the drain is connected to an internal circuit. The internal circuit is connected to a resistor, which is in series with an NPN transistor. The base of this NPN transistor is connected to the internal circuit, and the emitter is connected to the PGND pin. The collector of the NPN transistor is connected to the internal circuit. The PGND pin is connected to the source of the PMOS transistor and the emitter of the NPN transistor.</p> |

8. Functions / Operation description

8.1 General outline of wireless power system

Qi compliant wireless power system consists of the first side (TX) which transmits power and the second side (RX) which receives power. Power is transmitted by adjoining coils included in the TX and RX and by sharing and combining their electromagnetic flux. The RX controls the transferred power by monitoring the received power and sending feedback signals to the TX. The TX controls the power by controlling its transmitted power according to the feedback signal which is received from the RX. A configuration example of a wireless power system is shown in Figure 8.1.

Communication signals from RX to TX are transmitted (modulated) by ASK modulation. The communication rate and its packets are defined by the Qi standard. Communication rate is 2kbps. Packets are ID, identification signal, error information, receive power, and stop signal. The TX is powered on intermittently and confirms the existence of a RX on the TX pad. When the TX recognizes a RX it succeeds to the identification phase; transmit operation starts after a compliant RX has been identified. The TX continues the transmit operation until it cannot recognize the existence of a RX or receives a transmit stop signal from the RX.

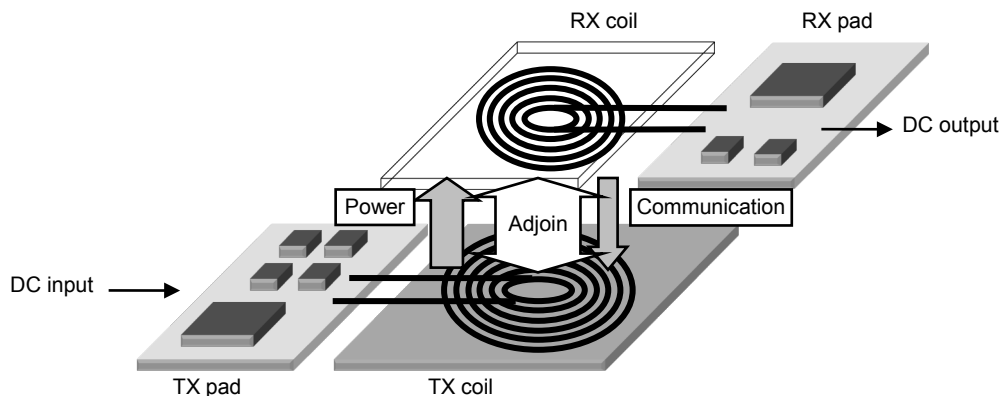


Figure 8.1 General outline of a wireless power system

8.2 General outline of wireless power RX system

The TC7763WBG includes a rectifier circuit which smoothes the RX coil current of the wireless power system; a digital control circuit; a modulation circuit which communicates between RX and TX; a regulator circuit which controls the load supply voltage; and a load switch control circuit which switches between wired and wireless supply inputs.

A wireless power system can be constructed easily without the control of a MCU because the TC7763WBG includes a digital control circuit which can operate in standalone mode. The digital control circuit corresponds to the WPC v1.1 standard and transmits the received power information to the TX after some calculations. By using the TC7763WBG as RX, the TX can take advantage of the received power information sent by the RX and a wireless power system can be constructed including FOD detection.

A configuration example of a RX system with wireless feeding and AC adapter connection input is shown in Figure 8.2. In Figure 8.2, the TC7763WBG controls wireless feeding, is capable to detect a wired AC adapter, and selects the best input power as load supply. When a connection of an AC adapter is detected, the TC7763WBG stops controlling wireless feeding and starts the load supply through the load switch. The wireless power system is controlled only when wired connection is not detected. Removing the AC adapter or USB supply will re-start the wireless power transfer if the TX allows that.

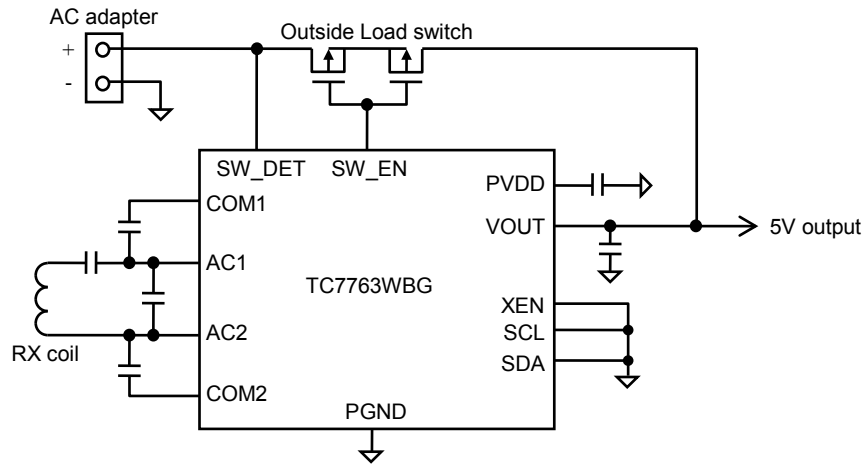


Figure 8.2 General outline of RX with the TC7763WBG

8.3 Control of TC7763WBG

8.3.1 Basic operation

The TC7763WBG incorporates a digital control circuit to realize communication with a TX. The TC7763WBG starts Qi compliant communication when it receives power from a TX.

After a certain period of time with PVDD being not less than 7V during the Power Transfer Phase, the LDO can be turned on. This is indicated by changing the STAT signal to “L”. The LDO is enabled only when STAT and XEN are “L”. Figure 8.3 shows a basic operation sequence using an externally controlled XEN signal.

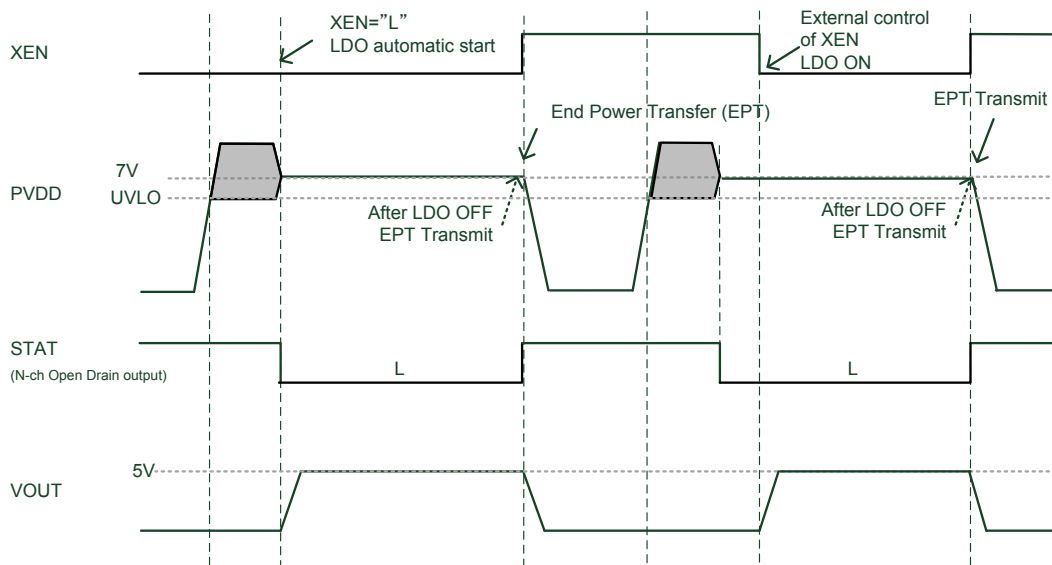


Figure 8.3 Basic operation (using XEN control)

8.4 Control state machine

The state machine of the TC7763WBG consists of SHUTDOWN mode, DISABLE mode, STARTUP mode, OUTPUT mode, and OVP mode. The wireless power system starts operation when a Qi compliant transmitters TX coil and the TC7763WBGs RX coil are adjoined. A wired power supply detected by the SW_EN input will transfers the system to the DISABLE mode.

The state transition diagram of the wireless feeding control of the TC7763WBG is shown in the Figure 8.4. The operation state of each circuit in each mode is shown in the table 8.1.

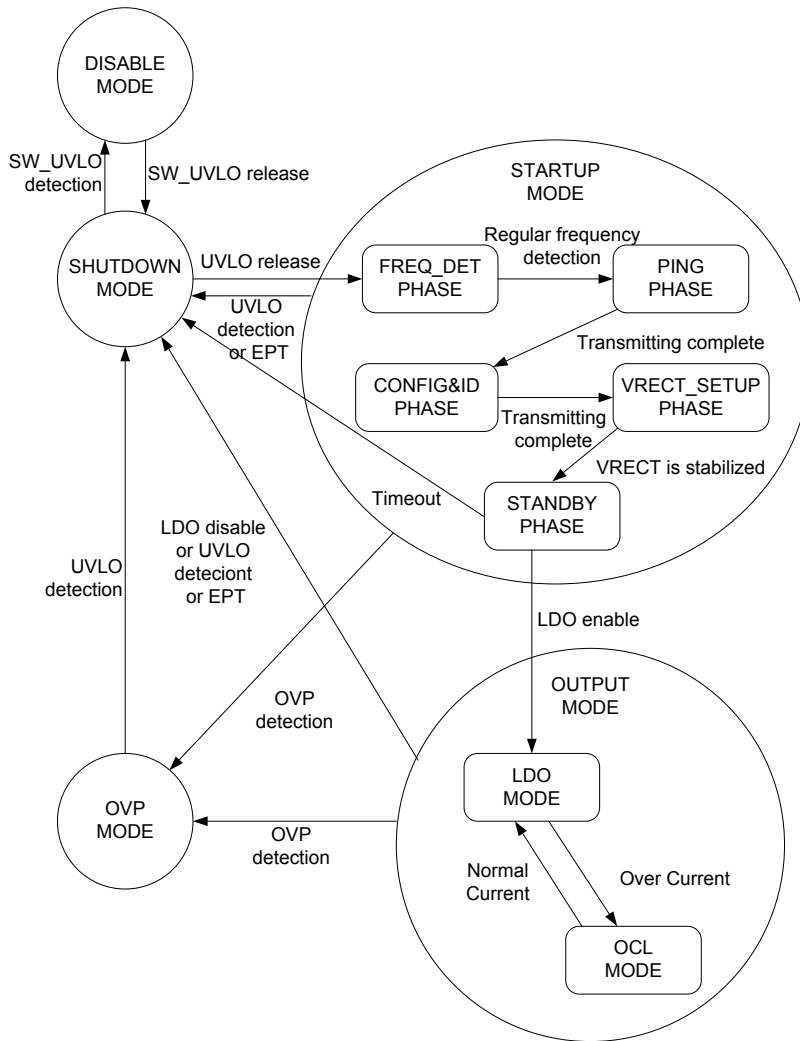


Figure 8.4 State transition diagram of TC7763WBG wireless power supply control

Table 8.1 Operating condition for each mode

| Wireless charge control mode | | Rectifier circuit | Packets (Header values) | VOUT output | UVLO | TSD | STAT output |
|------------------------------|-------------|---|----------------------------|----------------------|---------|---------|----------------|
| SHUTDOWN | | Diode bridge rectification | - | OFF | Valid | Invalid | Hi-Z |
| DISABLE | | Diode bridge rectification + RECT_CLAMP | - | OFF | Invalid | Invalid | Hi-Z |
| STARTUP | FREQ_DET | Diode rectification | NA | OFF | Valid | Valid | Hi-Z |
| | PING | Diode rectification | 01h | OFF | Valid | Valid | Hi-Z |
| | CONFIG&ID | Diode rectification | 71h, 51h | OFF | Valid | Valid | Hi-Z |
| | VRECT_SETUP | Diode rectification | 03h, 04h | OFF | Valid | Valid | Hi-Z |
| | STANDBY | Diode rectification | 03h, 04h | OFF | Valid | Valid | L |
| OUPUT | LDO | Diode rectification or synchronous rectification | 03h, 04h | 5V | Valid | Valid | L |
| | OCL | Diode rectification or synchronous rectification | 03h, 04h | Depending on load | Valid | Valid | L |
| OVP | | Diode bridge rectifier + RECT_CLAMP | 03h, 04h | OFF | Valid | Valid | Hi-Z |

8.4.1 SHUTDOWN mode

SHUTDOWN mode is the status without detection of wired or wireless power supply. The detection judgment whether wireless power supply is on or not is done by internal monitoring of the PVDD terminal voltage (VRECT; the voltage generated by rectifying the RF wireless power).

When the VRECT is below the UVLO release voltage, TC7763WBG enters SHUTDOWN mode.

In SHUTDOWN mode, the rectifier circuit work as a diode bridge rectifier. Then all MOSFETs are off and the diode bridge rectifies through the MOSFET body diodes. The digital control circuit, communication circuit and regulator circuits are stopped.

When the UVLO is released, TC7763WBG starts to operate the wireless power supply control and goes to STARTUP mode.

8.4.2 DISABLE mode

DISABLE mode is the status when TC7763WBG detects a wired power supply. The wireless power supply is stopped. When the TC7763WBG detects a wired connection, the RECT_CLAMP function becomes available to prevent accidentally providing wireless power.

8.4.3 STARTUP mode

STARTUP mode is the status when the TC7763WBG detects wireless power, in which it certificates with TX and stabilizes VRECT. The status has 5 phases which automatically transit in the following sequence: FREQ_DET phase, PING phase, CONFIG&ID phase, VRECT_SETUP phase and STANDBY phase.

In the STARTUP mode the rectifier circuit works as diode rectifier in which the low-side MOSFETs are fixed to off and only the high-side MOSFETs work.

After the LDO is enabled, the system shifts to the OUTPUT mode.

(1) FREQ_DET phase

In the FREQ_DET phase, TC7763WBG determines if the TX is compliant to the Qi standard. After UVLO is released, TC7763WBG starts detection of the frequency on AC1 and AC2. When the range of the frequency is from 85 kHz to 286 kHz, TC7763WBG considers that the frequency is stable.

After confirming both the proper frequency and frequency stability, TC7763WBG shifts to the PING phase.

(2) PING phase

In the PING phase, TC7763WBG notifies detection of wireless power supply to the TX. After 28 ms have elapsed in this phase, TC7763WBG measures VRECT to determine its received power and sends a packet including header (01h) and the result of the received power calculation.

After that the TC7763WBG automatically shifts to the CONFIG&ID phase.

(3) CONFIG&ID phase

In the CONFIG&ID phase, TC7763WBG sends RX information to the TX. After 7.5 ms have elapsed in this phase, TC7763WBG sends a packet including header (71h), WPC version, maker code and serial code. Subsequently, after 7.5 ms, it sends a packet including header (51h), received power and timing code measured by the TC7763WBG.

Then TC7763WBG automatically shifts to VRECT_SETUP phase.

(4) VRECT_SETUP phase

In the VRECT_SETUP phase, VRECT is converged to its target value. After 7.5 ms have elapsed in this phase, TC7763WBG calculates an error value. After 1 ms TC7763WBG sends a packet including header (03h) and Control Error Packet (CEP) including the error value. Subsequently, after 40.5 ms, the TC7763WBG calculates the received power and sends a packet including header (04h) and received power.

In this mode the sending cycle of the error code is 62 ms. The sending cycle of the received power is once per 29 sending cycles of the CEP.

If the VRECT is over 7V and after CEP are sent twice, TC7763WBG switches STAT to L and moves to the STANDBY phase.

(5) STANDBY phase

STANDBY phase is the status until the LDO works. When the LDO is stable, the TC7763WBG shifts to the OUTPUT mode.

It is possible to select LDO start-up from the following settings; XEN terminal or automatic startup by eFuse setting. If the LDO doesn't work within 190 ms, TC7763WBG shifts to the SHUTDOWN mode.

8.4.4 OUTPUT mode

In the OUTPUT mode, TC7763WBG provides power received from a wireless power supply to the load. The OUTPUT mode has 2 sub-modes: the LDO mode that provides 5V and the OCL mode that works with a 2 step constant current limit.

If the output current exceeds 250 mA, the rectifier circuit shifts to synchronous rectifier mode. If the output current is below 220 mA, the rectifier circuit shifts to diode rectifier mode.

In this mode the sending cycle of the CEP is 192.5 ms. The sending cycle of the received power is one time per 8 sending cycles of the CEP.

(1) LDO mode

In the LDO mode, VRECT – generated by a wireless power supply – passes through the built-in LDO and gives out a 5V constant voltage. The maximum current is set to 1.0A and OCL (over current limit) current (IOCL) is set to 1.3A.

(2) OCL mode

OCL mode is the status when the output current is limited by the 2 step OCL function. The 2 step OCL is a function in which the TC7763WBG switches IOCL according to VOUT. When VOUT exceeds 2.8V, IOCL is set to 1.3A. When VOUT is below 2.5V, IOCL is set to 0.35A. If VOUT is over 2.8V with IOCL = 0.35 A, IOCL is reconfigured to 1.3A. Figure 8.5 shows the V-I characteristics.

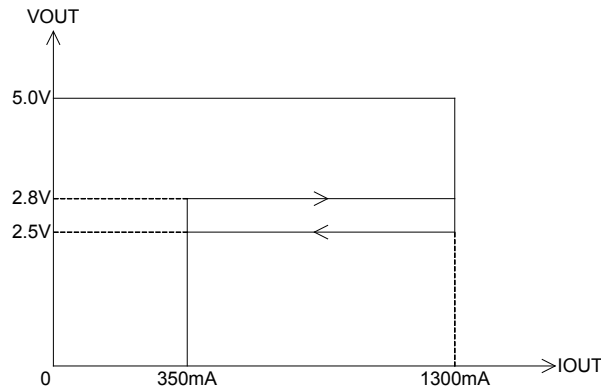


Figure 8.5 OCL function and V-I characteristic of LDO

8.4.5 VRECT automatic switching function

The VRECT automatic switching function sets the voltage of VRECT automatically according to the output current. TC7763WBG divides the status of its output current as shown below in Table 8.2. It is possible to reduce IC internal losses by reducing the difference between input and output voltages at heavy load and reducing output voltage variations by controlling VRECT at load changes.

Table 8.2 IOUT – VRECT setting voltages

| Output current | VRECT setting voltage |
|------------------------------------|-----------------------|
| less than 100mA | 7.05 to 7.21V |
| More than 100mA less than 200mA | 6.25 to 6.41V |
| More than 200mA less than 400mA | 5.5 to 5.66V |
| More than 400mA | 5.1 to 5.25V |

8.4.6 OVP mode

This function is to avoid overvoltage of VRECT by the over voltage detection function of VRECT and the RECT_CLAMP function. If VRECT exceeds 15 V, TC7763WBG judges it as an over voltage. In such a case the TC7763WBG connects AC1 and AC2 to GND through external capacitors by switching CLMP1 and CLMP2 from Hi-Z to GND. The RX coil current flows through the capacitors, so that TC7763WBG can reduce VRECT. WPT_OVP function has a latching function that is reset through a UVLO condition.

8.4.7 Operation stop

Two methods can be used to stop the wireless power supply operation: EPT (End Power Transfer) messages and the communication timeout. When TC7763WBG activates any of its protection functions (OVP, output OFF, and timeout), it transmits an EPT message to the TX. The TX then stops its power transmission. The communication timeout means that the TX does not receive any packet which TC7763WBG transmitted for a fixed period. Then the TX stops power transmission automatically.

9. Descriptions of functional details

9.1 Communication function of the wireless power system

In the STARTUP mode, when the UVLO is released and the frequency of rectifier is the range of 85 kHz to 286kHz, the input is judged normal and communication (PING Phase) of the wireless power system automatically starts.

9.1.1 ASK modulation

Capacitors are connected between COM1 and AC1 and between COM2 and AC2. TC7763WBG communicate with TX by ASK modulation. The coil current is overlapped with the signals that TC7763 controls capacity load.

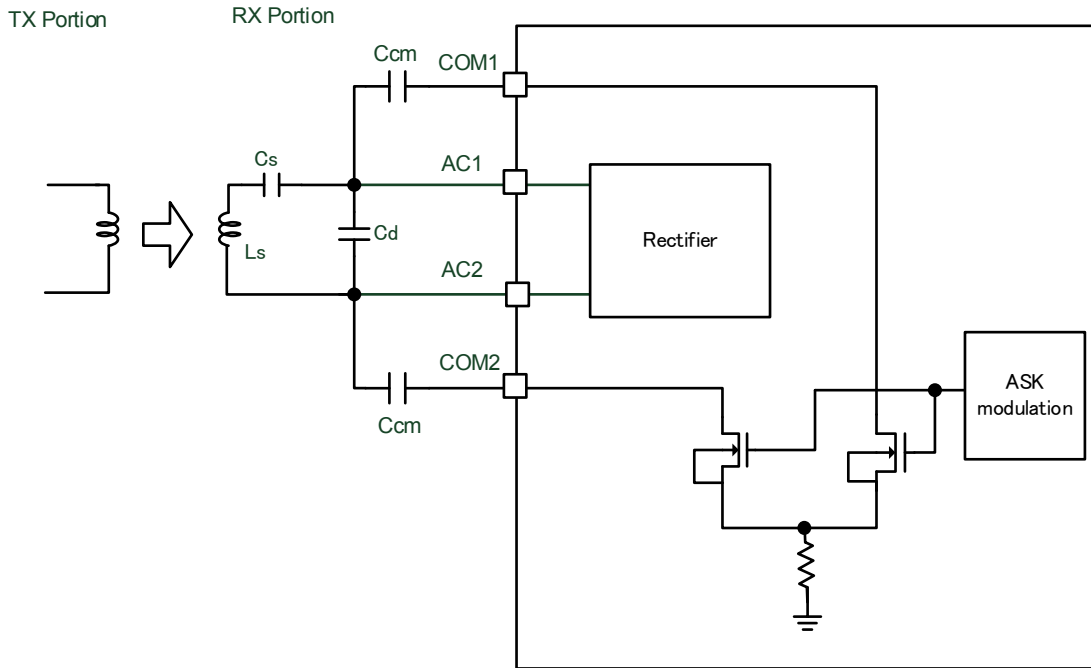


Figure 9.1 Connection diagram of ASK modulation

9.1.2 Communication protocol

(1) Bit Encoding Scheme

Bit chart of WPC communication is as follows.

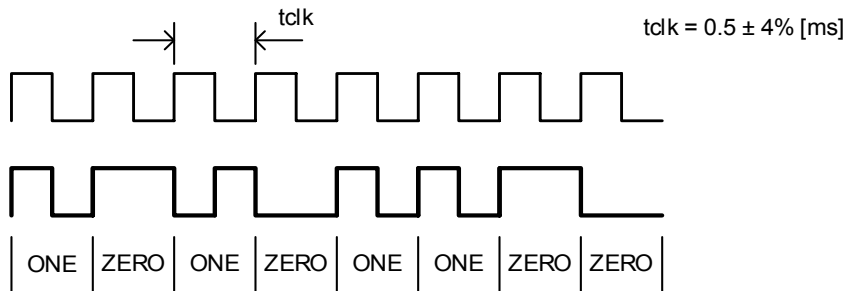


Figure 9.2 Example of the differential bi-phase encoding (WPC volume 1:Low power, part 1 Interface Definition)

(2) Byte Encoding Scheme

Byte chart of WPC communication is as follows. Start bit: "ZERO", Stop bit: "ONE".
The order of the data bits is lsb first.

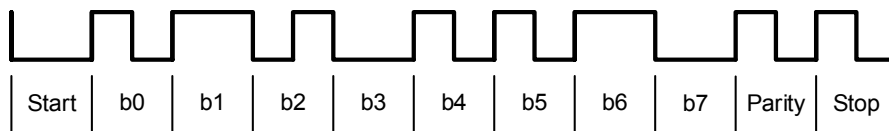


Figure 9.3 Example of the asynchronous serial format (WPC volume 1:Low power, part 1 Interface Definition)

(3) Packet Structure

Packets of WPC communication consist of four parts; Preamble, Header, Message, and Checksum.

Preamble: 11bit (default) of ONE continuously.

Header: Indicates the kind of packet and specifies the size of the message that will be sent next.

Message: Data of each packet type.

Checksum: XOR value of Header and Message.

$$\text{Checksum} = \text{Header} + \text{Message}(0) + \text{Message}(1) + \dots + \text{Message}(\text{last})$$

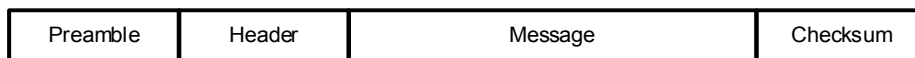


Figure 9.4 Packet format (WPC volume 1:Low power, part 1 Interface Definition)

9.1.3 Communication packets

The TC7763WBG transmits packets according to the following definitions.

- PING Phase

(1) Signal Strength Packet (01h)

Table 9.1 Strength Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------------------|--------|----|-----------------------|----|----|----|----|----|----|----|
| Signal Strength Packet | 01h | B0 | Signal Strength Value | | | | | | | |

Signal Strength Value:

It indicates the strength of the coupling between primary side and secondary side, which is calculated by monitoring VRECT.

- CONFIG & ID Phase

(2) Identification Packet (71h)

Table 9.2 Identification Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|-----------------------|--------|----|---------------|-------------------------|----|----|---------------|----|----|-------|--|
| Identification Packet | 71h | B0 | Major Version | | | | Minor Version | | | | |
| | | B1 | (msb) | Manufacturer Code | | | | | | (lsb) | |
| | | B2 | | | | | | | | | |
| | | B3 | EXT | (msb) | | | | | | | |
| | | B4 | | Basic Device Identifier | | | | | | | |
| | | B5 | | | | | | | | | |
| | | B6 | | | | | | | | (lsb) | |

Major Version : Fixed to "01h"

Minor Version : Fixed to "01h"

Manufacturer Code : Indicates manufacture code. The code of Toshiba is "0033h".

EXT : Fixed to "EXT="0"

Basic Device Identification

: Indicates the individual device ID.

(3) **Configuration Packet (51h)**

Table 9.3 Configuration Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|----------------------|--------|----|-------------|----------|---------------|----|---------------|-------|----|----|--|
| Configuration Packet | 51h | B0 | Power Class | | Maximum Power | | | | | | |
| | | B1 | Reserved | | | | | | | | |
| | | B2 | Prop | Reserved | | | | Count | | | |
| | | B3 | Window Size | | | | Window Offset | | | | |
| | | B4 | Reserved | | | | | | | | |

Power Class : "00h"
 Maximum Power : "0Ah" (5W)
 Prop : "00h"
 Count : "00h"
 Window Side : "04h"
 Window Offset : "01h"

- VRECT_SETUP Phase / STANDBY Phase

(4) **Control Error Packet (03h)**

Table 9.4 Control Error Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----------------------|--------|----|---------------------|----|----|----|----|----|----|----|
| Control Error Packet | 03h | B0 | Control Error Value | | | | | | | |

(5) **Received Power Packet (04h)**

Table 9.5 Received Power Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-----------------------|--------|----|----------------------|----|----|----|----|----|----|----|
| Received Power Packet | 04h | B0 | Received Power Value | | | | | | | |

Received Power Value: Indicates received power including FOD compensation.

(6) End power transfer packet (02h)

Table 9.6 End Power Transfer Packet

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------------------|--------|----|--------------------------|----|----|----|----|----|----|----|
| End Power Transfer Packet | 02h | B0 | End Power Transfer Value | | | | | | | |

End Power Transfer Value: Signal of End Power Transfer is transmitted according to Table 9.7.

Table 9.7 End Power Transfer Value

| Reason | Value | Condition |
|------------------|-------|--|
| Unknown | 00h | Low voltage of VOUT (VOUT<4.4V) |
| Charge Complete | 01h | When LDO turns off due to XEN="H" or EN_LDO="0" At time out when LDO doesn't work in STANDBY phase. |
| Internal Fault | 02h | Unused |
| Over Temperature | 03h | Internal and external over temperature detection |
| Over Voltage | 04h | Unused (Note 1) |
| Over Current | 05h | At the detection of over current limitation |
| Battery Failure | 06h | At the detection of VOUT overvoltage (VOUT>5.6V) |
| Reconfigure | 07h | Unused |
| No Response | 08h | When VRECT deviates from the setting voltage range at constant time |

Note 1: TC7763WBG does not transmit OVP because it has RECT_CLAMP function.

9.2 Rectifier circuit

9.2.1 Rectifier modes

The rectifier circuit has 3 modes: synchronous rectification, diode rectification, and diode bridge mode. TC7763WBG automatically switches the modes.

In SHUTDOWN mode, the rectifier operates in the diode bridge mode. In this mode, all MOSFETs are fixed to OFF and the rectifier operates over the MOSFETs body diode.

In STARTUP mode, the rectifier operates in the diode rectifier mode. In this mode, the low side MOSFETs are fixed to OFF. The rectifier operates by turning on and off only the high side MOSFETs.

In OUTPUT mode, when the output current exceeds 250mA, the rectifier circuit operates in the synchronous rectification mode by turning on and off all MOSFETs. In the synchronous rectification mode, when the output current decreases to 220mA or less, the rectifier circuit switches to the diode rectifier mode.

Table 9.8 Rectifier modes

| The condition of VRECT voltage | Light load mode (Output current is below 220mA.(Note)) | Normal mode (Output current is over 250mA.(Note)) |
|--------------------------------|---|--|
| $V_{RECT} < UVLO$ | Diode bridge mode | - |
| $V_{RECT} \geq UVLO$ | Diode rectification mode | Synchronous rectification mode |

Note: 30mV hysteresis

9.2.2 RECT_CLAMP function

The RECT_CLAMP function suppresses over voltages of VRECT. The clamping functions circuitry can be seen in Figure 9.5. Excessive coil current potentially generating an over voltage at the internal rectifier output will be shunted to GND through a capacitive load connected to the IC's CLMP terminals and the IC internal MOSFETs. This suppresses the excessive rise of VRECT.

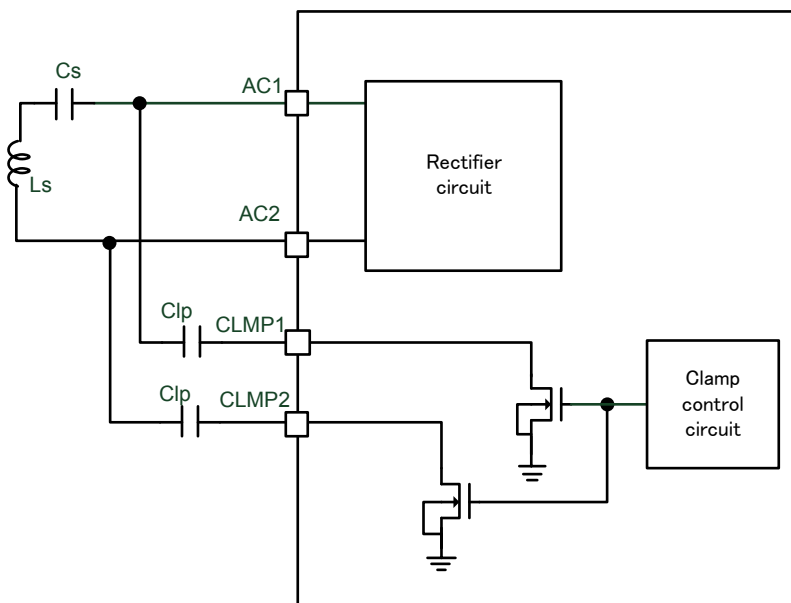


Figure 9.5 Connection diagram of clamp circuit

9.3 FOD function

The FOD function is used to calculate losses of received power in the mobile device. TC7763WBG can revise the actual received power, measured by the rectifier current, with an external resistor on the FOD terminal.

9.4 Thermal detection function

External temperature is monitored by connecting a NTC thermistor to the VTHD terminal. Recommended thermistor is equivalent to the SEMITEC503FT.

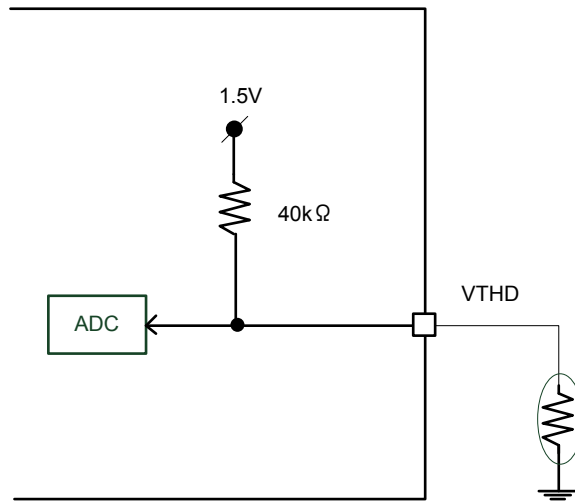


Figure 9.6 Connection diagram of thermal detection circuit

9.5 External Load switch control circuit

An external load switch control circuit monitors the voltage of the SW_DET terminal and selects the wireless power output or the USB input (or AC adopter) by controlling an external load switch. When a secondary input power is connected to the SW_DET terminal, below control is performed by the TC7763WBG.

Table 9.9 External Load switch control

| Conditions of SW_DET | External Load Switch | Voltage of SW_EN | Clamp circuit | LDO and rectifier circuit | WPC operation |
|----------------------|----------------------|---------------------------------------|---------------|---------------------------|---------------|
| SW_DET<4V | OFF | The higher voltage of SW_DET or VOUT. | OFF | ON | Available |
| 5.75V≥SW_DET≥4V | ON | 0V | ON | OFF | Stop |
| SW_DET>5.75V | OFF | SW_DET, voltage | ON | OFF | Stop |

9.6 Protection functions

9.6.1 Under voltage lockout (UVLO) function

Under voltage lockout (UVLO) function avoids errors caused by too low VRECT voltages. UVLO detection condition is that the voltage of VRECT falls below 3.7V (typ.). UVLO function is released when the voltage of VRECT exceeds 4.0V (typ.). The UVLO function stops the LDO output and sets the STAT terminal outputs into Hi-Z state.

9.6.2 Over voltage detection (WPT_OVP) function

Over voltage detection (WPT_OVP) function avoids errors caused by too high VRECT voltages. Detection condition of WPT_OVP function is that the voltage of PVDD exceeds 15V (typ.). The WPT_OVP function turns the output of the LDO off and activates the clamp circuit of the rectifier. When WPT_OVP is detected, the voltage of the PVDD terminal falls and wireless power operation stops because the output of internal detection signal is latched. WPT communication also stops. No message can be sent to the TX since the wireless power reception needs to be stopped as fast as possible to avoid damages of the receiver system. The TX will stop power transmission due to the missing control error packets.

9.6.3 Over current detection (OCL) function

Over current detection (OCL) function avoids excessive output current of the LDO. The detection condition of OCL function is that the current exceeds the output current determined by the voltage of VOUT (refer to the Figure 8.5). In case the OCL detection time exceeds 4ms (typ.), power transmission is stopped by transmitting an EPT message to the TX (05h: Over Current). The OCL detection current is 1.3A (typ.).

9.6.4 Thermal shutdown (TSD) function

Thermal shutdown (TSD) function avoids the IC destruction caused by rising chip internal temperature. The detection condition of TSD function is that the internal temperature exceeds 150°C (typ.). When TSD is detected, the output of LDO is turned off. In case the internal temperature falls below 130°C (typ.), TSD function is released automatically and LDO is turned on again. In case the TSD status continues for 200ms or more, the output of the LDO turns off and power transmission is finished by transmitting an EPT message to the TX (03h: Over Temperature).

9.6.5 External over temperature protection (OTP) function

External over temperature protection (OTP) function avoids the IC destruction, which is caused by rising temperature, by monitoring the voltage over the external thermistor. The detection condition of OTP function is that the voltage over the external thermistor exceeds the voltage configured in the SET_OVTEXT register. In case the OTP condition exceeds 1ms or more, the LDO output turns off and power transmission is finished by transmitting an EPT message to the TX (03h: Over Temperature)

9.6.6 Select control of external power (SW_UVLO/SW_OVLO) function

SW_UVLO/SW_OVLO function selects the wireless power output and the external power input with the external load switch by monitoring the voltage of SW_DET terminal.

When the voltage of the SW_DET terminal is less than 4.0V (typ.), SW_UVLO function turns off the external load switch and selects the wireless power output. When the voltage of the SW_DET terminal rises to the voltage of SW_UVLO detection voltage or exceeds it, the wireless power output is turned off by selecting the external power input by turning on the external load switch.

SW_OVLO function turns off the external load switch when the voltage of SW_DET terminal is exceeds 5.75V (typ.). It does not switch to the wireless power even if it is available.

9.6.7 Abnormality detection for LDO output function

Abnormality detection for LDO output function detects abnormal operation by monitoring the output voltage of VOUT. Abnormality detection of LDO output function detects abnormal operation by monitoring the output voltage VOUT. When VOUT falls below 4.4V (typ.) for 3.5s or more, the LDO output turns off and power transmission is finished by transmitting an EPT message to the TX (00h: Unknown).

When VOUT exceeds 5.6V (typ.) for 64ms or more, the LDO output turns off and power transmission is finished by transmitting an EPT message to the TX (06h: Battery Failure).

10. Absolute Maximum Ratings (Ta= 25°C)

Table 10.1 Absolute Maximum Ratings

| Characteristics | Symbol | Rating | Unit | Remarks |
|-----------------------|----------------------|-------------|------|----------|
| Supply voltage | VRECT _{MAX} | -0.3 to 18 | V | (Note 1) |
| Input voltage (1) | V _{I1} | -0.3 to 18 | V | (Note 2) |
| Input voltage (2) | V _{I2} | -0.3 to 30 | V | (Note 3) |
| Input voltage (3) | V _{I3} | -0.3 to 8 | V | (Note 4) |
| Input voltage (4) | V _{I4} | -0.3 to 5.6 | V | (Note 5) |
| Operating temperature | T _{opr} | -40 to 85 | °C | |
| Junction temperature | T _j | 150 | °C | |
| Storage temperature | T _{stg} | -55 to 150 | °C | |

Note The absolute maximum ratings of a semiconductor devices are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device to break down, damage, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

In addition, please assume it "PGND=0V".

Note 1: Applies to PVDD terminal only

Note 2: Applies to AC1, AC2, COM1, COM2, CLMP1 and CLMP2 terminals

Note 3: Applies to SW_EN and SW_DET terminals

Note 4: Applies to VPP terminal

Note 5: Applies to terminal except above terminals

11. Electrical Characteristics

11.1 DC characteristics Common Circuit, Digital Controller

Table 11.1 DC characteristics Common Circuit, Digital Controller

(Unless otherwise specified, VRECT = 7V, PGND = 0V, SW_DET = 0V, Ta = 25°C)

| Characteristics | | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|---------------------------|------------|-----------------------|--|------|------|------|------|----------|
| Operation voltage | | V _{OP} | | 2.5 | - | 15 | V | PVDD |
| UVLO detection voltage | | V _{UVLO_ON} | VRECT = 7V to 0V | 3.6 | - | 3.8 | V | PVDD |
| UVLO release voltage | | V _{UVLO_OFF} | VRECT = 0V to 7V | - | - | 4.2 | V | PVDD |
| Quiescent current | | I _{CC} | VRECT = 7V AC1 = AC2 = Open 5V LDO off | - | 2.5 | 6.0 | mA | PVDD |
| Input voltage(1) | High level | V _{IH1} | | 1.4 | - | - | V | XEN |
| | Low level | V _{IL1} | | - | - | 0.4 | | |
| Input current(1) | High level | I _{IH1} | V _{IH1} = V _{OUT45} | 20 | - | 75 | μA | XEN |
| | Low level | I _{IL1} | V _{IL1} = GND | -0.6 | - | 0.6 | | |
| Output voltage | Low level | V _{OL1} | I _{OUT} = -1mA | 0 | - | 0.4 | V | STAT |
| VDD45 voltage | | VDD45 | | 4.25 | - | 4.75 | V | VDD45 |
| Oscillator frequency | | f _{CLK} | | 3.84 | 4.0 | 4.16 | MHz | |
| TSD detection temperature | | T _{TSD_ON} | | 135 | 150 | 165 | °C | |
| TSD release temperature | | T _{TSD_OFF} | | 120 | - | - | °C | |

11.2 DC Characteristics Rectifier, Modulator

Table 11.2 DC Characteristics Rectifier, Modulator

(Unless otherwise specified, VRECT = 7.0V, PGND=0V, SW_DET = 0V, Ta = 25°C)

| Characteristics | | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|--------------------------------|-----------|----------------------|---|-----|------|-----|------|--------------|
| Rectifier MOSFET on-resistance | High-side | R _{ONH_AC} | I _{DS} = -100mA | - | 45 | - | mΩ | AC1, AC2 |
| | Low-side | R _{ONL_AC} | I _{DS} = 100mA | - | 30 | - | | |
| Clamper MOSFET on-resistance | | R _{ON_CLMP} | I _{DS} = 100mA | - | - | 1.5 | Ω | CLMP1, CLMP2 |
| Modulator output resistance 1 | | R _{COM1} | COM2 open Resistance between COM1 and PGND | 45 | - | 65 | Ω | COM1 |
| Modulator output resistance 2 | | R _{COM2} | COM1 open Resistance between COM2 and PGND | 45 | - | 65 | Ω | COM2 |

11.3 DC Characteristics 5V LDO

Table 11.3 DC Characteristics 5V LDO

(Unless otherwise specified, VRECT = 7.0V, PGND = 0V, SW_DET = 0V, Ta = 25°C)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|--------------------------------------|---------------------|-------------------------------------|------|------|------|------|------------------|
| 5V LDO output voltage accuracy | AccV _{OUT} | LDO MODE I _{OUT} = 10mA | -2 | - | 2 | % | V _{OUT} |
| 5V LDO OCL current 1 | I _{OCL1} | V _{OUT} = 5V | 1.1 | 1.3 | 1.5 | A | V _{OUT} |
| 5V LDO OCL current 2 | I _{OCL2} | V _{OUT} = 0V | 0.25 | 0.35 | 0.45 | A | V _{OUT} |
| OCL current change voltage threshold | V _{OCL} | V _{OUT} falling | - | - | 2.4 | V | V _{OUT} |
| Discharge resistance | R _{DCHG} | | 6 | 9 | 12 | kΩ | V _{OUT} |

11.4 DC Characteristics External Load Switch Driver

Table 11.4 DC Characteristics External Load Switch Driver

(Unless otherwise specified, SW_DET = 5V, PGND = 0V, Ta = 25°C)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal | |
|---|------------------------|-----------------------|---|------|-----|------|------------------|-------|
| SW_DET leakage current | I _{DET} | V _{OUT} = 0V | 250 | - | 500 | μA | SW_DET | |
| SW_UVLO detection voltage | V _{SUVLO_ON} | SW_DET = 5V to 0V | 3.8 | - | - | V | SW_DET | |
| SW_UVLO release voltage | V _{SUVLO_OFF} | SW_DET = 0V to 5V | - | - | 4.4 | V | SW_DET | |
| SW_OVP detection voltage | V _{SOVP_ON} | SW_DET = 5V to 6V | - | - | 5.9 | V | SW_DET | |
| SW_OVP release voltage | V _{SOVP_OFF} | SW_DET = 6V to 5V | 5.55 | - | - | V | SW_DET | |
| SW_EN sink current 1 | I _{SWEN1} | SW_DET = 5V | - | - | 6.5 | μA | SW_EN | |
| SW_EN output voltage | High level 1 | V _{OH_SWEN1} | SW_DET = 10V, V _{OUT} = 0V I _{OUT} = 0.1mA | 9.5 | - | 10 | V | SW_EN |
| | High level 2 | V _{OH_SWEN2} | SW_DET = 0V, V _{OUT} = 5V I _{OUT} = 0.1mA | 4.5 | - | 5 | V | |
| | Low level | V _{OL_SWEN} | SW_DET = 5V, I _{OUT} = -1mA | - | - | 0.4 | V | |
| V _{OUT} terminal leakage current | I _{LEAK_VOUT} | | - | - | 200 | μA | V _{OUT} | |

12. Application Circuit

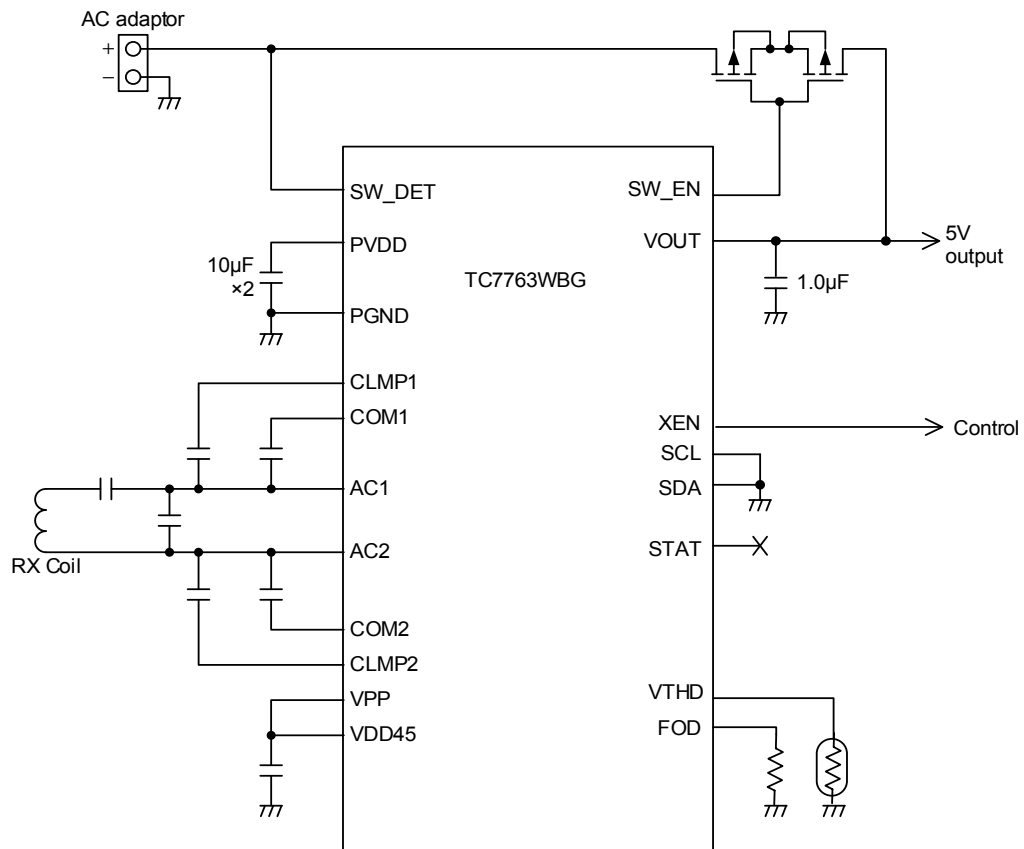
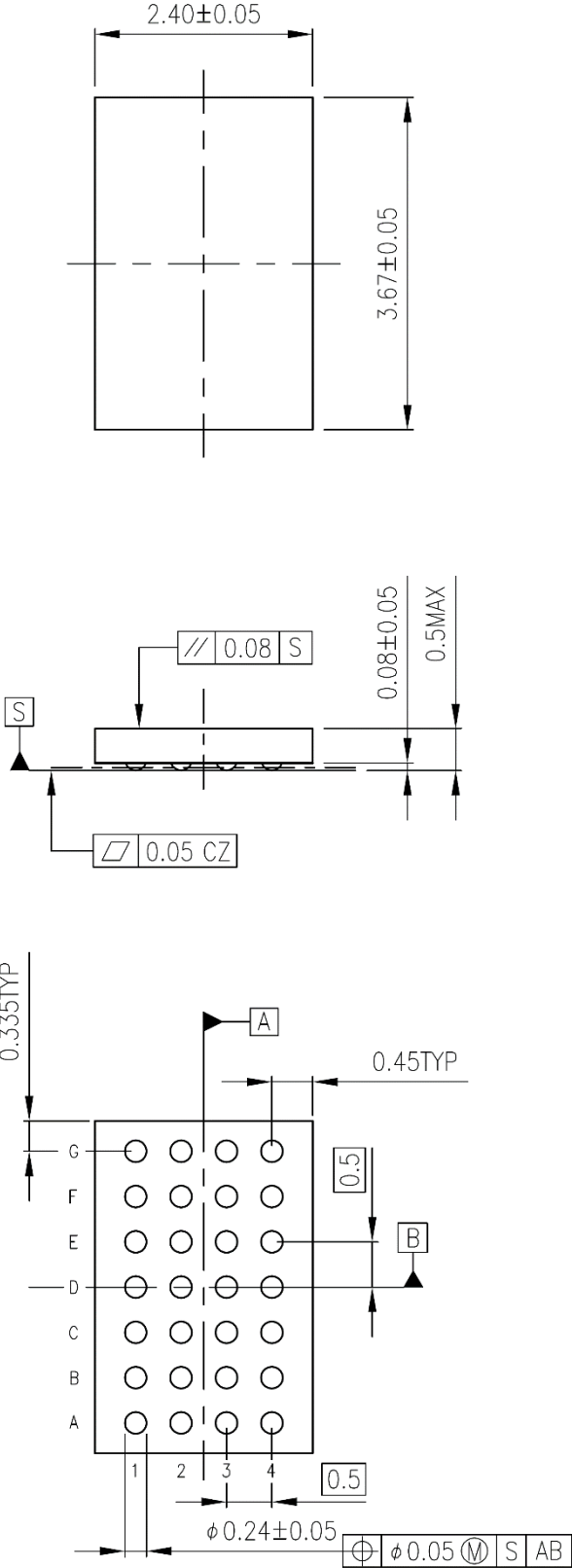


Figure 12.1 Application circuit

13. Package dimensions

S-XFLGA28-0304-0.50-001



Note 1: Unit: mm

Weight: 10mg (typ.)

14. RESTRICTIONS ON PRODUCT USE

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