TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MET573AFK

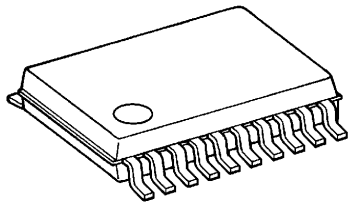
Octal D-type latch with 3-state output

The TC7MET573A is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
The input voltage are compatible with TTL output voltage.
This device may be used as a level converter for interfacing 3.3V to 5V system.
Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

*1: output in off-state

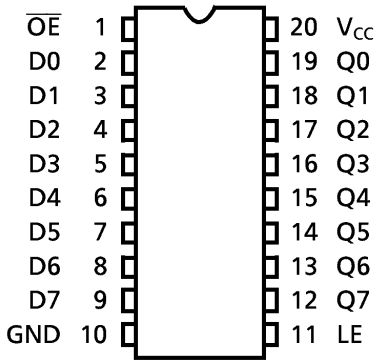
FEATURES:

- High Speed ····· t_{pd} = 7.7ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(max) at Ta = 25°C
- Compatible with TTL outputs ···· V_{IL} = 0.8V (max)
  V_{IH} = 2.0V (min)
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Low Noise ····· V_{OLP} = 1.6V (max)
- Pin and Function Compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 573 type.



VSSOP20-P-0030-0.50
Weight : 0.03g (typ.)

Pin Assignment



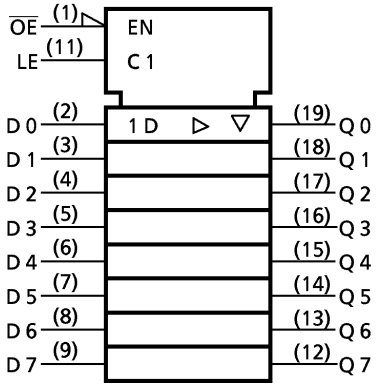
(TOP VIEW)

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC Logic Symbol



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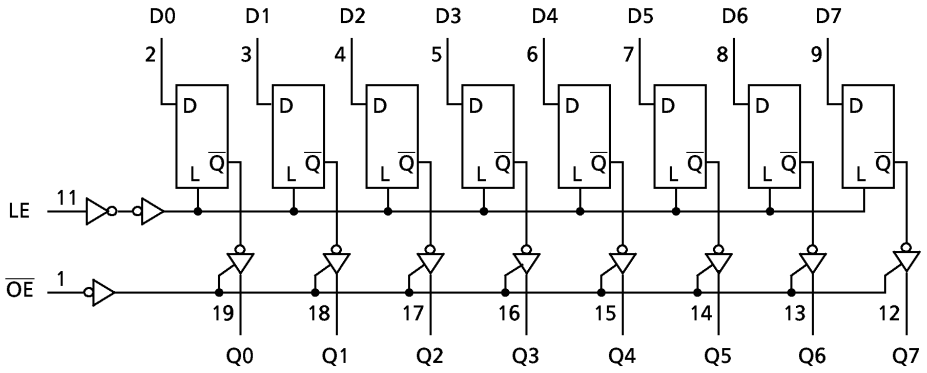
System Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~VCC + 0.5 (Note 2)	
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20 (Note 3)	mA
DC Output Current	I_{OUT}	±25	mA
DC Vcc/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

(Note 1): Output in Off-State
(Note 2): High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3): $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 4)	V
		0~VCC (Note 5)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~20	ns / V

(Note 4): Output in Off-State
(Note 5): High or Low State

DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITON		V_{CC} (V)	Ta = 25°C Min	Typ.	Max	Ta = −40~85°C Min	Max	UNIT
High - Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.40	4.50	—	4.40	—	V
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	
	I_{CCT}	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I_{OPD}	V_{OUT} = 5.5V		0	—	—	0.5	—	5.0	μA

Timing Requirements (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C Typ .	Limit	Ta = −40~85°C Limit	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		5.0 ± 0.5	—	6.5	8.5	ns
Minimum Set - up Time	t_s		5.0 ± 0.5	—	1.5	1.5	
Minimum Hold Time	t_h		5.0 ± 0.5	—	3.5	3.5	

AC Electrical Characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time (LE-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	−	7.7	12.3	1.0	13.5	ns
				50	−	8.5	13.3	1.0	14.5	
Propagation Delay Time (D-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	−	5.1	8.5	1.0	9.5	
				50	−	5.9	9.5	1.0	10.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	RL = 1kΩ	5.0 ± 0.5	15	−	6.3	10.9	1.0	12.5	
				50	−	7.1	11.9	1.0	13.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	RL = 1kΩ	5.0 ± 0.5	50	−	8.8	11.2	1.0	12.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 6)	5.0 ± 0.5	50	−	−	1.0	−	1.0	
Input Capacitance	C_{IN}				−	4	10	−	10	pF
Output Capacitance	C_{OUT}				−	6	−	−	−	
Power Dissipation Capacitance	C_{PD}	(Note 7)			−	25	−	−	−	

(Note 6): Parameter guaranteed by design. $t_{osLH} = |t_{pLH\,m} - t_{pLHn}|$, $t_{osHL} = |t_{pHL\,m} - t_{pHLn}|$

(Note 7): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per latch)}$$

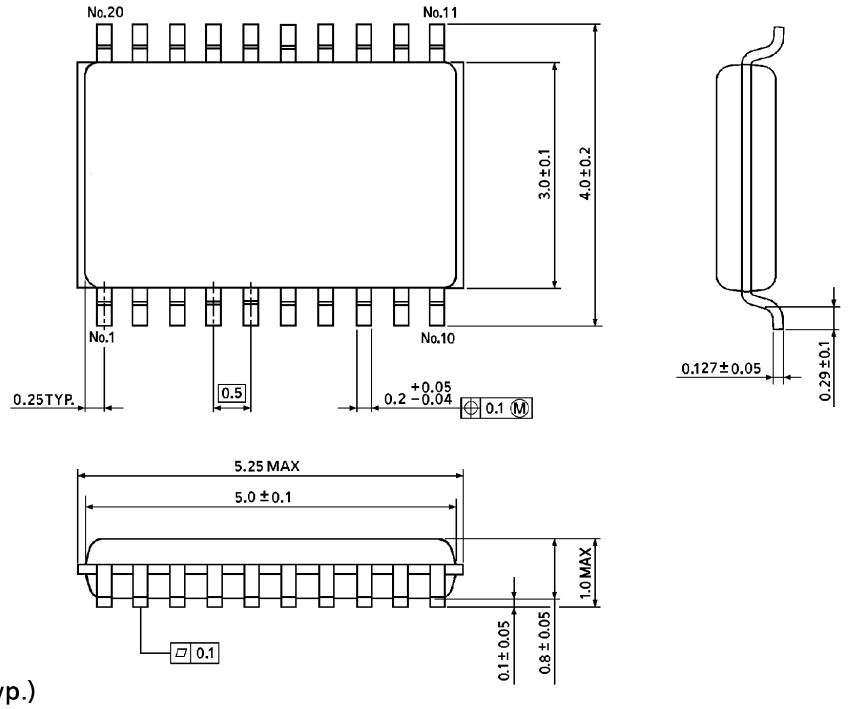
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}\,(\text{total}) = 14 + 11 \cdot n$$

Noise Characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	Typ.	Limit	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	1.1	1.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	− 1.1	− 1.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	−	0.8	V

PACKAGE DIMENSIONS (VSSOP20-P-0030-0.50) Unit in mm



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