

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7MH165FK

## 8 - Bit Shift Register (P - In, S - Out)

The TC7MH165 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.

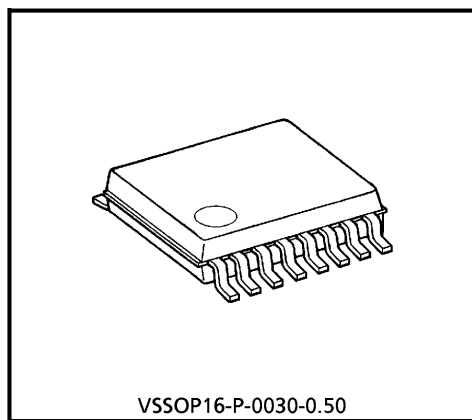
When the SHIFT/LOAD input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

An Input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**Features:**

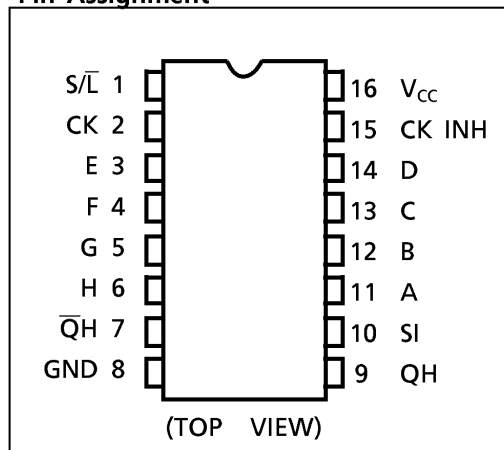
- High Speed ..... $f_{MAX} = 150\text{MHz}(\text{typ.})$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation .....  $I_{CC} = 4\mu\text{A}(\text{max})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{min})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74ALS165



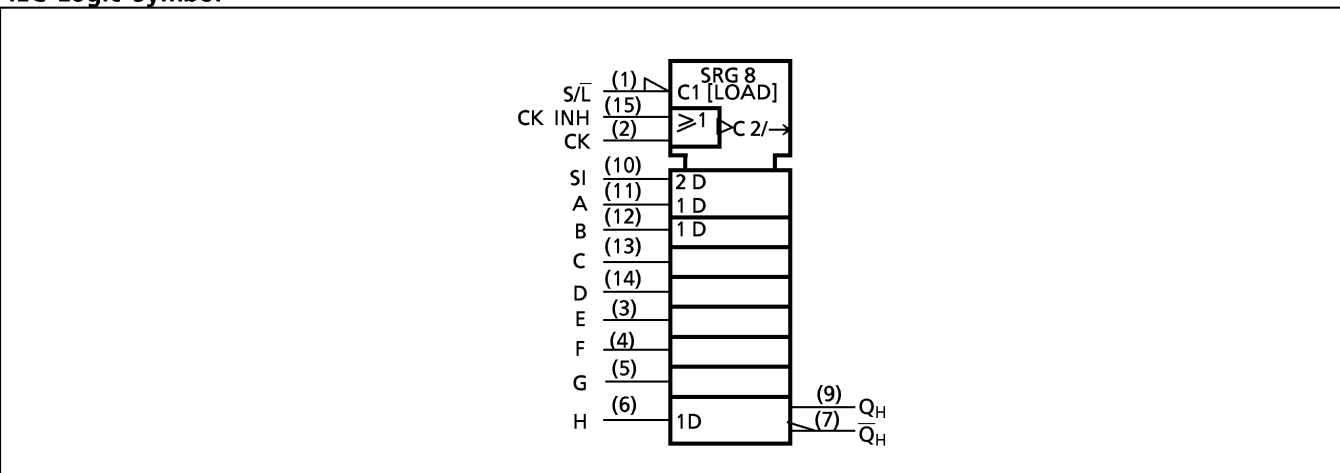
VSSOP16-P-0030-0.50

Weight: 0.02g (Typ.)

**Pin Assignment**



**IEC Logic Symbol**



980910EBA2

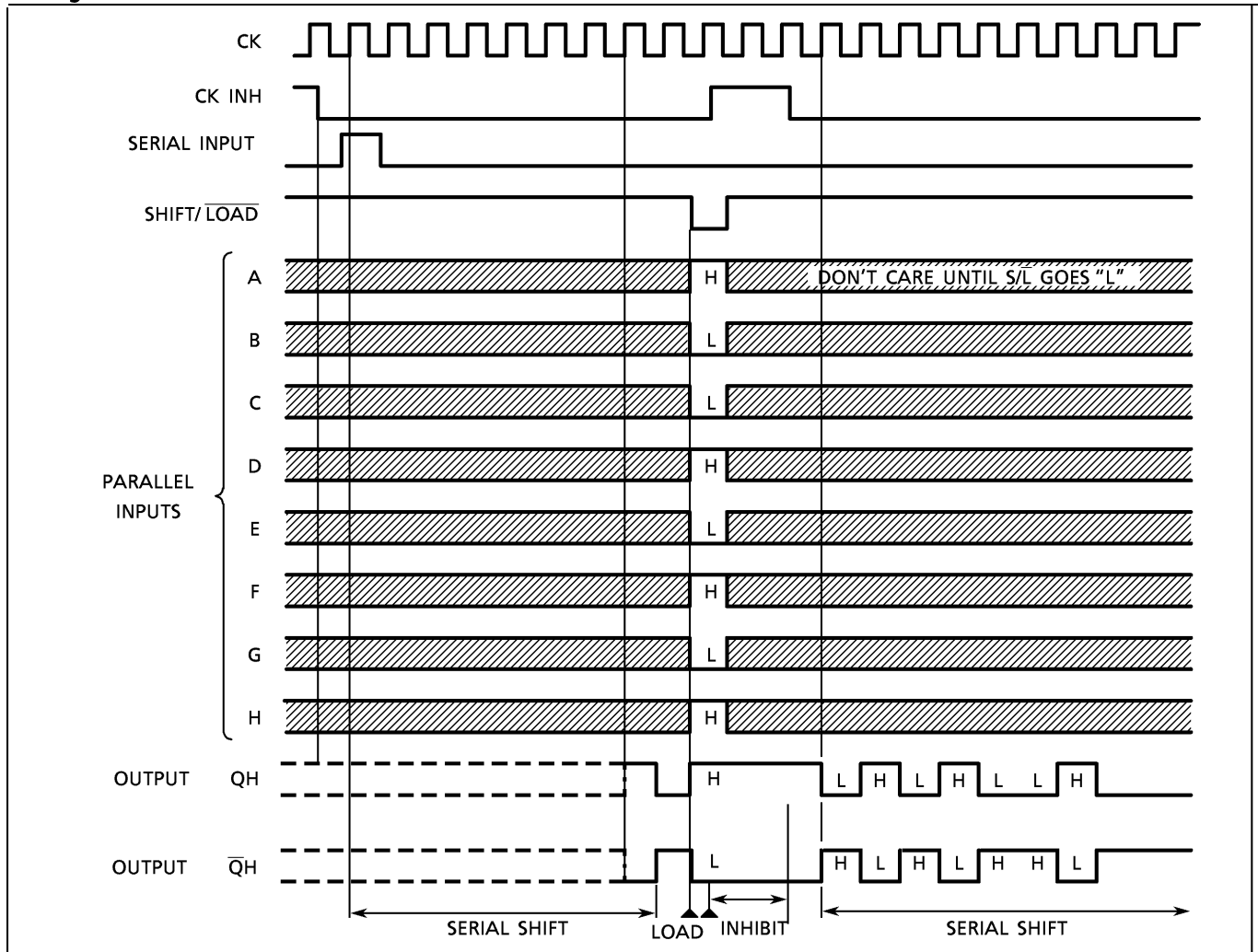
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Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT	
SHIFT/LOAD	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A ..... H	QA	QB	QH	$\bar{Q}H$
L	X	X	X	a ..... h	a	b	h	$\bar{h}$
H	L	$\downarrow$	H	X	H	QAn	QGn	$\bar{Q}Gn$
H	L	$\downarrow$	L	X	L	QAn	QGn	$\bar{Q}Gn$
H	$\downarrow$	L	H	X	H	QAn	QGn	$\bar{Q}Gn$
H	$\downarrow$	L	L	X	L	QAn	QGn	$\bar{Q}Gn$
H	X	H	X	X	NO CHANGE			
H	H	X	X	X	NO CHANGE			

X : Don't Care  
 a ..... h : The level of steady state input voltage at inputs A through H respectively  
 QAn~QGn: The level of QA~QG, respectively, before the most recent positive transition of the CK.

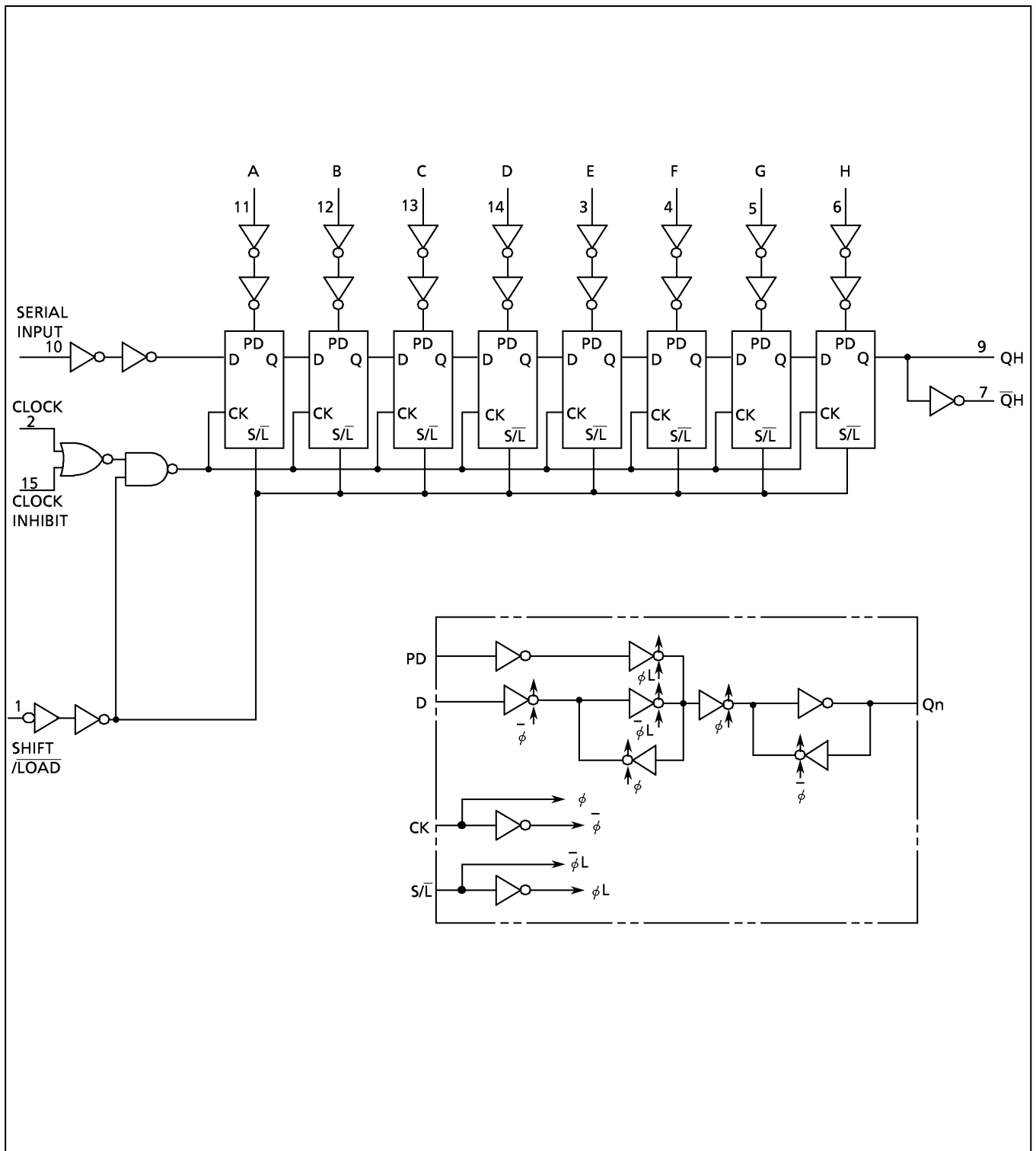
Timing Chart



980910EBA2'

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System Diagram



## Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

## Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 ( $V_{CC} = 3.3 \pm 0.3V$ ) 0~20 ( $V_{CC} = 5 \pm 0.5V$ )	ns / V

## DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT		
				Min	Typ.	Max	Min	Max			
High - Level Input Voltage	$V_{IH}$		2.0 3.0~5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V		
Low - Level Input Voltage	$V_{IL}$		2.0 3.0~5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V		
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V	
			$I_{OH} = -4\text{mA}$	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —		
			$I_{OH} = -8\text{mA}$	3.0 4.5	— —	— —	— —	0.36 0.36	— —		0.44 0.44
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V	
			$I_{OL} = 4\text{mA}$	3.0 4.5	— —	— —	— —	— —	— —		0.44 0.44
			$I_{OL} = 8\text{mA}$	3.0 4.5	— —	— —	— —	— —	— —		— —
Input Leakage Current	$I_{IN}$	$V_{IN} = 5.5V$ or GND	0~5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$		
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0			

Timing Requirements (Input  $t_r = t_f = 3ns$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	Limit	Limit	Limit	
Minimum Pulse Width (CK, CK INH)	$t_{W(L)}$ $t_{W(H)}$		3.3 ± 0.3	6.0	7.0	ns	
			5.0 ± 0.5	4.0	4.0		
Minimum Pulse Width (S/ $\bar{L}$ )	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	7.5 5.0	9.0 6.0		
Minimum Set-up Time (PI-S/ $\bar{L}$ )	$t_s$		3.3 ± 0.3 5.0 ± 0.5	7.5 5.0	8.5 5.0		
Minimum Set-up Time (SI-CK, CK INH)	$t_s$		3.3 ± 0.3 5.0 ± 0.5	5.0 4.0	6.0 4.0		
Minimum Set-up Time (S/ $\bar{L}$ -CK, CK INH)	$t_s$		3.3 ± 0.3 5.0 ± 0.5	5.0 4.0	6.0 4.0		
Minimum Hold Time (PI-S/ $\bar{L}$ )	$t_h$		3.3 ± 0.3 5.0 ± 0.5	0.5 1.0	0.5 1.0		
Minimum Hold Time (SI-CK, CK INH)	$t_h$		3.3 ± 0.3 5.0 ± 0.5	0.0 0.5	0.0 0.5		
Minimum Hold Time (S/ $\bar{L}$ -CK, CK INH)	$t_h$		3.3 ± 0.3 5.0 ± 0.5	0.0 0.5	0.0 0.5		
Minimum Removal Time (CK INH-CK) (CK-CK INH)	$t_{rem}$		3.3 ± 0.3	5.0	5.0		
			5.0 ± 0.5	3.5	3.5		

AC Electrical Characteristics (Input  $t_r = t_f = 3ns$ )

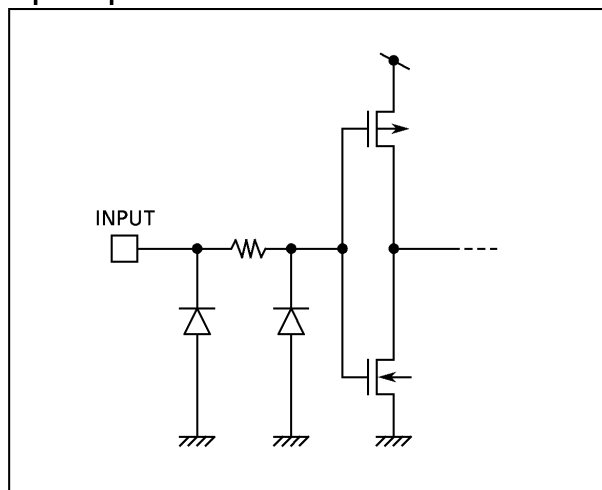
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V <sub>CC</sub> (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time (CK, CK INH-QH, QH)	t <sub>pLH</sub>	3.3 ± 0.3	15	—	9.9	15.4	1.0	18.0	ns
			50	—	12.4	18.9	1.0	21.5	
	5.0 ± 0.5	15	—	6.6	9.9	1.0	11.5		
		50	—	8.1	11.9	1.0	13.5		
Propagation Delay Time (S/L-QH, QH)	t <sub>pLH</sub>	3.3 ± 0.3	15	—	9.9	15.8	1.0	18.5	
			50	—	12.4	19.3	1.0	22.0	
	5.0 ± 0.5	15	—	6.7	9.9	1.0	11.5		
		50	—	8.2	11.9	1.0	13.5		
Propagation Delay Time (H-QH, QH)	t <sub>pLH</sub>	3.3 ± 0.3	15	—	9.2	14.1	1.0	16.5	
			50	—	11.7	17.6	1.0	20.0	
	5.0 ± 0.5	15	—	5.9	9.0	1.0	10.5		
		50	—	7.4	11.0	1.0	12.5		
Maximum Clock Frequency	f <sub>MAX</sub>	3.3 ± 0.3	15	65	85	—	55	—	MHz
			50	60	105	—	50	—	
		5.0 ± 0.5	15	110	150	—	90	—	
			50	95	130	—	85	—	
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 1)		—	50	—	—	—	

Note (1): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

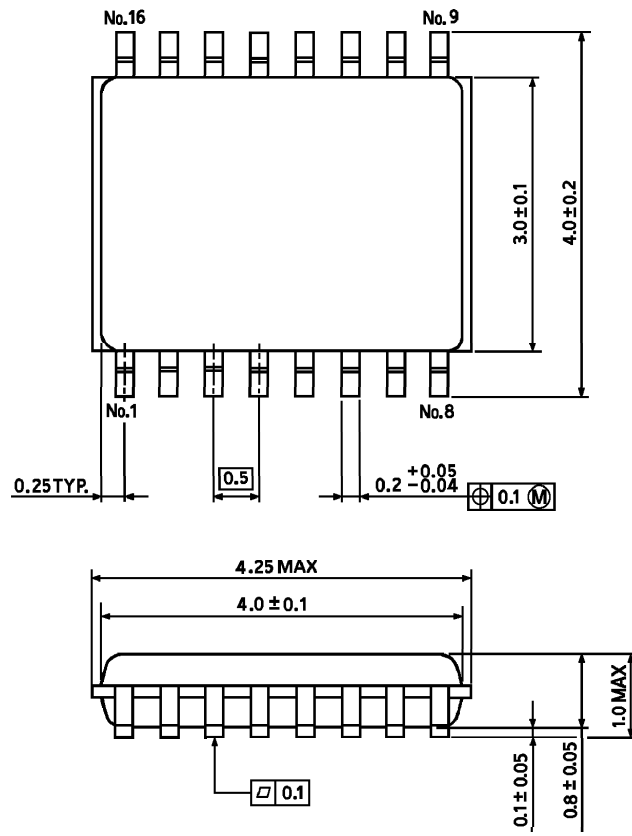
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Input Equivalent Circuit



Outline Drawing  
VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02g (Typ.)