

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MZ373FK

LOW VOLTAGE OCTAL D-TYPE LATCH WITH 5 V TOLERANT INPUTS AND OUTPUTS

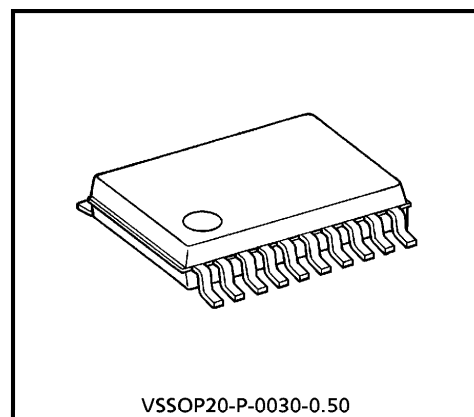
The TC7MZ373 is a high performance CMOS OCTAL D-TYPE LATCH. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This 8 bit D-type latch is controlled by a latch enable input (LE) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.



VSSOP20-P-0030-0.50

Weight : 0.03 g (typ.)

Features

- Low voltage operation : $V_{CC} = 2.0\sim 3.6\text{ V}$
- High speed operation : $t_{pd} = 8.0\text{ ns (max)}$
($V_{CC} = 3.0\sim 3.6\text{ V}$)
- Output current : $|I_{OH}|/I_{OL} = 24\text{ mA (min)}$
($V_{CC} = 3.0\text{ V}$)
- Latch-up performance : $\pm 500\text{ mA}$
- Available in VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 373 type.

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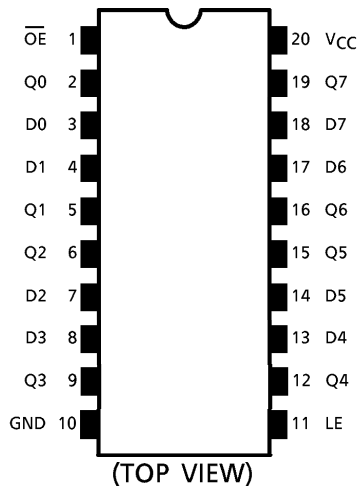
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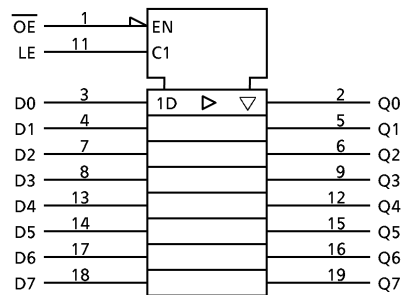
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Pin Assignment



IEC Logic Symbol

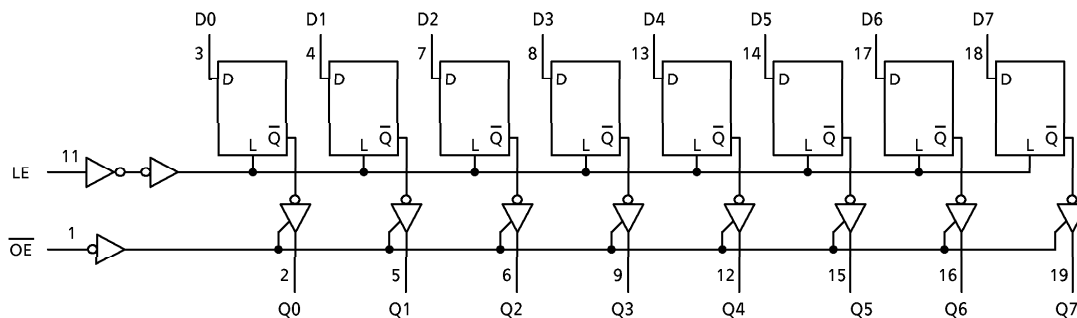


Truth Table

| INPUTS | | | OUTPUTS |
|-----------------|----|---|---------|
| \overline{OE} | LE | D | |
| H | X | X | Z |
| L | L | X | Qn |
| L | H | L | L |
| L | H | H | H |

- X : Don't Care
- Z : High Impedance
- Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Maximum Ratings

| PARAMETER | SYMBOL | RATING | UNIT |
|-----------------------------|------------------|-------------------------------|------|
| Supply Voltage Range | V_{CC} | -0.5~7.0 | V |
| DC Input Voltage | V_{IN} | -0.5~7.0 | V |
| DC Output Voltage | V_{OUT} | -0.5~7.0 (Note 1) | V |
| | | -0.5~ V_{CC} + 0.5 (Note 2) | |
| Input Diode Current | I_{IK} | -50 | mA |
| Output Diode Current | I_{OK} | ±50 (Note 3) | mA |
| DC Output Current | I_{OUT} | ±50 | mA |
| Power Dissipation | P_D | 180 | mW |
| DC V_{CC} /Ground Current | I_{CC}/I_{GND} | ±100 | mA |
| Storage Temperature | T_{stg} | -65~150 | °C |

(Note 1): Output in Off-State

(Note 2): High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3): $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

| PARAMETER | SYMBOL | RATING | UNIT |
|--------------------------|-----------------|----------------------|------|
| Supply Voltage | V_{CC} | 2.0~3.6 | V |
| | | 1.5~3.6 (Note 4) | |
| Input Voltage | V_{IN} | 0~5.5 | V |
| Output Voltage | V_{OUT} | 0~5.5 (Note 5) | V |
| | | 0~ V_{CC} (Note 6) | |
| Output Current | I_{OH}/I_{OL} | ±24 (Note 7) | mA |
| | | ±12 (Note 8) | |
| Operating Temperature | T_{opr} | -40~85 | °C |
| Input Rise And Fall Time | dt/dv | 0~10 (Note 9) | ns/V |

(Note 4): Data Retention Only

(Note 5): Output in Off-State

(Note 6): High or Low State

(Note 7): $V_{CC} = 3.0\sim 3.6$ V

(Note 8): $V_{CC} = 2.7\sim 3.0$ V

(Note 9): $V_{IN} = 0.8\sim 2.0$ V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC characteristics (Ta = -40~85°C)

| PARAMETER | | SYMBOL | TEST CONDITION | V _{CC} (V) | Min | Max | UNIT | |
|---------------------------------------|-----------|------------------|--|---------------------------|---------|-----------------------|------|---|
| | | | | | | | | |
| Input Voltage | "H" Level | V _{IH} | | 2.7~3.6 | 2.0 | — | V | |
| | "L" Level | V _{IL} | | 2.7~3.6 | — | 0.8 | | |
| Output Voltage | "H" Level | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -100 μA | 2.7~3.6 | V _{CC} - 0.2 | — | V |
| | | | | I _{OH} = -12 mA | 2.7 | 2.2 | — | |
| | | | | I _{OH} = -18 mA | 3.0 | 2.4 | — | |
| | | | | I _{OH} = -24 mA | 3.0 | 2.2 | — | |
| | "L" Level | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 100 μA | 2.7~3.6 | — | 0.2 | |
| | | | | I _{OL} = 12 mA | 2.7 | — | 0.4 | |
| | | | | I _{OL} = 16 mA | 3.0 | — | 0.4 | |
| | | | | I _{OL} = 24 mA | 3.0 | — | 0.55 | |
| Input Leakage Current | | I _{IIN} | V _{IN} = 0~5.5 V | 2.7~3.6 | — | ± 5.0 | μA | |
| 3-State Output Off-State Current | | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~5.5 V | 2.7~3.6 | — | ± 5.0 | μA | |
| Power Off Leakage Current | | I _{OFF} | V _{IN} / V _{OUT} = 5.5 V | 0 | — | 10.0 | μA | |
| Quiescent Supply Current | | I _{CC} | V _{IN} = V _{CC} or GND | 2.7~3.6 | — | 10.0 | μA | |
| | | | V _{IN} / V _{OUT} = 3.6~5.5 V | 2.7~3.6 | — | ± 10.0 | | |
| Increase In I _{CC} Per Input | | ΔI _{CC} | V _{IH} = V _{CC} - 0.6 V | 2.7~3.6 | — | 500 | μA | |

AC characteristics (Ta = -40~85°C)

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Min | Max | UNIT |
|-------------------------------|--------------------|----------------|---------------------|-----|-----|------|
| | | | | | | |
| Propagation Delay Time (D-Q) | t _{pLH} | (Fig.1, 2) | 2.7 | — | 9.0 | ns |
| | t _{pHL} | | 3.3 ± 0.3 | 1.5 | 8.0 | |
| Propagation Delay Time (LE-Q) | t _{pLH} | (Fig.1, 2) | 2.7 | — | 9.5 | ns |
| | t _{pHL} | | 3.3 ± 0.3 | 1.5 | 8.5 | |
| Output Enable Time | t _{pZL} | (Fig.1, 3) | 2.7 | — | 9.5 | ns |
| | t _{pZH} | | 3.3 ± 0.3 | 1.5 | 8.5 | |
| Output Disable Time | t _{pLZ} | (Fig.1, 3) | 2.7 | — | 8.5 | ns |
| | t _{pHZ} | | 3.3 ± 0.3 | 1.5 | 7.5 | |
| Minimum Pulse Width (LE) | t _w (H) | (Fig.1, 2) | 2.7 | 4.0 | — | ns |
| | | | 3.3 ± 0.3 | 3.3 | — | |
| Minimum Set-Up Time | t _s | (Fig.1, 2) | 2.7 | 2.5 | — | ns |
| | | | 3.3 ± 0.3 | 2.5 | — | |
| Minimum Hold Time | t _h | (Fig.1, 2) | 2.7 | 1.5 | — | ns |
| | | | 3.3 ± 0.3 | 1.5 | — | |
| Output To Output Skew | t _{osLH} | (Note 10) | 2.7 | — | — | ns |
| | t _{osHL} | | 3.3 ± 0.3 | — | 1.0 | |

(Note 10): Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics (Ta = 25°C, Input t_r = t_f = 2.5 ns, C_L = 50 pF, R_L = 500 Ω)

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Typ. | UNIT |
|--|------------------|--|---------------------|------|------|
| | | | | | |
| Quiet Output Maximum Dynamic V _{OL} | V _{OLP} | V _{IH} = 3.3 V, V _{IL} = 0 V | 3.3 | 0.8 | V |
| Quiet Output Minimum Dynamic V _{OL} | V _{OLV} | V _{IH} = 3.3 V, V _{IL} = 0 V | 3.3 | 0.8 | V |

Capacitive Characteristics (Ta = 25°C)

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Typ. | UNIT |
|-------------------------------|------------------|------------------------------------|---------------------|------|------|
| | | | | | |
| Input Capacitance | C _{IN} | — | 3.3 | 7 | pF |
| Output Capacitance | C _{OUT} | | 3.3 | 8 | pF |
| Power Dissipation Capacitance | C _{PD} | f _{IN} = 10 MHz (Note 11) | 3.3 | 25 | pF |

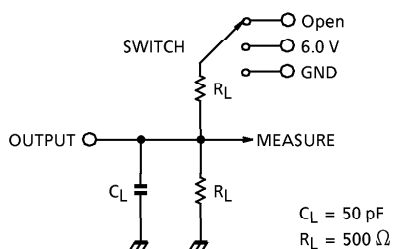
(Note 11): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Test Circuit

Fig.1



| PARAMETER | SWITCH |
|--------------------|--------|
| t_{pLH}, t_{pHL} | Open |
| t_{pLZ}, t_{pZL} | 6.0 V |
| t_{pHZ}, t_{pZH} | GND |
| t_w, t_s, t_h | Open |

AC Waveform

Fig.2 $t_{pLH}, t_{pHL}, t_w, t_s, t_h$

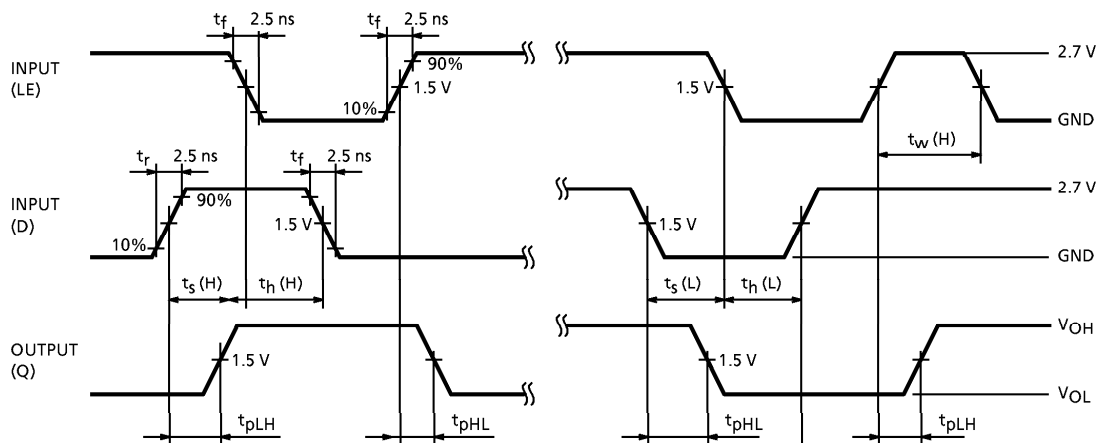
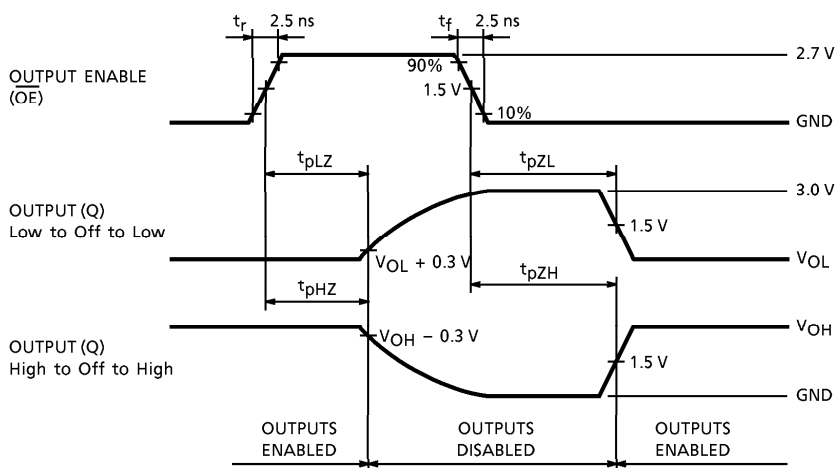
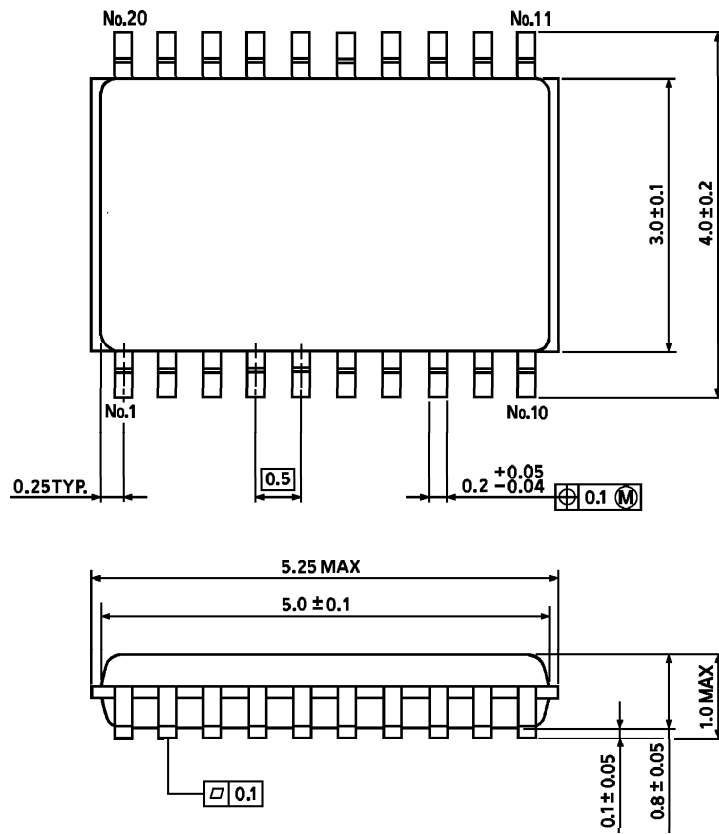


Fig.3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$



Outline Drawing
VSSOP20-P-0030-0.50

Unit : mm



Weight : 0.03 g (typ.)