TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MZ541FK

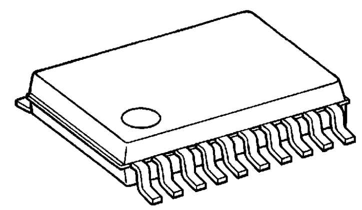
LOW VOLTAGE OCTAL BUS BUFFER WITH 5 V TOLERANT INPUTS AND OUTPUTS

The TC7MZ541 is a high performance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The TC7MZ541 is a non-inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



VSSOP20-P-0030-0.50

Weight : 0.03 g (typ.)

Features

- Low voltage operation : V_{CC} = 2.0~3.6 V
- High speed operation : t_{pd} = 6.5 ns (max) (V_{CC} = 3.0~3.6 V)
- Output current : $|I_{OH}| / I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance : ±500 mA
- Available in VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / VHC / HC / F / ALS / LS etc.) 541 type.

980910EBA1

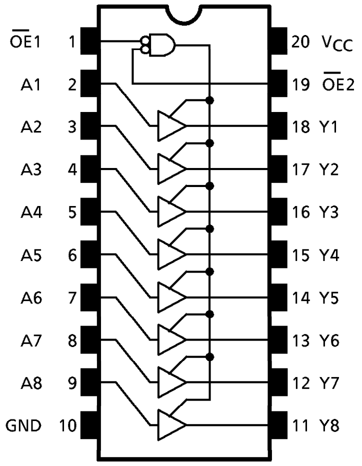
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

● The products described in this document are subject to the foreign exchange and foreign trade laws.

● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

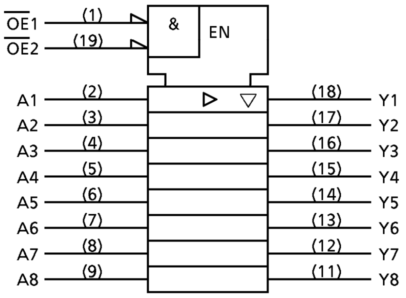
● The information contained herein is subject to change without notice.

Pin Assignment



(TOP VIEW)

IEC Logic Symbol



Truth Table

INPUTS			OUTPUTS
$\overline{OE}1$	$\overline{OE}2$	An	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X : Don't Care
Z : High Impedance

Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1): Output in Off-State
(Note 2): High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3): $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 9)	ns / V

(Note 4): Data Retention Only
(Note 5): Output in Off-State
(Note 6): High or Low State
(Note 7): V_{CC} = 3.0~3.6 V
(Note 8): V_{CC} = 2.7~3.0 V
(Note 9): V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C)

PARAMETER		SYMBOL	TEST CONDITION			Min	Max	UNIT
					V_{CC} (V)			
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7~3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~5.5 V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5 V		2.7~3.6	—	±5.0	μA
Power Off Leakage Cuurent		I_{OFF}	V_{IN} / V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
			V_{IN} / V_{OUT} = 3.6~5.5 V		2.7~3.6	—	±10.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7~3.6	—	500	μA

AC characteristic (Ta = −40~85°C)

PARAMETER	SYMBOL	TEST CONDITION		Min	Max	UNIT
			V_{CC} (V)			
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig.1, 2)	2.7	—	7.5	ns
			3.3 ± 0.3	1.5	6.5	
Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	2.7	—	8.5	ns
			3.3 ± 0.3	1.5	7.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10): Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics (Ta = 25°C, Input $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Typ.	UNIT
			V_{CC} (V)		
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 3.3$ V, $V_{IL} = 0$ V	3.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	$V_{IH} = 3.3$ V, $V_{IL} = 0$ V	3.3	0.8	V

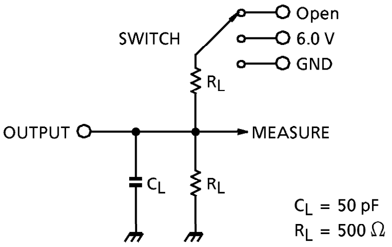
Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION		Typ.	UNIT
			V_{CC} (V)		
Input Capacitance	C_{IN}	—	3.3	7	pF
Output Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10$ MHz (Note 11)	3.3	40	pF

(Note 11): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

Test Circuit

Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V
t_{pHZ}, t_{pZH}	GND

AC Waveform

Fig.2 t_{pLH}, t_{pHL}

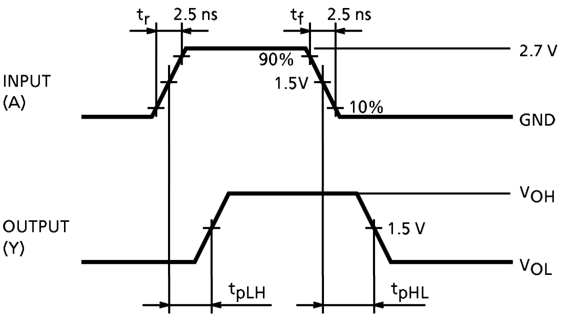
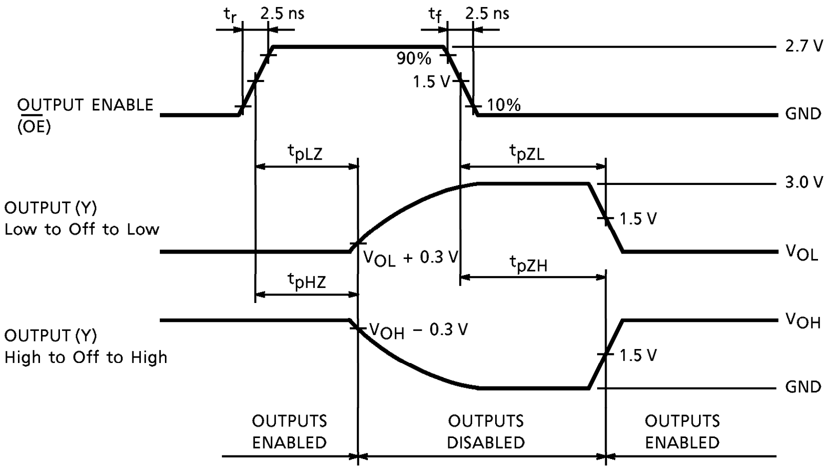


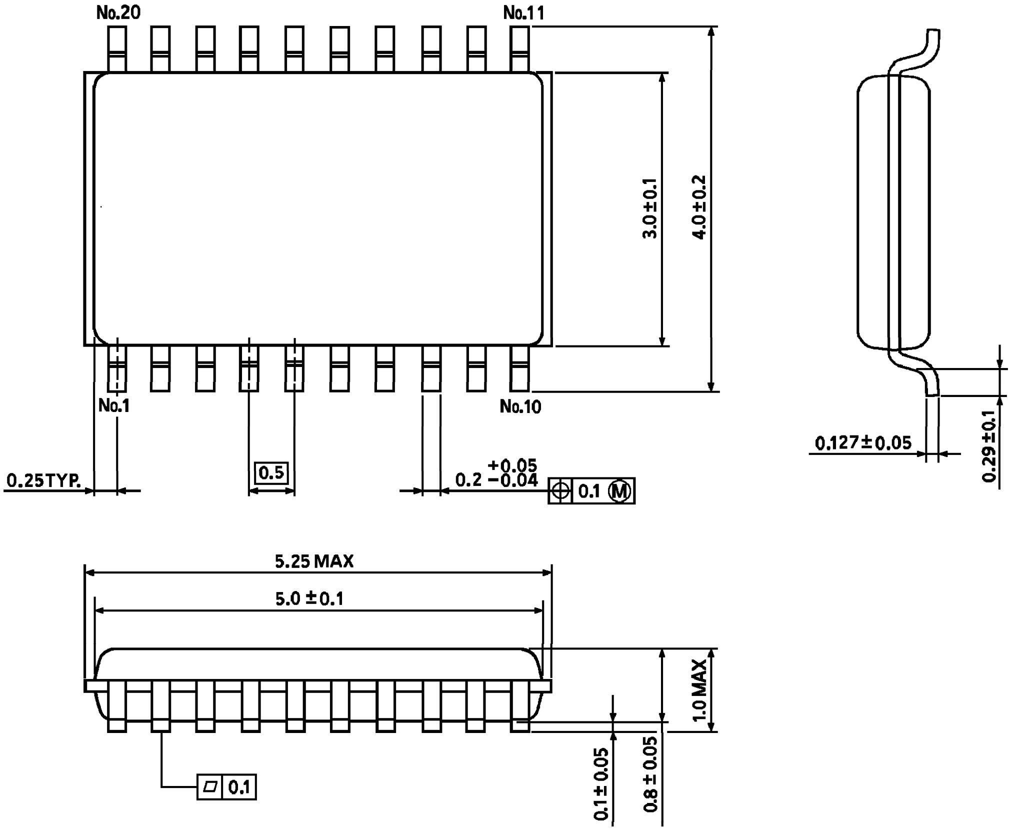
Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



PACKAGE DIMENSIONS

VSSOP20-P-0030-0.50

Unit : mm



Weight : 0.03 g (typ.)