

TC7SB66FU

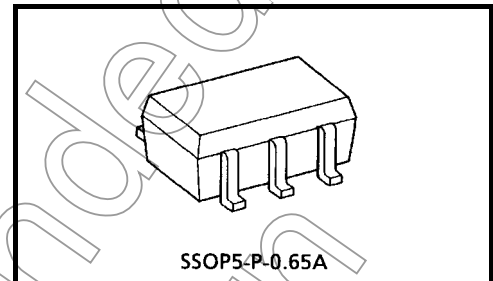
Single Bus Switch

The TC7SB66FU is a low on-resistance, high-speed CMOS 1-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (OE) is at High level, the switch is on; when at Low level, the switch is off.

P-MOS and N-MOS channel block means the device is suitable for analog signal transmission.

All inputs are equipped with protector circuits to protect the device from static discharge.

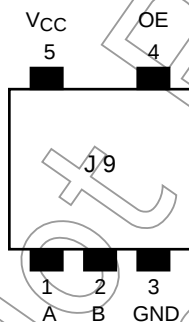


Weight: 0.006 g (typ.)

Features

- Operating voltage: $V_{CC} = 2 \sim 5.5 \text{ V}$
- High speed operation: $t_{pd} = 0.25 \text{ ns (max)}$
- Ultra-low on resistance: $R_{ON} = 5 \Omega \text{ (typ.)}$
- ESD performance: Machine model $\geq \pm 200 \text{ V}$
Human body model $\geq \pm 2000 \text{ V}$
- High noise margin: $V_{NIL} = V_{NIH} = 28\% V_{CC} \text{ (min)}$
- Power-down protection for inputs (control inputs only)
- Package: USV

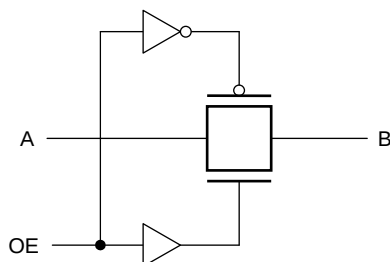
Pin Assignment (top view)



Truth Table

Inputs	Function
OE	
H	A port = B port
L	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	-0.5~7.0	V
Control pin input voltage		V_{IN}	-0.5~7.0	V
Switch terminal I/O voltage		V_S	-0.5~ $V_{CC} + 0.5$	V
Clump diode current	Control input pin	I_{IK}	-50	mA
	Switch terminal		±50	
Switch I/O current		I_S	128	mA
Power dissipation		P_D	200	mW
DC V_{CC} /GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~5.5	V
Control pin input voltage	V_{IN}	0~5.5	V
Switch I/O voltage	V_S	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition	V _{CC} (V)	Min	Typ. (Note 1)	Max	Unit
Control pin input voltage	“H” level	V _{IH}	—	2.0~5.5	0.7 × V _{CC}	—	—	V
	“L” level	V _{IL}	—	2.0~5.5	—	—	0.3 × V _{CC}	
Control pin input leakage current		I _{IIN}	V _{IIN} = 0~5.5 V	2.0~5.5	—	—	±1.0	μA
Off-state leakage current (switch off)		I _{ISZ}	A, B = 0~V _{CC} , OE = GND	2.0~5.5	—	—	±1.0	μA
ON resistance (Note 2)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA	4.5	—	3	7	Ω	
		V _{IS} = 4.5 V, I _{IS} = 30 mA	4.5	—	5	15		
		V _{IS} = 2.4 V, I _{IS} = 15 mA	4.5	—	6	12		
		V _{IS} = 0 V, I _{IS} = 24 mA	3.0	—	4	9		
		V _{IS} = 3 V, I _{IS} = 24 mA	3.0	—	7	20		
		V _{IS} = 0 V, I _{IS} = 8 mA	2.0	—	6	12		
		V _{IS} = 2 V, I _{IS} = 8 mA	2.0	—	10	30		
Quiescent supply current		I _{CC}	V _{IIN} = V _{CC} or GND, I _{OUT} = 0	5.5	—	—	10	μA

Note 1: The typical values are at Ta = 25°C.

Note 2: Apply the specified current to the switch, then measure the voltages on pins A and B. The on-resistance is the lower of the two.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note)		2.0	—	0.5	ns
				3.3 ± 0.3	—	0.35	
				5.0 ± 0.5	—	0.25	
Output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3		2.0	—	8	ns
				3.3 ± 0.3	—	5	
				5.0 ± 0.5	—	4.5	
Output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3		2.0	—	8	ns
				3.3 ± 0.3	—	6.5	
				5.0 ± 0.5	—	5	

Note: The propagation delay time is calculated by the RC (on-resistance and load capacitance) time constant.

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Control pin input capacitance		C _{IN}	(Note)	5.0	3	pF
Switch terminal capacitance		C _{I/O}	OE = GND (Note)	5.0	10	pF

Note: Guaranteed by design.

Switch

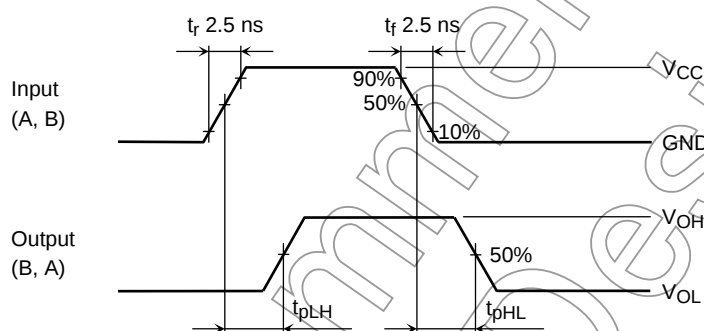
- Open
- $2 \times V_{CC}$
- GND

Output

Measure

$C_L = 50 \text{ pF}$
 $R_L = 500 \Omega$

Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	$2 \times V_{CC}$
t_{pHZ}, t_{pZH}	GND

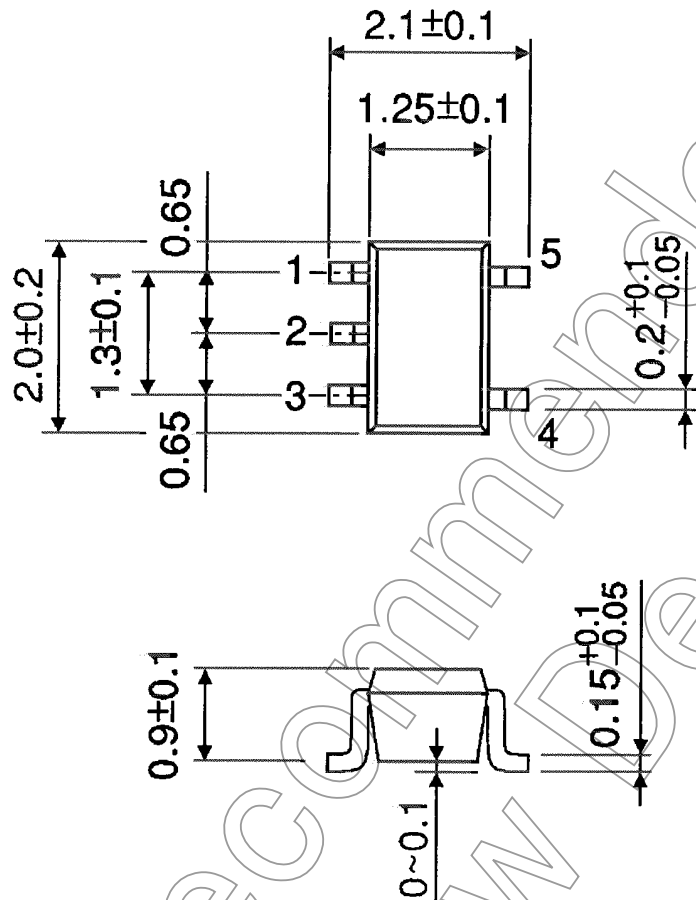


Timing diagram for the 74VHC125. The diagram shows the relationship between the Output Enable (OE) signal and the outputs A and B. The OE signal is active-low, with a pulse width of 2.5 ns. The outputs A and B are shown in two states: Low to Off to Low and High to Off to High. The timing parameters include t_f (fall time), t_r (rise time), t_{pLZ} (propagation delay from OE low to output low), t_{pHZ} (propagation delay from OE high to output high), t_{pLH} (propagation delay from OE low to output high), and t_{pHL} (propagation delay from OE high to output low). The outputs are shown with 10%, 50%, and 90% voltage levels.

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

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