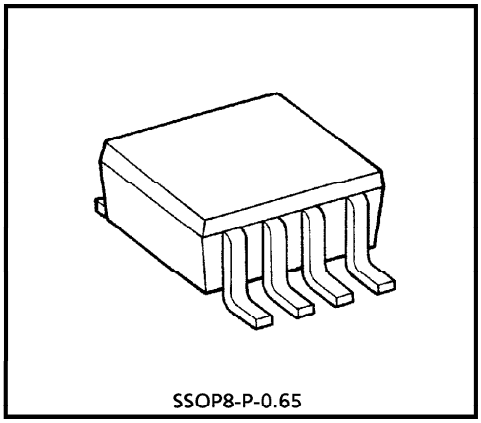
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7W126FU

DUAL BUS BUFFER

The TC7W126FU is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.
The require 3-state control input G to be set low to place the output into the high impedance.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight : 0.02g (Typ.)

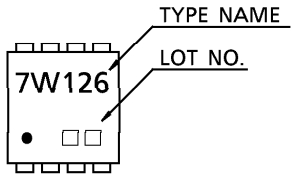
FEATURES

- High Speed ····· t_{pd} = 10ns (Typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 2μA (Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 6mA (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· $V_{CC\,(opr)}$ = 2~6V

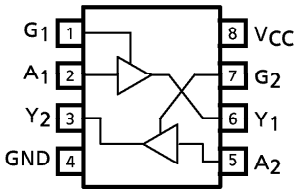
MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±37.5	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10s)	T_L	260	°C

MARKING



PIN ASSIGNMENT (TOP VIEW)



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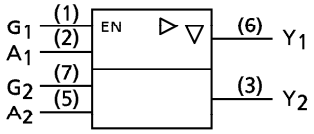
LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X : Don't Care
Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CIR-CUIT	TEST CONDITION		V_{CC}	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}	—	—		2.0 4.5 6.0	1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	V
Low-Level Input Voltage	V_{IL}	—	—		2.0 4.5 6.0	— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	—	V_{IN} = V_{IH}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
				I_{OH} = −6mA I_{OH} = −7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low-Level Output Voltage	V_{OL}	—	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
				I_{OL} = 6mA I_{OL} = 7.8mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	—	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	—	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	—	V_{IN} = V_{CC} or GND		6.0	—	—	2.0	—	20.0	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CIR-CUIT	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
				C_L	V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}	—	—	50	2.0	—	20	60	—	75	ns
					4.5	—	6	12	—	15	
					6.0	—	5	10	—	13	
Propagation Delay Time	t_{pLH} t_{pHL}	—	—	50	2.0	—	30	90	—	115	
					4.5	—	11	18	—	23	
					6.0	—	10	15	—	20	
				150	2.0	—	42	130	—	165	
					4.5	—	14	26	—	33	
					6.0	—	12	22	—	28	
Output Enable Time	t_{pZL} t_{pZH}	—	$R_L = 1k\Omega$	50	2.0	—	30	90	—	115	
					4.5	—	11	18	—	23	
					6.0	—	10	15	—	20	
				150	2.0	—	42	130	—	165	
					4.5	—	14	26	—	33	
					6.0	—	12	22	—	28	
Output Disable Time	t_{pLZ} t_{pHZ}	—	$R_L = 1k\Omega$	50	2.0	—	24	100	—	125	
					4.5	—	12	20	—	25	
					6.0	—	10	17	—	21	
Input Capacitance	C_{IN}	—	—	—	—	—	5	10	—	10	pF
Output Capacitance	C_{OUT}	—	—	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C_{PD}	—	Note (1)	—	—	—	32	—	—	—	

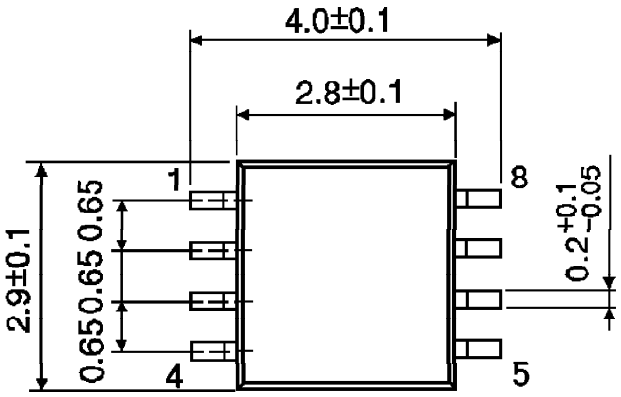
Note (1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

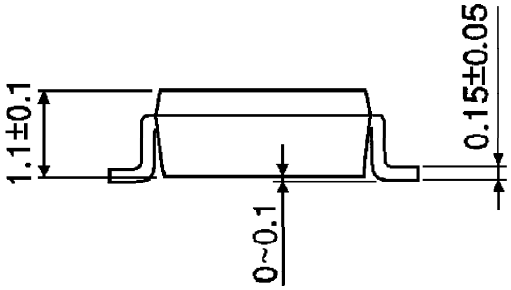
$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \quad \text{(per Gate)}$$

OUTLINE DRAWING

SSOP8-P-0.65

Unit : mm





Weight : 0.02g (Typ.)