TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH245FU, TC7WH245FK

Dual Bus Transceiver

FEATURES

• High Speed : $t_{pd} = 4.0 \text{ ns (typ.)}$

at $V_{CC} = 5 \text{ V}, C_{L} = 15 \text{pF}$

Low Power Dissipation : I_{CC} = 2 μA (max) at Ta = 25°C
 High Noise Immunity : V_{NIH} = V_{NIL} = 28% V_{CC} (min)

• Balanced Propagation Delays: t_{pLH} ≈ t_{pHL}

• Wide Operating Voltage Range: V_{CC (opr)} = 2 to 5.5 V

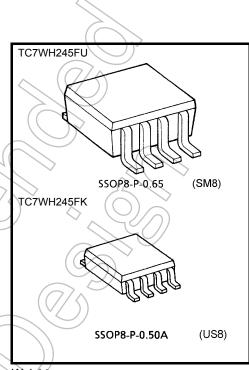
• Low Noise : V_{OLP} = 0.8 V (max)

APPLICATION NOTES

 Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

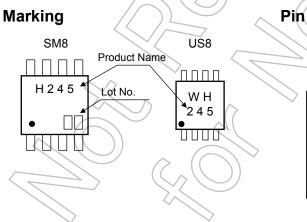
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

A parasitic diode is formed between the bus and Vcc terminals.
 Therefore bus terminal can not be used to interface 5V to 3V systems directly.

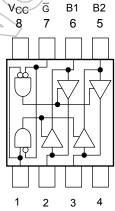


Weight

SSOP8-P-0.65 : 0.02 g (typ.) SSOP8-P-0.50A : 0.01 g (typ.)







DIR A1 A2 GND

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply Voltage	V _{CC}	−0.5 to 7	V
DC Input Voltage	V _{IN}	–0.5 tp 7	٧
DC Output Voltage	V _{OUT}	-0.5 toV _{CC} + 0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	lok	±20 (Note 1)	mA
DC Output Current	lout	±25	mA (
DC Vcc/Ground Current	ICC	±50	mA
Dower Dissination	D-	300(SM8)	mW
Power Dissipation	P _D	200(US8)	HIVV
Strage Temperature	T _{stg}	-65 to 150	°Ç
LeadTemperature(10s)	TL	260	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: V_{OUT} < GND, V_{OUT} > V_{CC}

IEC Logic Symbol

G3 DIR (1) G3 3 EN 1 [BA] 3 EN 2 [AB] A1 (2) V1 (6) B1

Truth Table

	Inp	out	Fund	Output	
	G	DIR	A BUS	Output	
I		7/r	OUTPUT	INPUT	A = B
	(4)/^	H	INPUT	B=A	
	(H)) x	High im	Z	

X: Don't care

Z: High impedance

Operating Ranges

Characteristic	Symbol	Rating	Unit	
Supply Voltage	Acc	2 to 5.5	V	
Input Voltage	V _{IN}	0 to 5.5	V	
Output Voltage	V _{OUT}	0 to V _{CC}	V	
Operating Temperature	T _{opr}	-40 to 85	°C	
Input Rise and Fall Time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3 \text{ V}$)	nc/\/	
imput rase and rail rime	avav	0 to 20 (V _{CC} = 5.0 ± 0.5 V)	ns/V	

B2

Electrical Characteristics

DC Characteristics

Characteristic Symbol Test Condition		Toot Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
		V _{CC} (V)	Min	Тур.	Max	Min	Max	Offic		
High-Level				2.0	1.5	_ <	X	1.5	_	
Input Voltage		_		3.0 to 5.5	V _{CC} × 0.7			V _{CC} ⊗0.7		V
Low-Level .				2.0	_	7	0.5	7 <u> </u>	0.5	V
Input Voltage	V _{IL}	_		3.0 to 5.5	_	1	V _{CC} × 0.3	_	$\begin{array}{c} V_{CC} \\ \times \ 0.3 \end{array}$	
				2.0	1.9	2.0		1.9		
	Voн	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -50 \mu A$	3.0	2.9	3.0		2.9		V
High-Level Output Voltage				4.5	4.4	4.5	_	4.4		
, -			$I_{OH} = -4 \text{ mA}$	3.0	2.58	_	- (2.48	>	
			$I_{OH} = -8 \text{ mA}$	4.5	3.94		+	3.80	_	
			/	2.0	<i>J</i>	0.0	0.1	(4)	0.1	V
			I _{OL} = 50 μA	3.0	_	0.0	0.1		0.1	
Low-Level Output Voltage	V_{OL}	V _{IN} = V _{IH} or V _{IL}	40	4.5	_	0.0	0.1	_	0.1	
			$I_{OL} = 4 \text{ mA}$	3.0	_		0.36	—	0.44	
			$I_{OL} = 8 \text{ mA}$	4.5	_	(4)	0.36	—	0.44	
3-State Output Off-State Current	loz	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5			±0.25	_	±2.50	μΑ
Input Leakage Current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5		//-	±0.1	_	±1.0	μΑ
Quiescent Spply Current	Icc	V _{IN} =V _{CC} or GND		5.5			2.0	_	20.0	μΑ

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristic	Symbol Test Condition				Ta = 25°C			Ta =-40 to 85°C		Unit
Characteristic	Symbol	rest Condition	V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Min	Max	Offic
			3.3 ± 0.3	15	_	5.8	8.4	1.0	10.0	
Propagation Delay	t _{pLH}		3.3 ± 0.3	50	_	8.3	11.9	1.0	13.5	ns
Time	t _{pHL}		5.0 ± 0.5	15	_	4.0	5.5	1.0	6.5	110
			3.0 ± 0.3	50	_	5.5	7.5	1.0	8.5	
		R _L = 1 kΩ	3.3 ± 0.3	15	_	8.5	13.2	1.0	15.5	
3-State Output Enable Time	t _{pZL} t _{pZH}		3.3 ± 0.3	50	₹ \	11.0/	16.7	1.0	19.0	ns
			5.0 ± 0.5	15	-	5.8	8.5	1.0	10.0	113
				50	-(7.3	10.6	1.0	12.0	
3-State Output	t _{pLZ}	$R_L = 1 k\Omega$	3.3 ± 0.3	50		11.5	15.8	1.0	18.0	ns
Disable Time	t _{pHZ}	N 1 K22	5.0 ± 0.5	50 <	7(-)	7.0	9.7	1.0	11.0	115
Output to Output	t _{osLH}	(NI=4= 0)	3.3 ± 0.3	50		_	1.5	2 -	1.5	ns
Skew	t _{osHL}	(Note 2)	5.0 ± 0.5	50	(()	-	1.0		1.0	115
Input Capacitance	C _{IN}	DIR, G				4	(10)	(H)	10	pF
Bus Input Capacitance	C _{I/O}	An, Bn			_	8	7 (\ \ \	_	pF
Power Dissipation Capacitance	C _{PD}		4	(Note 3)	_	21	(2)	_	_	pF

Note 2: Parameter guranteed by design.

 $t_{OSLH} = |t_{DLHm} - t_{DLHn}|, t_{OSHL} = |t_{DHLm} - t_{DHLn}|$

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calucurated from the operating current consumption without load.

Average iperating current can be obtained by the equation:

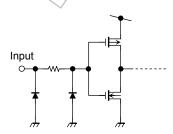
 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$

Noise Characteristics (Ta = 25°C, Input: $t_r = t_f = 3$ ns)

Characteritic	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Quiet Output Maximum Dynamic V _{OL}	VOLP	C _L = 50 pF	5.0	0.5	0.8	V
Quiet Output Minimum Dynamic VOL	V _{OLV}	C _L = 50 pF	5.0	-0.5	-0.8	٧
Minimum High Level Dynamic Input Voltage	Уінр	C _L = 50 pF	5.0	_	3.5	٧
Maximum Low Level Dynamic Input Voltage	VILD	C _L = 50 pF	5.0	_	1.5	V

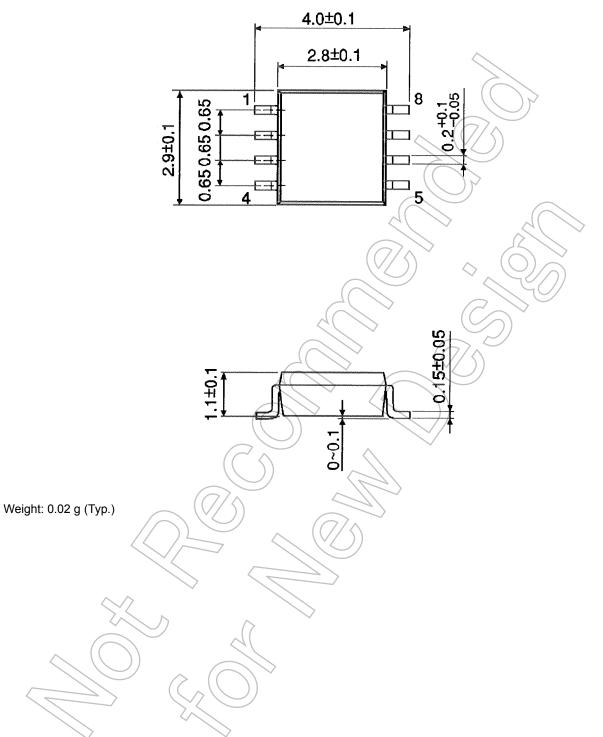
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Input Equivalent Circuit



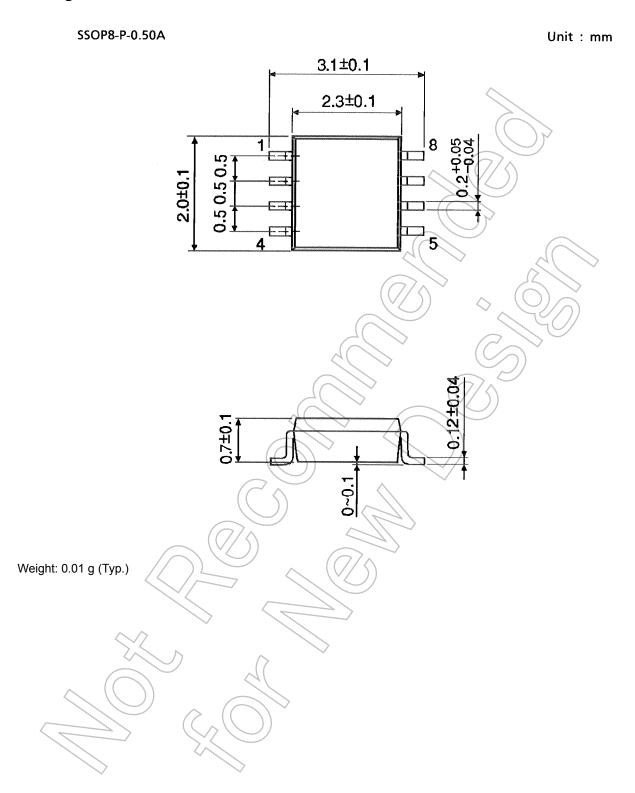
TOSHIBA

SSOP8-P-0.65 Unit: mm



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Package Dimensions



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