

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WPB306FC, TC7WPB306FK TC7WPB307FC, TC7WPB307FK

Low Voltage/Low Power 2-Bit Dual Supply Bus Switch

The TC7WPB306 and TC7WPB307 are high-speed CMOS two-bit bus switches with low ON-resistance that allow interfacing between different voltage nodes.

These devices have two separate power supplies, VL for a 1.8-V, 2.5-V or 3.3-V bus and VH for a 2.5-V, 3.3-V or 5.0-V bus.

For bidirectional level-shifting, the VH pin is connected to a high-voltage power supply through a bias resistor, and pull-up resistors are connected between the high-voltage power supply and the switch.

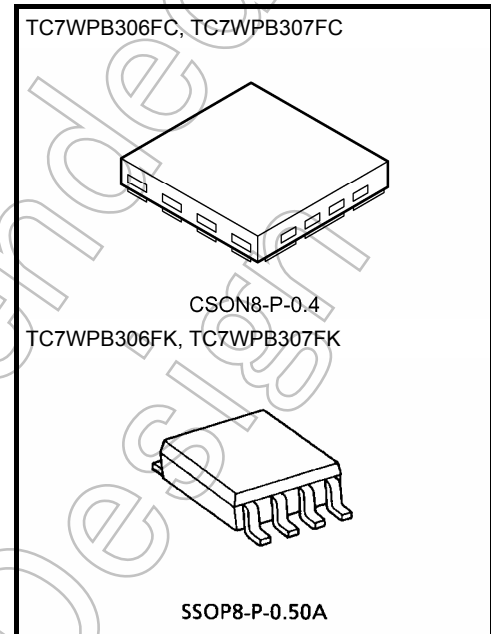
The enable signal can be used to disable the device so that the buses are effectively isolated.

For the TC7WPB306, Output Enable (OE) is active-High: When OE is High, the switch is on; when Low, the switch is off. For the TC7WPB307, Output Enable (\overline{OE}) is active-Low: When \overline{OE} is Low, the switch is on; when High, the switch is off.

The TC7WP306 and TC7WP307 support power-down protection by incorporating 5.5-V-tolerant control inputs.

The bus switch channels are fabricated with NMOS technology.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight	
CSON8-P-0.4	: 0.002 g (typ.)
SSOP8-P-0.50A	: 0.01 g (typ.)

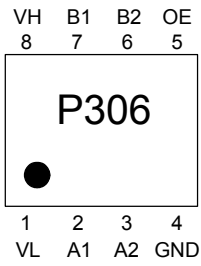
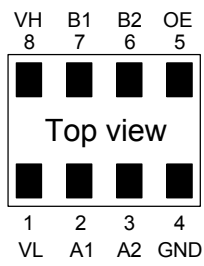
Features

- Operating voltage: 1.8-V to 2.5-V, 1.8-V to 3.6-V, 1.8-V to 5.5-V, 2.3-V to 3.6-V, 2.3-V to 5.5-V or 3.0-V to 5.5-V bidirectional interface
- Operating voltage: VL = 1.65 to 5.0 V, VH = VL + 0.5 to 5.5 V
- High-speed operation: $t_{pd} = 0.12\text{ns}(\text{max})$
(VL = 3.0 V, VH = 4.5 V)
- Low ON-resistance: RON = 3.0 Ω (typ.)
(ON-resistance test circuit: V_{IS} = 0 V, I_{IS} = 30 mA, VH = 4.5 V)
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- 5.5-V tolerance and power-down protection at the Output Enable input.
- Packages: CSON8 (CST8), SSOP8 (US8)

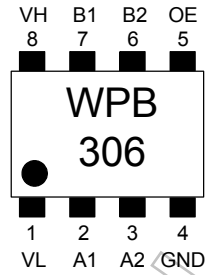
Start of commercial production
2006-09

Pin Assignment (top view), Marking

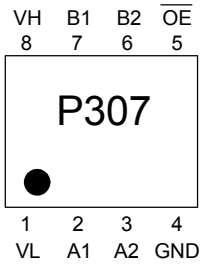
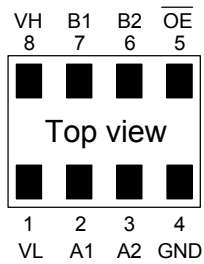
TC7WPB306FC



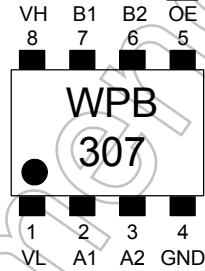
TC7WPB306FK



TC7WPB307FC



TC7WPB307FK

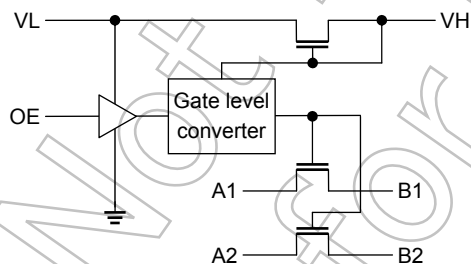


Truth Table

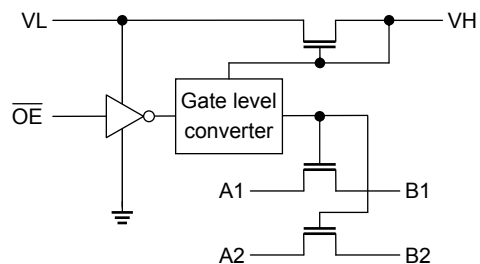
Input (306)	Function	Input (307)	Function
OE		$\overline{\text{OE}}$	
H	$A_n = B_n$	H	Disconnected
L	Disconnected	L	$A_n = B_n$

Circuit Schematic

TC7WPB306



TC7WPB307



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	VL	-0.5 to 7.0	V
	VH	-0.5 to 7.0	
Control input voltage (OE (306)/ OE (307))	V _{IN}	-0.5 to 7.0	V
Switch input/output voltage	V _S	-0.5 to 7.0	V
Clump diode current	I _{IK}	-50	mA
Switch input/output current	I _S	128	mA
DC V _{CC} /ground current per supply pin	I _{VL}	±25	mA
	I _{VH}	±25	
Power dissipation	P _D	150 (CSO8) 200 (SSOP8)	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	VL	1.65 to 5.0	V
	VH	2.3 to 5.5	
Control input voltage	V _{IN}	0 to 5.5	V
Switch input/output voltage	V _S	0 to 5.5	V
Operating temperature	T _{opr}	-40 to 85	°C
Control input rise and fall times	dt/dv	0 to 10	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Note 2: The voltage difference between the VL and the VH must be 0.5 V or greater. (VL < VH)

Application Circuit

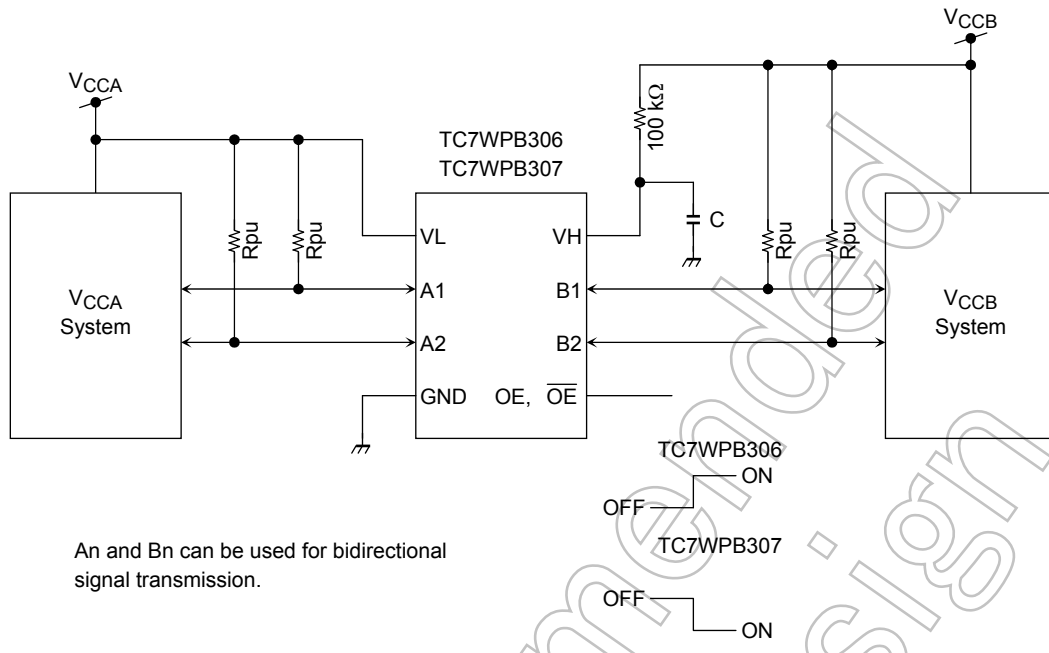


Figure 1 Application Circuit Diagram

The voltage difference between the (low-voltage) VCCA system and the (high-voltage) VCCB system must be 0.5 V or greater. ($V_{CCA} < V_{CCB}$)

For level-shifting between the VCCA and VCCB systems, connect a bias resistor between the VH pin and the VCCB system, and also connect pull-up resistors to An and Bn pins.

Not Recommended for New Design

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition	VL (V)	VH (V)	Ta = -40 to 85°C		Unit
						Min	Max	
Control input voltage	High-level	V _{IH}	OE (306), \overline{OE} (307)	1.65 ≤ VL < 2.3	(VL + 0.5) to 5.5	0.8 × VL	—	V
				2.3 ≤ VL ≤ 5.0	(VL + 0.5) to 5.5	0.7 × VL	—	
	Low-level	V _{IL}	OE (306), \overline{OE} (307)	1.65 ≤ VL < 2.3	(VL + 0.5) to 5.5	—	0.2 × VL	
				2.3 ≤ VL ≤ 5.0	(VL + 0.5) to 5.5	—	0.3 × VL	
ON-resistance (Note)	R _{ON}	V _{IS} = 0 V, I _S = 30 mA (Figure 2)	—	2.3	—	9.5	Ω	
			—	3.0	—	7.0		
			—	4.5	—	5.5		
Power off leakage current	I _{OFF}	An, Bn = 0 to 5.5V	0	0	—	±1.0	μA	
Switch-off leakage current	I _{SZ}	An, Bn = 0 to 5.5 V $\overline{OE} = VL, OE = GND$	1.65 to 5.0	(VL + 0.5) to 5.5	—	±1.0	μA	
Control input current	I _{IN}	\overline{OE} or OE = 0 to 5.5 V	1.65 to 5.0	(VL + 0.5) to 5.5	—	±1.0	μA	
Quiescent supply current	I _{VL1}	V _{IN} = VL or GND, I _S = 0 A	1.65 to 5.0	VL	—	2.0	μA	
	I _{VH1}	V _{IN} = VL or GND, I _S = 0 A	1.65 to 5.0	VL	—	2.0		
	I _{VL2}	VL ≤ V _{IN} ≤ 5.5 V, I _S = 0 A	1.65 to 5.0	VL	—	±2.0		
	I _{VH2}	VL ≤ V _{IN} ≤ 5.5 V, I _S = 0 A	1.65 to 5.0	VL	—	±2.0		

Note: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current. It depends on the VH voltage.

Not Recommended for New

AC Characteristics (Ta = -40 to 85°C, Input: tr = tf = 2.0 ns, f = 10kHz)

VL (VCCA) = 3.3 ± 0.3 V, VCCB = 5.0 ± 0.5 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (A → B)	tpLH tpHL	Figures 3 and 5	—	0.12	ns
3-state output enable time (OE or \overline{OE} → B)	tpZL	Figures 4 and 6	—	6.5	
3-state output disable time (OE or \overline{OE} → B)	tpLZ	Figures 4 and 6	—	10.5	

VL (VCCA) = 2.5 ± 0.2 V, VCCB = 5.0 ± 0.5 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (A → B)	tpLH tpHL	Figures 3 and 5	—	0.12	ns
3-state output enable time (OE or \overline{OE} → B)	tpZL	Figures 4 and 6	—	8.5	
3-state output disable time (OE or \overline{OE} → B)	tpLZ	Figures 4 and 6	—	12.0	

VL (VCCA) = 2.5 ± 0.2 V, VCCB = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (A → B)	tpLH tpHL	Figures 3 and 5	—	0.15	ns
3-state output enable time (OE or \overline{OE} → B)	tpZL	Figures 4 and 6	—	9.5	
3-state output disable time (OE or \overline{OE} → B)	tpLZ	Figures 4 and 6	—	12.0	

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition			Typ.	Unit
			VL (V)	VH (V)		
Control input capacitance	CIN		3.3	3.3	3	pF
Switch input/output capacitance	C _{I/O}	SW = OFF	3.3	3.3	10	pF

DC Test Circuits

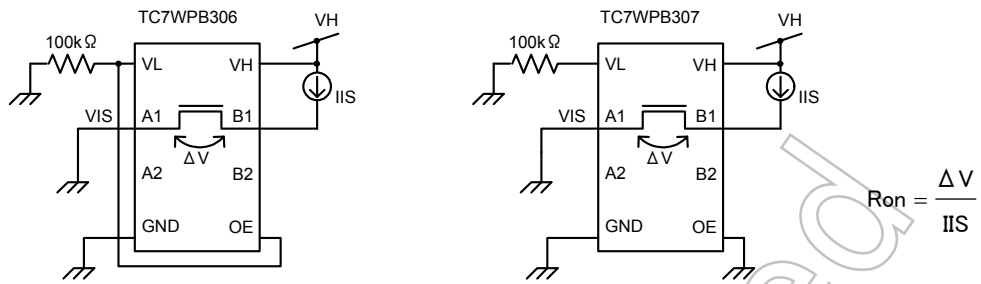


Figure 2 ON-resistance Test Circuits

AC Test Circuits

- tpLH,HL

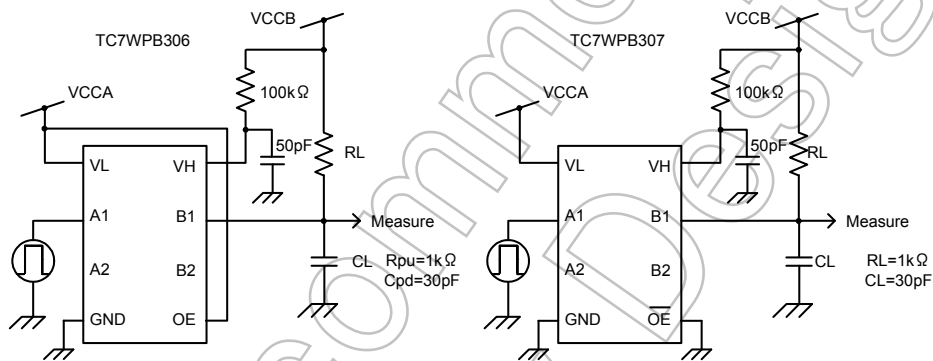


Figure3 tpLH, tpHL Test Circuits

- tpLZ,ZL

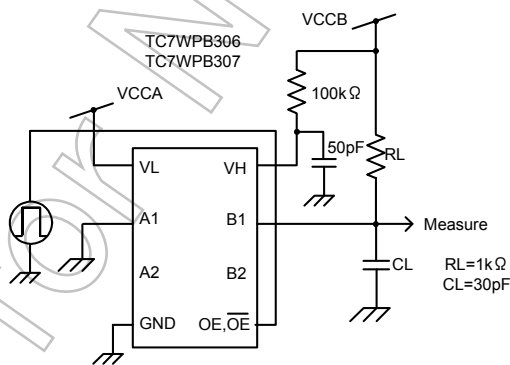


Figure4 tpLZ, tpZL Test Circuits

AC Waveform

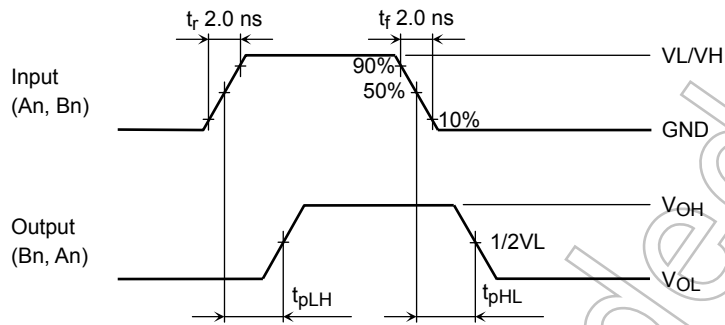


Figure5 tpLH, tpHL

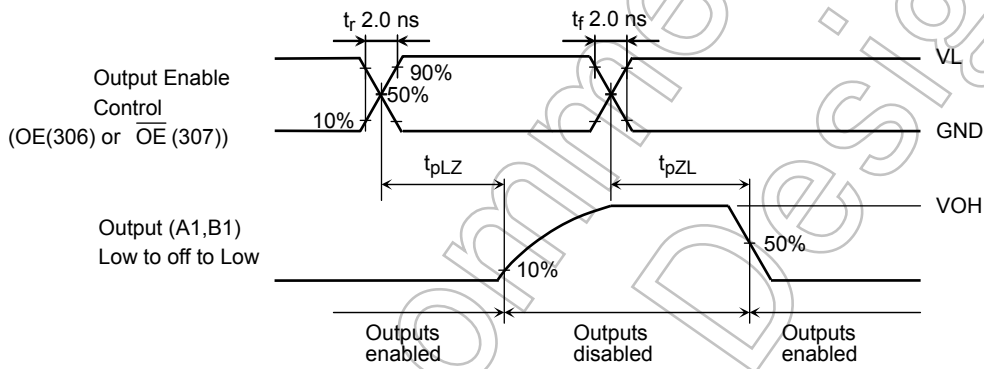


Figure6 tpLZ, tpZL

tpZ Characteristics

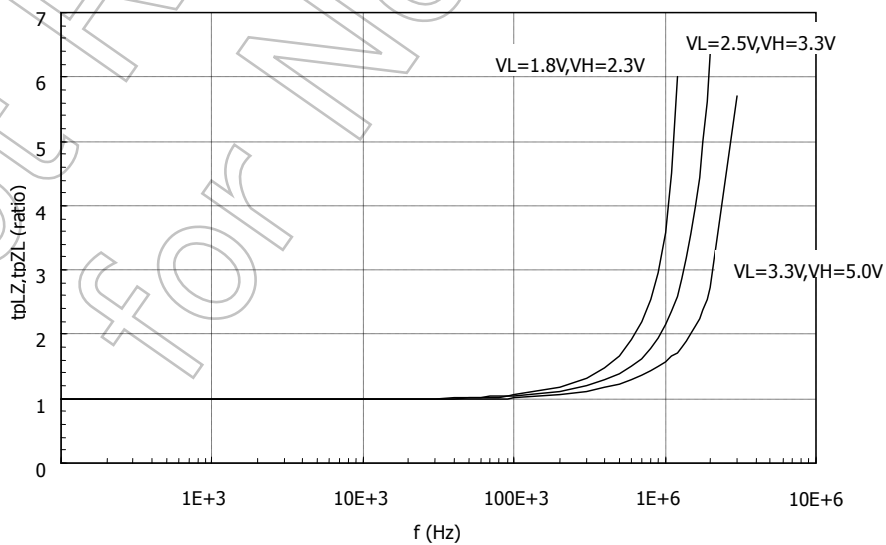


Figure7 tpLZ, tpZL Frequency Characteristic

This figure shows the ratio of delay time for t_{pLZ} and t_{pZL} at the frequency characteristic of OE or /OE when t_{pLZ} and t_{pZL} at the OE or /OE frequency by 10kHz are assumed to be one.

Level Shift Function (Used Pull-up Resistance)

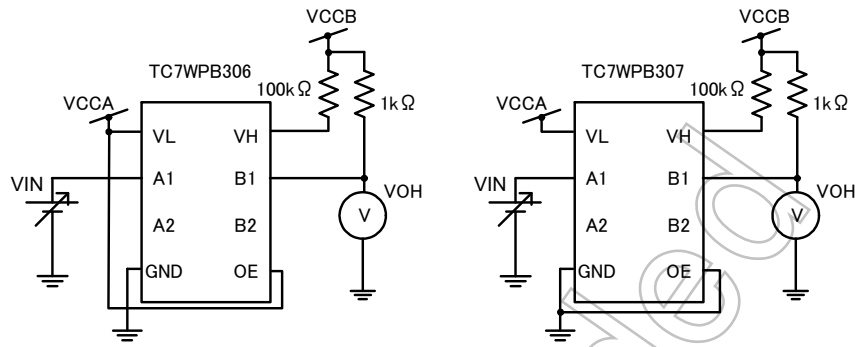


Figure8 Test Circuits

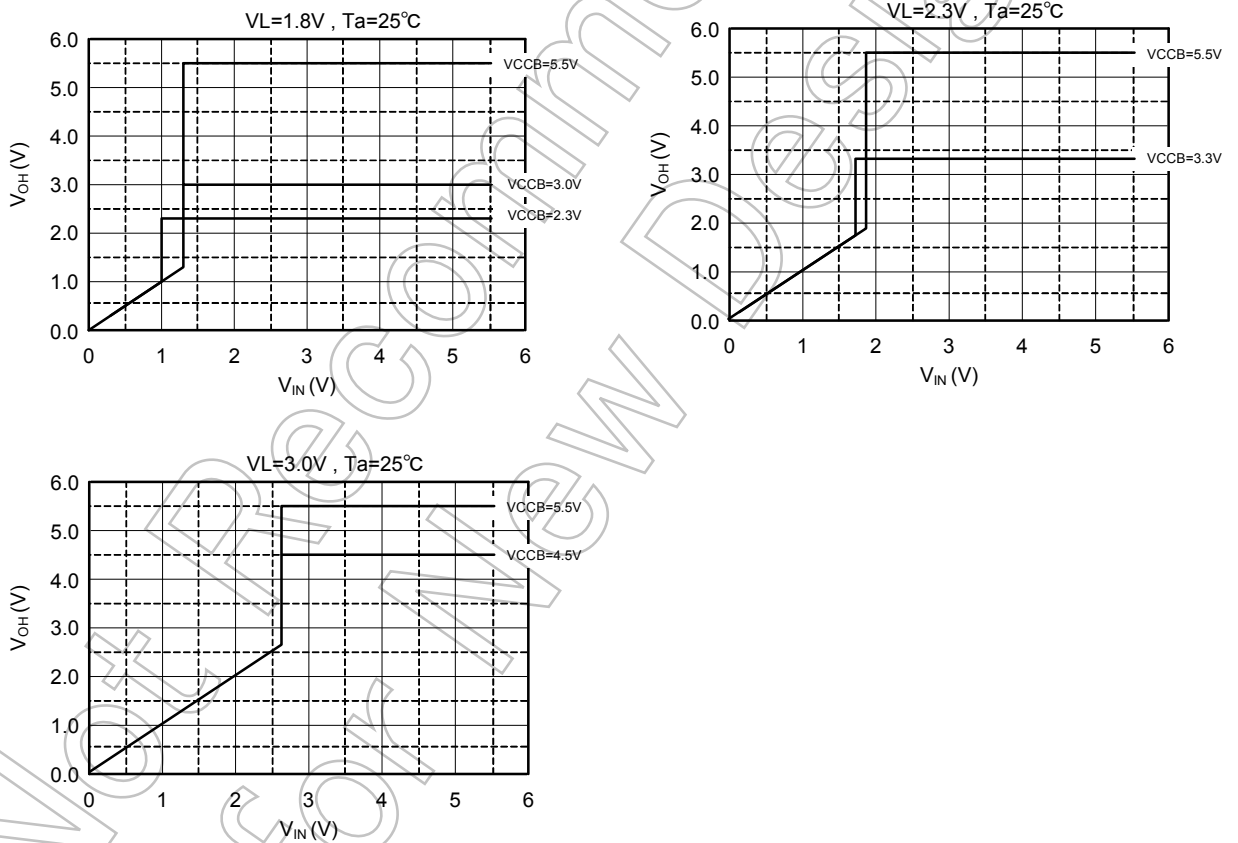


Figure9 Input/Output Characteristics (Typ.)

Level Shift Function (Unused Pull-up Resistance)

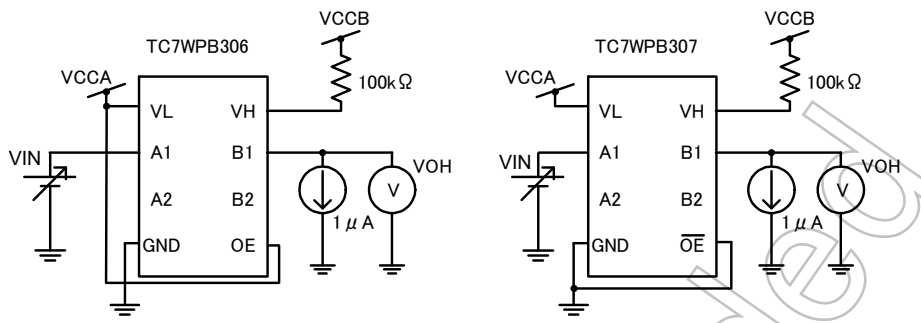


Figure 10 Test Circuits

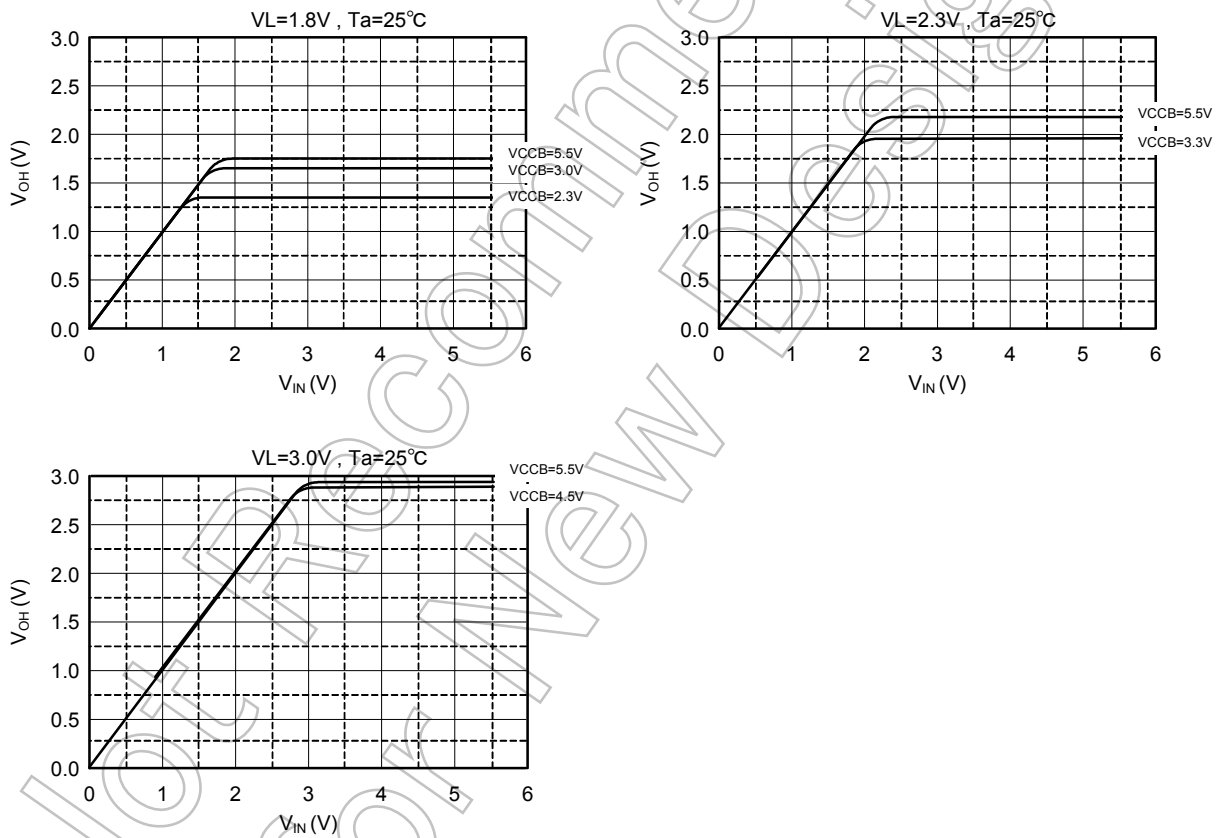
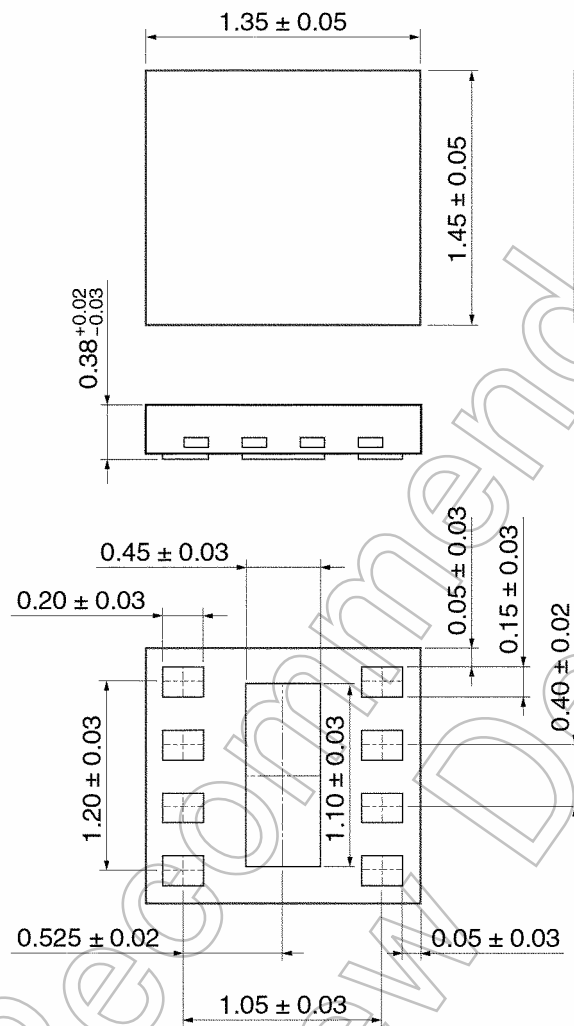


Figure11 Input/Output Characteristics (Typ.)

Package Dimensions

CSON8-P-0.4

Unit: mm



Weight: 0.002 g (typ.)

Not Recommended for New Design

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