1. GENERAL

The TC8835 is a single chip CMOS LSI for voice recording / play-back using the ADM (Adaptive Delta Modulation). It composes a voice recording system with a dynamic RAM for voice memory and an audio circuit including a microphone, speaker, filter, amplifier, etc. as an external circuit.

2. FEATURES

- ☐ DRAMs (Dynamic RAM) are used as a voice data memory up to 2 pieces of 256 kbit, or 2 pieces of 1M.
- ☐ 4 pins for control I / O.($\overline{WR}$, $\overline{RD}$, D0, D1)
- ☐ On manual control, bit rate is fixed at 16Kbps and recording / play-back is capable on one phrase.
- ☐ On CPU control, recording / play-back is capable on 16 phrases at maximum.
- ☐ Block editing can be easily operated on CPU control.
- ☐ 2 kinds of bit rates (22k, 16kbps) are provided on CPU control.
- ☐ 3 types of oscillation circuits is selectable, as below.

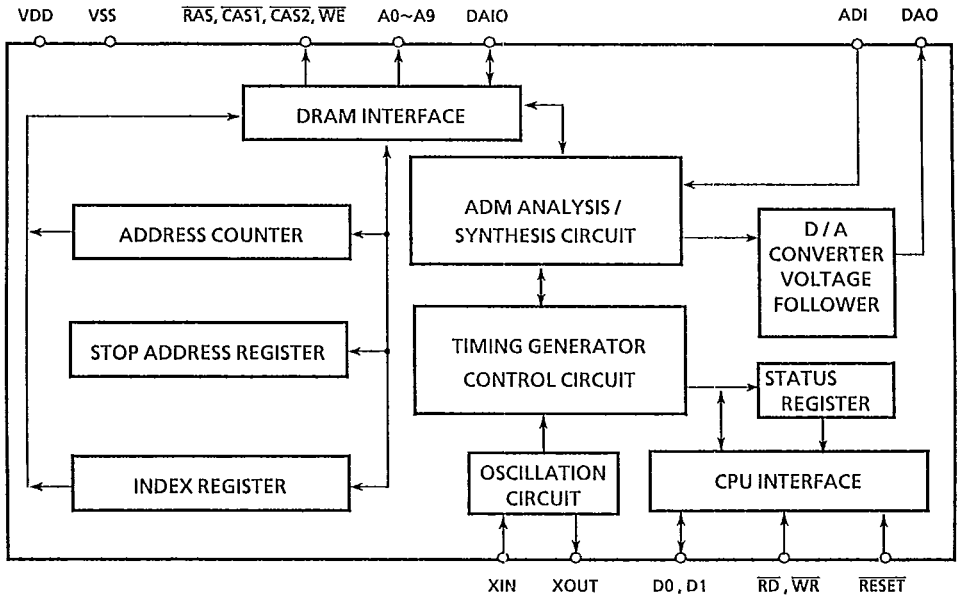
TC8835N / F	Direct 4MHz
TC8835AN / F	Ceramic Oscillation 800kHz
TC8835BN / F	RC oscillation 800kHz

- ☐ The method of refresh for DRAM is $\overline{CAS}$ before $\overline{RAS}$ which is auto refresh method.
- ☐ Single 5V power supply.
- ☐ 28-pin small outline package or 28-pin shrink DIP package.

- ◦ The phrase means the phrase which is recorded or played - back..
- ◦ The bit rate means the number of bits per second to be used.

3. BLOCK DIAGRAM

3.1 TC8835N/F Block Diagram



3.2 Block Diagram Description

(1) ADDRESS COUNTER

The 21-bit counter to indicate address of the external DRAMs.

(2) STOP ADDRESS REGISTER

The 21-bit register to indicate address to stop recording / play-back.

(3) INDEX REGISTER

The register to indicate address of the index area on DRAMs.

(4) STATUS REGISTER

The 2-bit register which shows the status of TC8835. When $\overline{RD}$ terminal is L level on CPU control, TC8835 gives this contents to D0 and D1.

(6) CPU INTERFACE

The interface circuit for the external microprocessor. This circuit has also the chattering circuit in the manual control. This chattering elimination preventing has an effect on D0 and D1 pins.

3.3 Example of Voice Recording System

3.3.1 CPU Control Type

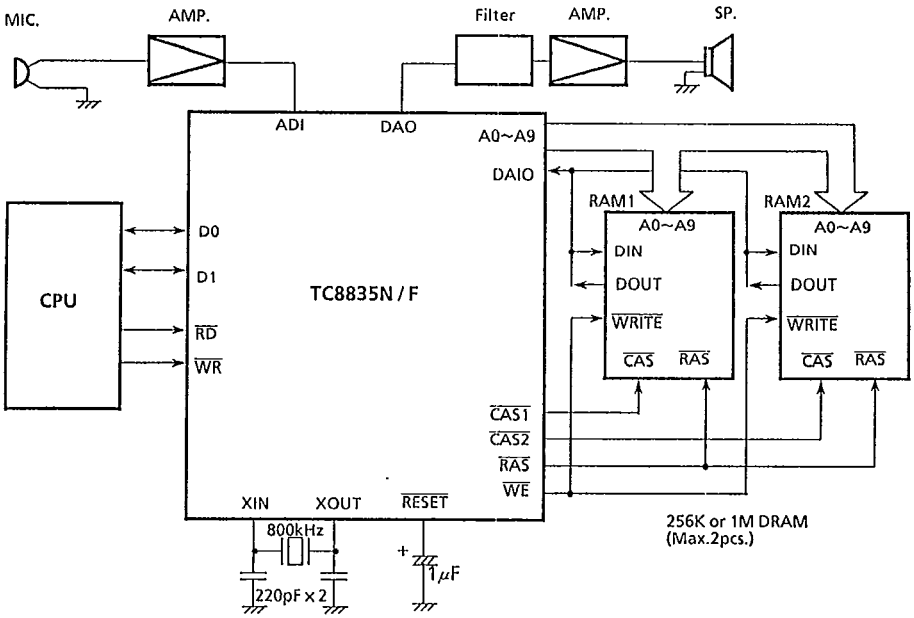


Fig3.1 CPU control type

3.3.2 Manual Control Type

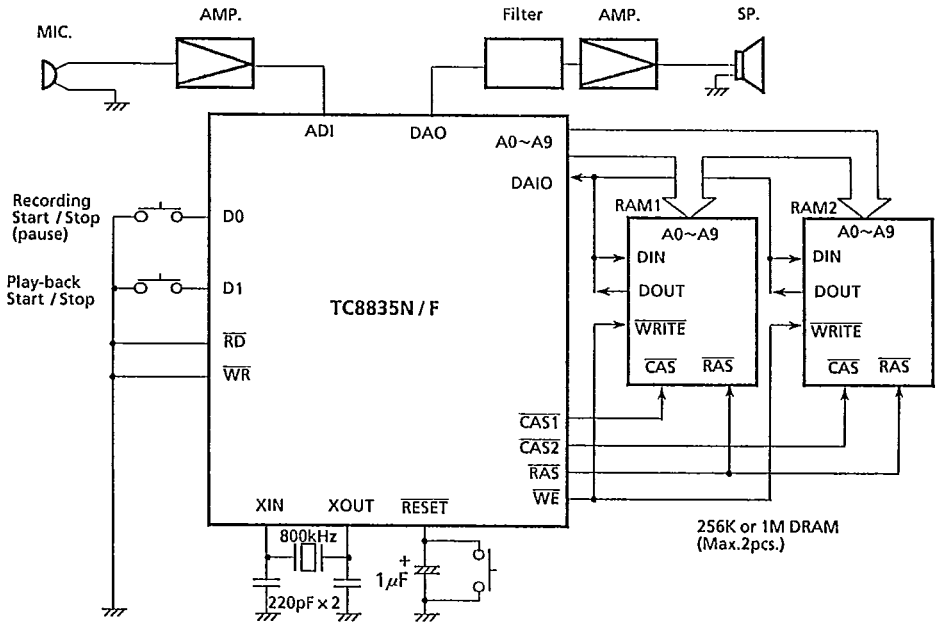
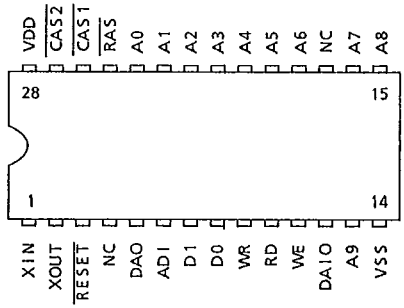


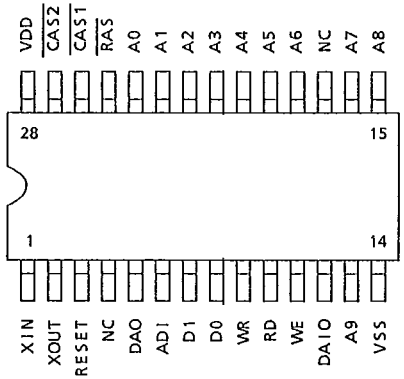
Fig.3.2 Manual control type

4. PIN ASSIGNMENTS

1) SDIP



2) SOP



Pin assignments are the same between SDIP and SOP.

4.1 Pin Functions

name	no.	structure		Functional explanation
		I/O	pull up / down	
XIN XOUT	1 2	In Out	- -	Input and output pins of the oscillator. Mask option for ceramic oscillation (800kHz), RC oscillation (800kHz), and direct clock in (4MHz).
$\overline{\text{RESET}}$	3	In	pull up	Input pin for reset the internal system such as the address counter etc. After reset, the bit rate is set at 16kbps, mode is normal phrase mode, and the capacity of DRAMs is detected.
DAO	5	Out	-	Output pin of the voice synthesis circuit.
ADI	6	In	none	Input pin of the voice analysis circuit. Input voice signal should be biased to VDD / 2.
D1 D0	7 8	I/O	pull up	Input pins for command in CPU control. Recording / play-back start input pin in manual control.
$\overline{\text{WR}}$	9	In	pull up	Write strobe input pin. Making of $\overline{\text{WR}}$ and $\overline{\text{RD}}$ L level places TC8835 manual control.
$\overline{\text{RD}}$	10	In	pull up	Read strobe input pin.
$\overline{\text{WE}}$	11	Out	-	Write strobe output pin for external DRAMs. Connect this pin to $\overline{\text{WRITE}}$ of DRAMs.
DAIO	12	I/O	pull up	Data input / output pin. Connect this pin to both of data input pin of DRAM (DIN) and data output pin (DOUT).
A9	13	I/O	-	Address output and DRAM's capacity definition input pin. Input L level to this pin and memory capacity is defined as 256Kbit.
VSS	14	Power supply	-	Power supply pin to be connected to ground.
A8 A7 A6 A5 A4 A3 A2 A1 A0	15 16 17 19 20 21 22 23 24	I/O	-	Address output pin. Connect to address input pins of DRAMs.
$\overline{\text{RAS}}$	25	Out	none	Row address strobe output pin for DRAMs. Connect this pin to $\overline{\text{RAS}}$ of DRAMs.

name	no.	structure		Functional explanation
		I/O	pull up /down	
$\overline{CAS1}$ $\overline{CAS2}$	26 27	I/O Out	- -	Column address strobe output pins for DRAMs. Connect each pin to $\overline{CAS}$ of each DRAM. In case of 1 pc use of DRAM, connect $\overline{CAS2}$ pin to VDD.
VDD	28	Power supply	-	Power supply pin to be connected to VDD.

5. OPERATIONS AND FUNCTIONS

When composing a voicer recording / play-back system with TC8835, control method is classified into "the CPU control" and "the manual control" using switches, etc.

5.1 CPU Control

In the CPU control, the operation is controlled by 4 kinds of commands and a CPU can read the status of TC8835 by 2bit status register.

(1) CLEAR D1 | 0 | 0 | D0

This command initializes the internal circuit including the address counter and detects the number of DRAMs connected with TC8835. After initializing, TC8835 becomes the waiting state.

(2) OPR D1 | 0 | 1 | D0

With successive 2 bit data, this command is used to start, pause or stop the recording / play-back.

REC START··· ◦ The recording is started, when this command is executed under the waiting state.
◦ The pause is released, when this command is executed during pause.

REC STOP··· ◦ The recording is restarted , when this command is executed during recording.
◦ The play - back is paused, when this command is executed during play - back.

PLAY START··· ◦ The play - back is started, when this command is executed under the waiting state.

PLAY STOP··· ◦ The play - back is stopped, when this command is executed during play - back.
◦ It becomes the waiting state, when this command is executed during pause.

(3) CNDT D1 | 1 | 0 | D0

Specifies bit rate and the phrase mode (normal phrase mode or block phrase mode) with the successive 2 bit data. For more details, please refer to 5.1.10 NORMAL PHRASE MODE and 5.1.11 BLOCK PHRASE MODE.

(4) PHRASE D1 | 1 | 1 | D0

Specifies Phrase No. which is from 0 to 15, by the successive 4 bit data. Under block phrase mode, it is prohibited to specify the phrase number of 14 or 15.

When TC8835 dose not receive the command of REC / PLAY STOP (this means that TC8835 receives REC / PLAY STOP command incorrectly because the addressing is stopped reaching the maximum address of DRAMs, before TC8835 receiving the command.), please specify the phrase number of 0. The phrase command becomes the CLEAR command.

Table.5.1 Command list

command	first data		second data		third data	
	D1	D0	D1	D0	D1	D0
CLEAR	0	0	----			
OPR	0	1	ST1	ST0		
	REC START →		0	0		
	REC STOP →		0	1		
	PLAY START →		1	0		
	PLAY STOP →		1	1		
CNDT	1	0	BLK	BIT	----	
	NORMAL PHRASE MODE / 16kbps→		0	0		
	NORMAL PHRASE MODE / 22kbps→		0	1		
	BLOCK PHRASE MODE / 16kbps→		1	0		
	BLOCK PHRASE MODE / 22kbps→		1	1		
PHRASE	1	1	PH3	PH2	PH1	PH0
	Specify the phrase number by PH3~PH0 (MSB··· PH3, LSB··· PH0)					

5.1.2 Status Register

The status register consists of 2 bits. When the $\overline{RD}$ pin is set to L level at the CPU control, data of the status register is come out to D0, D1 pins and the internal operating status of the TC8835 can be checked. Each flag of the status register is explained in following.

Table 5.2 Status register

pin name	D1	D0
Status register	BUSY	EOS

(1) BUSY flag

When this flag is set to H level, it indicates that the TC8835 is in command processing, address comparator processing, or reset state. Don't give any command from microprocessor, in this status. If the command is given, the internal status may possibly becomes uncertainty.

(2) EOS flag

This flag is set to H level under the recording / play-back waiting state, and reset L level during recording or play-back.

5.1.3 BUSY Flag

Conditions for

When it is detected that the $\overline{WR}$ pin becomes L level in the CPU control, BUSY flag is set to H level. The commands are written to TC8835 when the $\overline{WR}$ pin is made H level. When the process of command is completed, BUSY flag returns to reset L level again.

(2) Address overflow process

When the value of the address counter reaches the value of the stop address resister during recording / play - back or reaches the maximum address of the connected DRAMs during recording, recoding / pay - back is stopped automatically and TC8835 processes the same as the command of REC STOP or PLAY STOP. During this process, the BUSY flag is set H level.

(3) Reset process

When the $\overline{RESET}$ pin becomes L level, BUSY flag becomes set to H level. When the $\overline{RESET}$ pin returns to H level again, the internal state of TC8835 is initialized and after completed, BUSY flag becomes L level.

5.1.4 Flag and Internal States

Table 5.3 shows the internal states and the status register. In this table, "BUSY period" means the maximum period from time when the command is written to time when the BUSY flag becomes L level.

Table 5.3.1 Internal states, status resister, and BUSY period

		before process (Write condition)		Change of status				BUSY period (s)	
				In process		After process			
		EOS	BUSY	EOS	BUSY	EOS	BUSY	22Kbps	16Kbps
RESET processing (including when the power is on.)		*	*	1	1	1	0	432 SYS	
CLEAR command		*	0	1	1	1	0	384 SYS	
in waiting state	CNDT command	1	0	1	1	1	0	144 SYS	192 SYS
	second data (condition set)	1	0	1	1	1	0	144 SYS	192 SYS
	PHRASE command	1	0	1	1	1	0	144 SYS	192 SYS
	second data (MSB of phrase#)	1	0	1	1	1	0	108 SYS	144 SYS
	third data (LSB of phrase#)	1	0	1	1	1	0	216 SYS	288 SYS
	OPR command	1	0	1	1	1	0	144 SYS	192 SYS
	second data (REC START)	1	0	1	1	0	0	936 SYS	1248 SYS
	second data (PLAY START)	1	0	1	1	0	0	1728 SYS	2304 SYS
in recording	OPR command	0	0	0	1	(0	0) note	144 SYS	192 SYS
	second data (REC STOP)	0	0	0	1	1	0	936 SYS	1248 SYS

Table 5.3.2 Internal states, status resister, and BUSY period

		before process (Write condition)		Change of status: In process		Change of status: After process		BUSY period (s)	
		EOS	BUSY	EOS	BUSY	EOS	BUSY	22Kbps	16Kbps
in play - back	OPR command	0	0	0	1	(0	0) note	144 SYS	192 SYS
	second data (REC STOP)	0	0	0	1	0	0	144 SYS	192 SYS
	second data (PLAY STOP)	0	0	1	1	1	0	180 SYS	240 SYS
in pause	OPR command	0	0	0	1	0	0	144 SYS	192 SYS
	second data (REC START)	0	0	0	1	0	0	216 SYS	288 SYS
	second data (PLAY STOP)	0	0	0	1	1	0	180 SYS	240 SYS
in recording	address over	0	0	1	1	1	0	864 SYS	1152 SYS
in recording/ in play -back	automatic stop of play -back (including block recording)	0	0	1	1	1	0	108 SYS	144 SYS

NOTE In case of ceramic or RC oscillation → SYS = 1 / fCLK
In case of direct clock in (4M) → SYS = 5 / fCLK fCLK = frequency of clock (Hz)
If the flag is (1 0), TC8835 has stopped automatically. In this case please execute the phrase command specifying "0" to execute command cancel.

* ···Don't care

2

5.1.5 Status Change in the CPU Control

4 commands control TC8835 in CPU control. The relation between the commands that operate on recording / play - back and each status of recording / play - back is as follows

Table 5.4 Status change table in the CPU control

state \ Command	REC START	REC STOP	PLAY START	PLAY STOP
waiting starts	starts recording	(waiting starts)	starts Play-back	(waiting starts)
in recording	(Stops recording and returns to the waiting state.) (A)	(Stops recording and returns to the waiting state.) (A)	(Stops recording and returns to the waiting state.) (A)	(Stops recording and returns to the waiting state.) (A)
in Play-back	(Returns to the waiting state.) (B)	Paced in the pause state.	(Returns to the waiting state.) (B)	(Returns to the waiting state.) (B)
pause	Releasing the pause and states Play-back	(pause)	(pause)	Releasing the pause and returns to the waiting state.

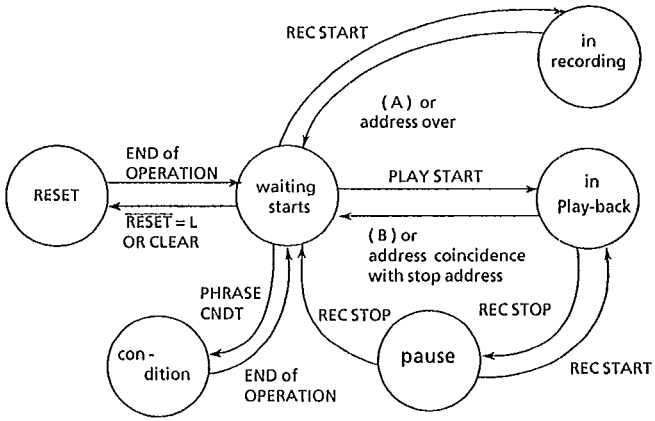


Fig.5.1 Status change at the CPU control

5.1.6 How to write commands

Check the flag of TC8835 by $\overline{RD}$ pulse as shown Fig 5.2. If the condition for writing is satisfied, set the command data to D1 and D0 pins and then write the command by $\overline{WR}$ pulse.

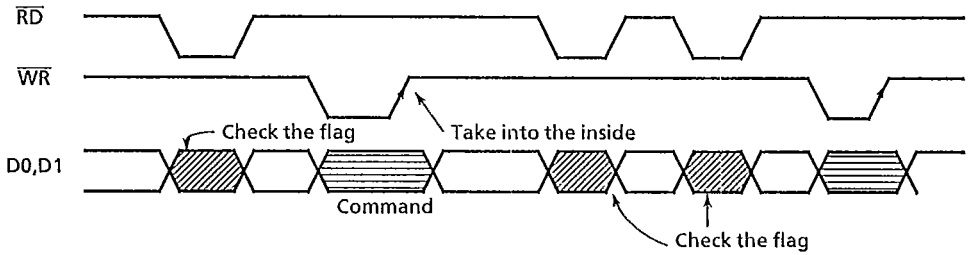


Fig 5.2 How to write command

5.1.7 Example for the Flowchart of Recording

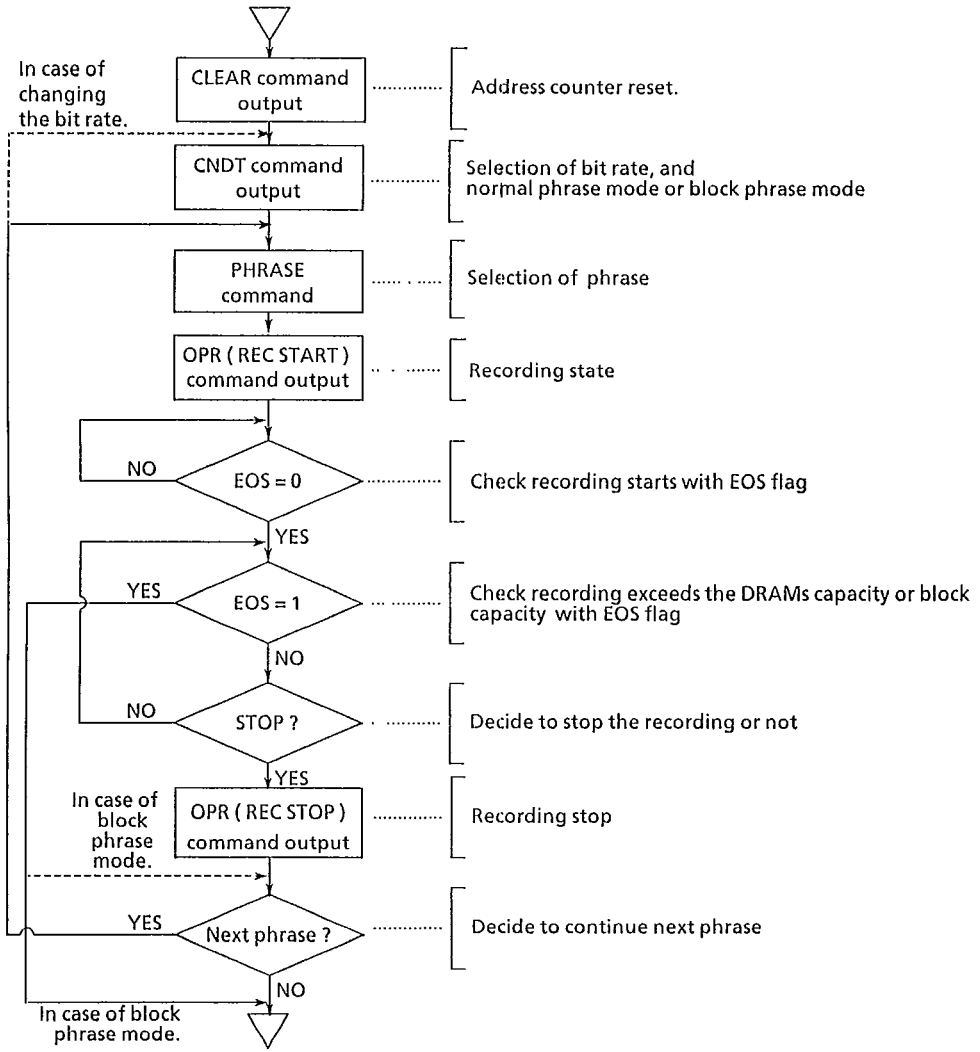


Fig 5.3 Flowchart of recording

5.1.8 Example for the Flowchart of Play - back

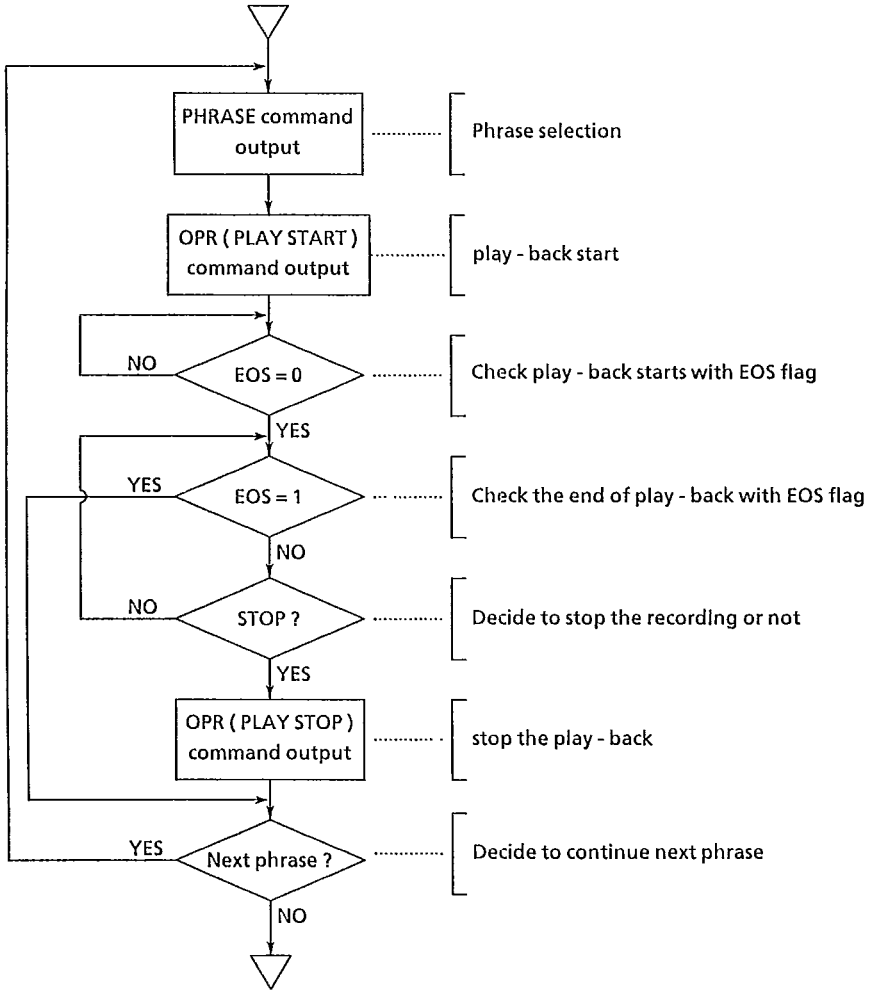


Fig 5.4 Flowchart of play - back

5.1.9 Modes in CPU Control

There are two modes in CPU control. One is " normal phrase mode " that divides the DRAMs by 16 phrases at maximum in free time period. And the other is " block phrase mode " that divides the DRAMs at the fixed address.

During recording, the start address and stop address of specified phrase number are saved to a certain area of DRAM (index area). And during play - back, the start address and stop address of specified phrase number are loaded from index area of DRAM to TC8835.

The configuration of the data are and the index area in DRAMs are as following figure..

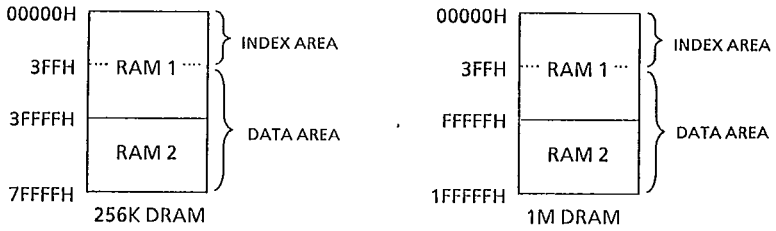


Fig. 5.5 Configuration of index area and data area

5.1.10 Normal Phrase Mode

(1) Recording

In performing the recording newly, reset the TC8835 by the CLEAR command then address counter is preset to 400 (IIEX). And next, bit rate and normal phrase mode are specified by the CNDT command. The conditions set by the CNDT command are fixed as log as it is not changed.

When Phrase No. are specified by the PIIRASE command and next the REC START command is written , then the recording starts. The contents of the address counter (start address) is written into the index area of DRAM before recording. During the recording, the value of the address counter is increased successively.

When REC STOP command is written during recording or the value of the address counter reaches the maximum address of DRAMs connected with TC8835, the recording ends and the contents of the address counter (stop address) are written into the index area. Thereafter the value of the address counter are added with one to prepare for next recording. To perform the recording for another phrase successively, phrase No. is specified by the PIIRASE command and next the REC START command is written again.

In the case that the recording is performed to the maximum capacity of DRAMs, the next phrase can not be recorded successively because of the protection of the data of DRAMs. So the address counter should be initialized by the CLEAR command when the next phrase is necessary to be recorded in this case.

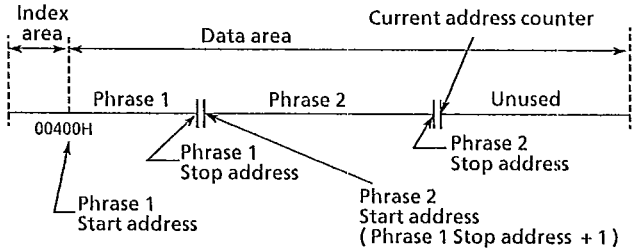


Fig.5.6 In case of recording two phrases

(2) Play-back of Phrase

When any recorded phrase No. is selected and the PLAY START command is given, the start address and stop address in the index area of DRAMs are loaded to TC8835 and then voice to that phrase No. is reproduced. Phrase No. can be designated irrespective of sequence of the recording. Further, it is also possible to stop speaking by giving the PLAY STOP command during play-back. When the play-back ends, the value of the address counter are added with 1. Thereafter, when the PLAY START is given again using the same phrase No., the play-back is performed from the beginning of that phrase. It is also possible to pause during play-back by the REC STOP command.

If the play-back is started by the phrase No. that was not used for the recording, reproduced sound is uncertain. However, it is possible to stop the play-back by giving the PLAY STOP command.

(3) Addition of phrase

First, reproduce the last phrase at the recording completely so that the address counter can indicate the address next to the stop address of the last phrase. Don't reset the TC8835 at this time. The recording is made by designating any unrecorded phrase No. to be added.

(4) Change of phrase contents

To change the contents of phrases that have been once recorded, reproduce a phrase preceding the phrase to be changed to make the address counter indicate the start address of the phrase to be changed. (For example, when phrases have been recorded in order of 5-7-3-6 and the contents of phrase No. 3 is necessary to change, reproduce phrase No. 7 completely.)

Don't reset the TC8835 at this time. When the recording is made by designating phrase No. to be changed successively, the contents of that phrase are changed to new contents.

If the recording time of the new phrase is longer than that of phrase before change, the first part of next phrase may be changed (Fig. 5.7). When the changed phrase is reproduced under this state, the new contents are spoken properly but when it is tried to reproduce next phrase, the play-back is started at the middle of the changed phrase to the end and then sound is reproduced successively from the middle of next phrase. This is phenomenon that is taken place as the start address of next phrase written in the index area remains unchanged from the previous address.

On the contrary, when the recording time of the new phrase is shorter than before change, the best part data of the phrase before change is left. When new phrase is reproduced, it stops at the end properly. Needless to say, next phrase is also properly reproduced. In this case, the part between the stop address of the changed phrase and the start address of next phrase is not used.

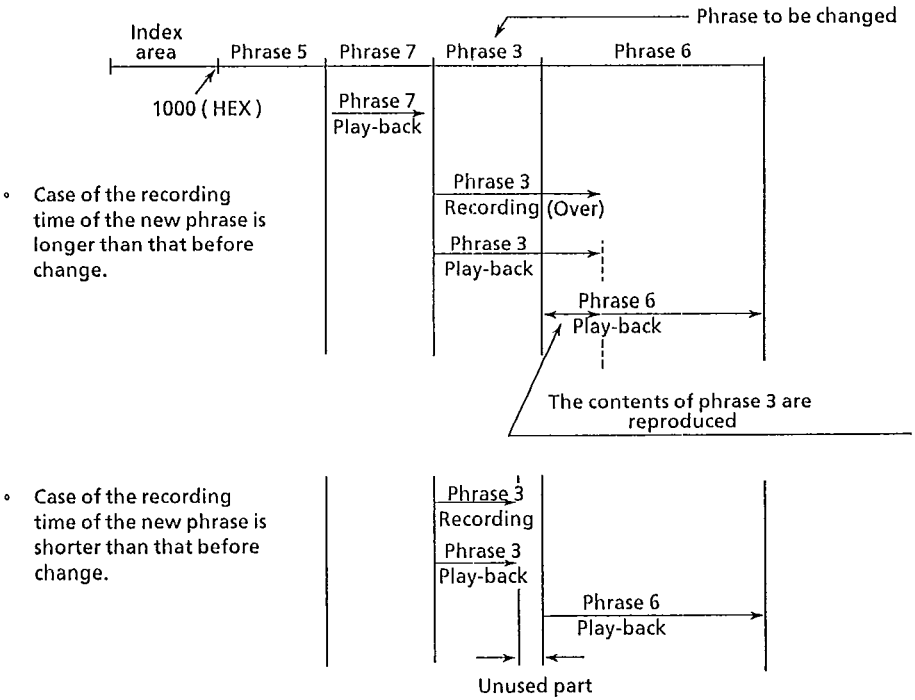


Fig.5.7 Change of phrase contents

5.1.11 Block Phrase Mode

In block phrase mode, the start address and stop address are defined to each phrase No. ,which is called block, in TC8835 and recording / play-back is performed in the block. In each block the recording can be stopped on the way of the block and the play-back is performed to the point that the recording is stopped. In block mode, the change of the contents of phrase is much easier because of the defined phrase area (block).

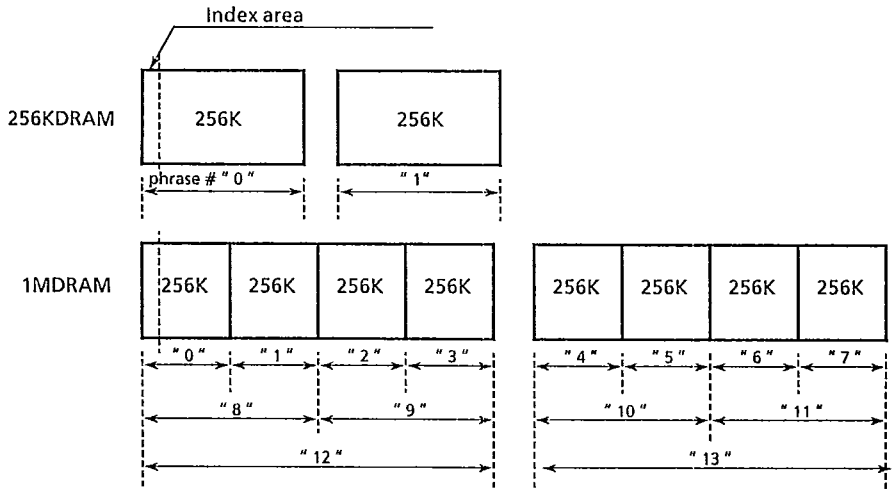


Fig 5.8 Block phrase number and address in DRAMs

(1) recording

When the recording is performed newly, reset TC8835 by the CLEAR command. Then the address counter is set 400 (HEX). And next, set the bit rate and block phrase mode by the CNDT command. The condition is not be changed as long as it is not changed by the CNDT command.

The phrase No. is specified by the PHRASE command, and the phrase No. specify the block.

After writing the REC START command, the value of the address counter is written to the index area of DRAM as the start address, and the recording is started. The value of the address counter increases successively during recording.

The REC STOP command makes recording stop, and writes the value of the address counter to the index area as the stop address. And next, the PHRASE command of another phrase and the REC START command enable TC8835 to record another phrase.

(2) Play - back of phrase

The PHRASE command of the recorded phrase and the following REC START command load the start address and stop address to TC8835, and enable TC8835 to reproduce the speech corresponding to that phrase No. The phrase No. can be designated irrespective of sequence of the recording.

The PLAY STOP command stops the speech on the way of play-back. And next, the PHRASE command of the same phrase and the following REC START command start the play-back from the beginning of the phrase. The REC STOP command during play-back places TC8835 pause state.

If the play-back is started in the phrase No. that was not used for the recording, reproduced sound is uncertain. However, it is possible to stop the play-back by giving the PLAY STOP command.

(3) Change of phrase contents

To change the contents of phrases that have been once recorded, recording of the phrase that is required to change changes the phrase contents. On the contrary to the normal phrase mode, the begging part of the next phrase is not changed because the maximum address is fixed in each phrase.

5.2 Manual Control

Set both of $\overline{WR}$ and $\overline{RD}$ pins to L level, and TC8835 is placed in the manual control mode.

In the manual control, the bit rate is fixed at 16kbps and recording / play-back is performed only on one phrase until reaching the maximum address of DRAMs. AS for the maximum address of DRAMs, refer to 5.1.2 the maximum address of DRAM. Besides reaching the maximum address of DRAMs, the REC STOP or the PLAY STOP command input can also stop the recording / play-back in manual control.

The recording / play-back can be performed using $\overline{RESET}$, D0, and D1 pins. D0 and D1 pins are connected with chattering preventing circuit. The function of D0 and D1 pins is shown as follows.

D0 = recording (start / stop) and play-back pause (pause / release)

Make D0 L level in the waiting state and TC8835 starts recording. And next, set D0 L level again after returning it to H level and TC8835 stops the recording.

Make D0 L level in the play-back and TC8835 becomes pause state. And next, set D0 L level again after returning it to H level and TC8835 releases the pause state and starts the play-back.

D1 = play-back(start / stop)

Make D1 L level in the waiting state and TC8835 starts play-back. And next, set D1 L level again after returning it to H level and TC8835 stops the the play-back.

Make D1 L level in recording and TC8835 stops the recording to become the waiting state.

The timing of manual control is shown as follows.

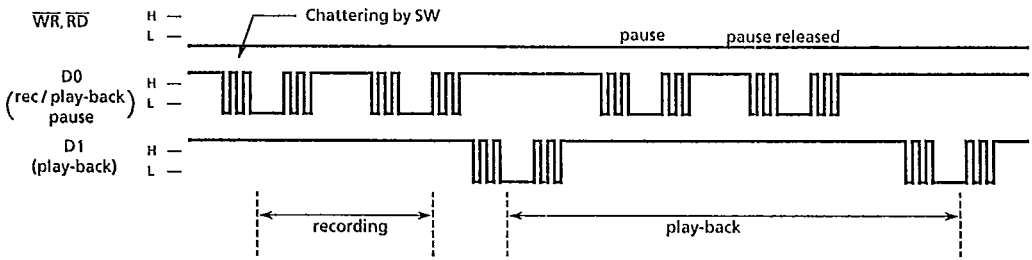


Fig 5.9 Recording / play-back in manual control

In manual control, there is not any monitor pins for states of recording / play-back. So in case of control by a micro processor, it is necessary to control the time of recording / play-back by timer, etc.

5.2.1 Recording

When the recording is performed newly, reset the address counter by $\overline{\text{RESET}}$ input. Then the address counter is set 400 (HEX).

After setting D0 pin L level, the value of the address counter is written to the index area of DRAM as the start address, and the recording is started. The value of the address counter increases successively during recording.

When D0 pin is set L level again or the value of the address counter reaches the maximum address of DRAMs, the recording is stopped.

In the case that the recording is performed to the maximum capacity of DRAMs, the next recording can not be performed successively because of the protection of the data of DRAMs. So the address counter should be initialized by $\overline{\text{RESET}}$ input when new recording is necessary in this case.

5.2.2 Play-back

The L level input to D1 makes TC8835 start play-back after loading the start address and the stop address to TC8835. When D1 pin is set L level again or the value of the address counter reaches the stop address, the play-back is stopped.

Make D0 L level in the play-back and TC8835 becomes pause state. And next, set D0 L level again after returning it to H level, and TC8835 releases the pause state and starts the play-back. Make D1 L level in the pause state and the play-back is ended.

5.2.3 Status Change in the CPU Control

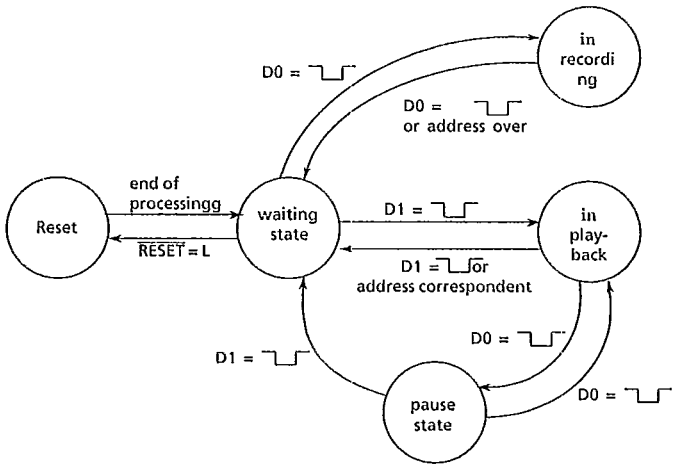
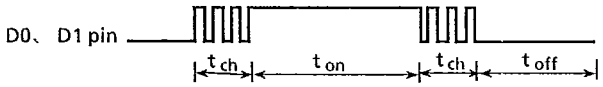


Fig 5.10 Status change in the CPU control

5.2.4 Chattering Preventing Circuit

In the manual control, the chattering preventing circuit is actuated to prevent from malfunction due to noise of the switches connected to the D0 and D1 pins..



t_{on}	t_{off}	t_{ch}
16 ms min.	16ms min.	16 ms min.

Ceramic or RC oscillation → fCLK = 800kHz

4M clock direct in → fCLK = 4MHz

fCLK = oscillating frequency (Hz)

Fig 5.11 Chattering preventing circuit

H level and L level of signals should be applied stably for more than t_{ON} and t_{OFF}. And do not input signal to the other pins during the period of t_{OFF}. If input, malfunction is possibly occurs.

5.3 Control of DRAM

5.3.1 TC8835 's Control of DRAM

The operations of the TC8835 and DRAMs in LABEL INDEX MODE are described in the following.

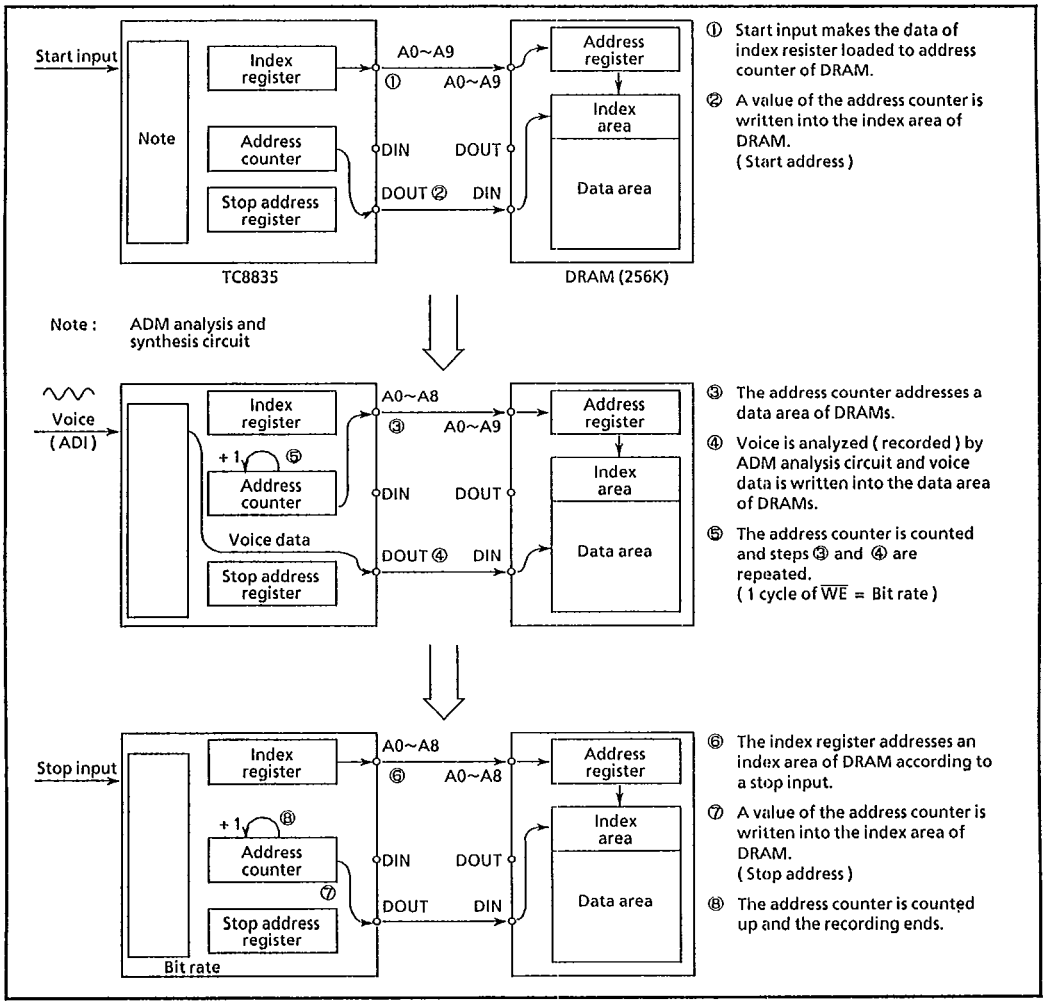


Fig 5.12 Recording

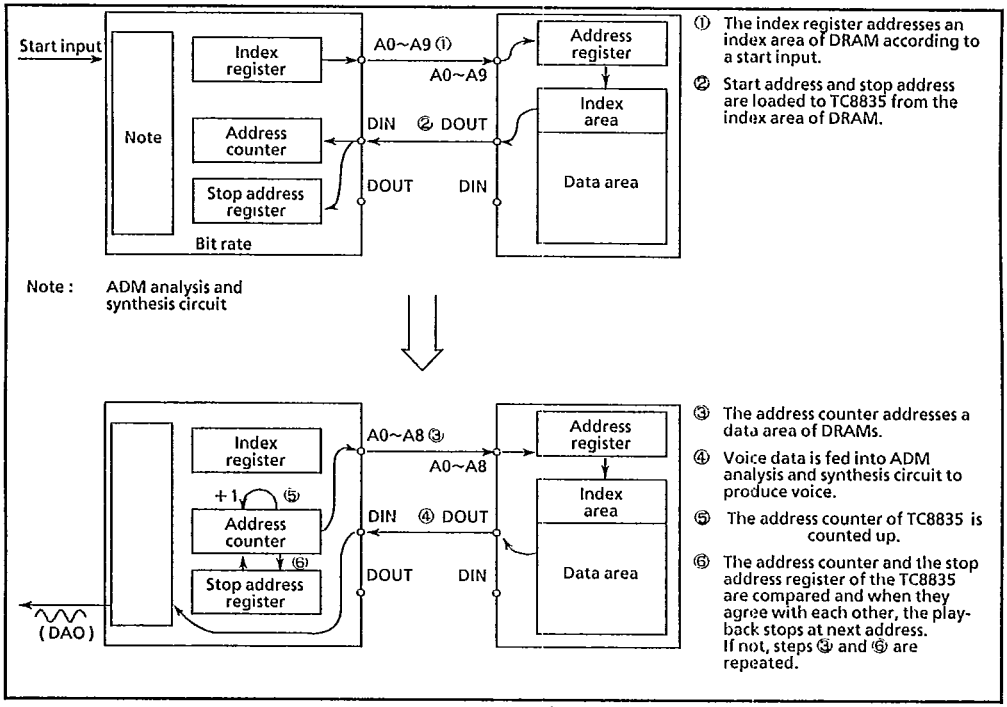


Fig.5.13 Play - back

5.3.2 Address Counter

Row address is the LSB side of address in TC8835.

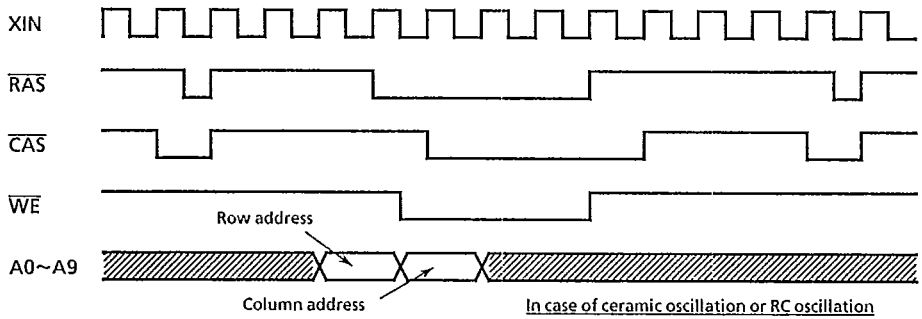


Fig 5.14 Address counter

5.4 System Initialize

5.4.1 The State after System Initialized

When $\overline{\text{RESET}}$ pin is set from L level to H level or the CLEAR command is written, TC8835 is initialized internally. After initializing TC8835 is placed in the following states.

(1) placed in the waiting state after stopping the recording / play-back. However in this case, the index area of DRAMs is not written any data.

(2) Address counter and stop address resister are set to 400 (HEX).

(3) The capacity of DRAM is detected.

After all the above processings are finished, BUSY flag is reset (L level).

5.4.2 The Processing after Powered on

After powered on, the following items become unstable.

(1) Recording and play-back state.

(2) Address counter.

(3) ADM analysis / synthesis circuit.

(4) Other processing circuits such as start and stop processing.

Therefore, to initialize this unstable condition and assure proper operations, apply $\overline{\text{RESET}}$ signal. $\overline{\text{RESET}}$ signal to be given after power on and it's pulse width are shown in Fig. 5.15.

However, if width of t_{DA} after power on is long, the unstable status lasts and causes malfunction (start recording / play-back, etc.) in Fig. 5.15.

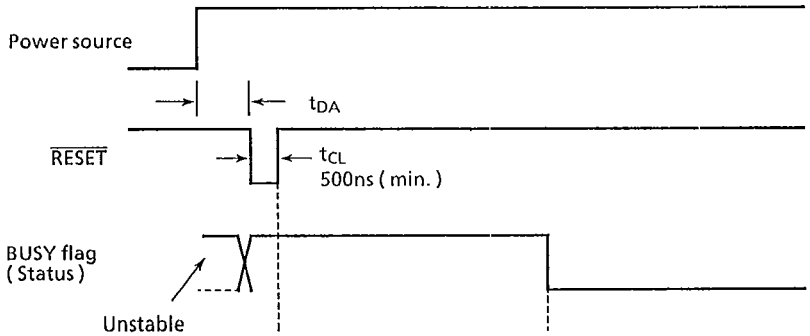


Fig 5.15 $\overline{\text{RESET}}$ pulse width

So, a power on reset circuit is configurated by conned 1μF capacitor to the $\overline{\text{RESET}}$ pin, and the system initialization is possible immediately after power on as illustrated in Fig. 5.16. And $\overline{\text{RESET}}$ input in this case is shown in Fig 5.17.

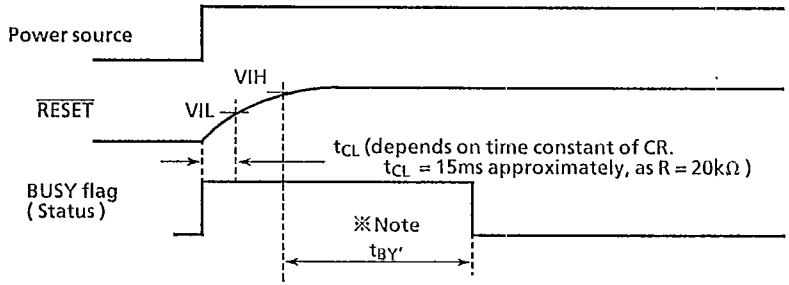


Fig5.17 $\overline{\text{RESET}}$ Input on power on reset

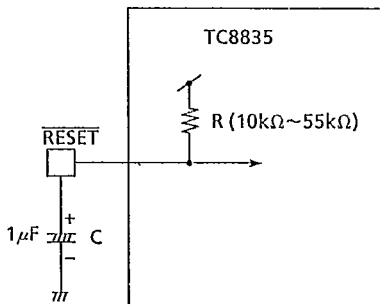
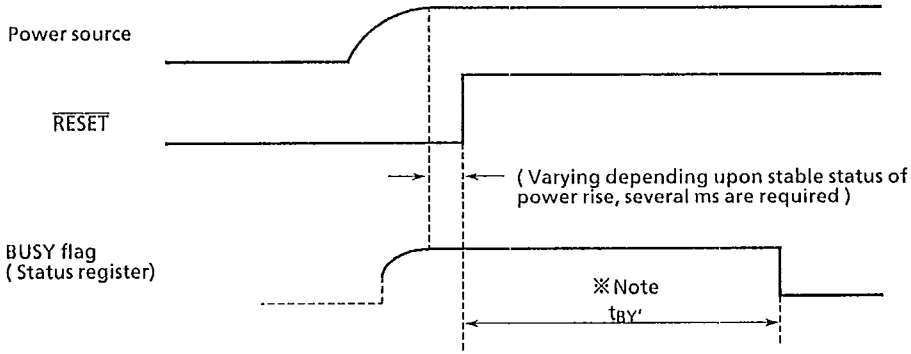


Fig 5.16 Power on reset circuit

However, the power on reset is effective only for a rapid step power rise and when power rise is gentle or power on / off is repeated in short cycle, no system initialization is performed.

Further, if the $\overline{ACL}$ pin can be controlled by a CPU regardless of power on / off at TC8835 side, the system initialization can be made as shown in Fig 5.18



※Note $t_{BY'}$ is a time that is required to stabilize oscillation after power on and it varies depending on an external oscillation device. (Several ms in case of CSB655)

Fig 5.18 System initialization by CPU control

5.5 Connection of DRAMs

The TC8835 uses DRAMs (Dynamic RAMs) for the storage of voice data.

Up to 2 pieces of 256K or 1M bit DRAMs are directly connected to the TC8835. But it is impossible to connect together with different type of DRAMs in capacity

In case of two DRAMs, $\overline{CAS1}$ pin of TC8835 must be connected to the $\overline{CAS}$ pin of 1'st DRAM, the $\overline{CAS2}$ to the $\overline{CAS}$ of 2'nd DRAM. That is, $\overline{CAS1}$ and $\overline{CAS2}$ pin must be connected to the $\overline{CAS}$ pins of each DRAM respectively. Other pins for DRAM connection on TC8835 may be connected in parallel to every DRAM.

In case of use of 256K bit DRAMs, A9 pin must be H level.

5.5.1 DRAM Specification

Available DRAMs are shown in Table 5.5. And TC8835 is designed for normal read cycle,write cycle (early write), and " $\overline{CAS}$ before $\overline{RAS}$ " which is auto refresh cycle.

Table 5.5 Available DRAM (x shoes the package)

Capacity	Available DRAM
1Mbit	TC511000Ax type
	TC511000AxL type (low power version)
256Kbit	TMM41256Ax type

5.5.2 Maximum Address of DRAMs

When the value of the address counter reaches the maximum address of DRAMs during recording in the normal phrase mode of CPU control or in manual control, recording is stopped automatically. In this case, the maximum address is written to the index area of DRAM as the stop address of the phrase. And at this time, the address counter is set 400 (HEX) to be stopped.

The maximum address depends on the capacity and the number of DRAMs

Table 5.6 The external DRAM and the maximum address

the external RAM		the maximum address
256K DRAM	1 pcs	3FFFFH
--------	2 pcs	7FFFFH
1M DRAM	1 pcs	FFFFFH
-------	2 pcs	1FFFFFH

5.5.3 Maximum Recording / Play-back Time

The maximum recording / play-back time depends on the maximum address of DRAMs, the oscillating frequency and the bit rate. The maximum recording / play-back time when the oscillating frequency is 800kHz at ceramic or RC oscillation and the bit rate is 16kbps is shown in Table 5.7. And the method to calculate the maximum recording / play-back time is as follows.

Table 5.7 Time of recording / play-back

the external RAM		time of recording / play-back
256K DRAM	1 pcs	16 s approx.
-------	2 pcs	32 s approx.
1M DRAM	1 pcs	64 s approx.
-------	2 pcs	128 s approx.

(1) In case that the mask option is ceramic oscillation or RC oscillation

○ 22kbps → total capacity of DRAM (bit)×36÷oscillating frequency (Hz)

○ 16kbps → total capacity of DRAM (bit)×48÷oscillating frequency (Hz)

(2) In case that the mask option is 4MHz clock direct in.

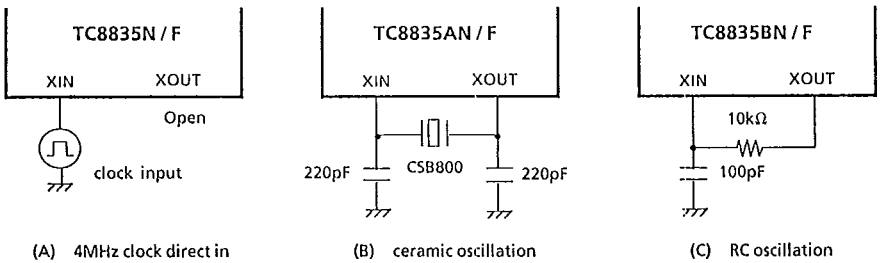
○ 22kbps → total capacity of DRAM (bit)×180÷oscillating frequency (Hz)

○ 16kbps → total capacity of DRAM (bit)×240÷oscillating frequency (Hz)

5.6 Oscillating Circuit

TC8835 has three types of oscillating circuit. According to surrounding system configuration it can be selected by specifying the following product name. The pin connections in every option are shown in Fig 5.19.

TC8835N / F ····· 4MHz clock direct in
TC8835AN / F ····· 800KHz in ceramic oscillation
TC8835BN / F ····· 800KHz in RC oscillation



(A) 4MHz clock direct in (B) ceramic oscillation (C) RC oscillation

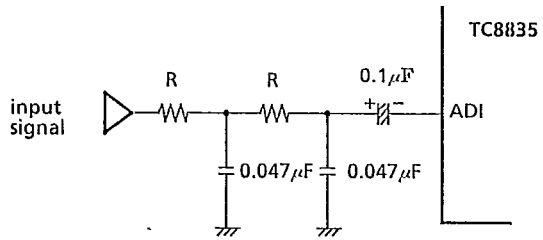
Fig 5.19 Oscillation circuit

5.7 Analog Circuit

The TC8835 composes a voice recording / play-back system with a microphone , an audio amplifier and a filter circuit.

5.7.1 The ADI Pin

The voice signal must be biased to VDD / 2. The example of the filter connected with ADI pin is shown in Fig 5.20. The filter in voice input circuit reject the useless frequency in recording and helps play-back to reproduce clearer voice.



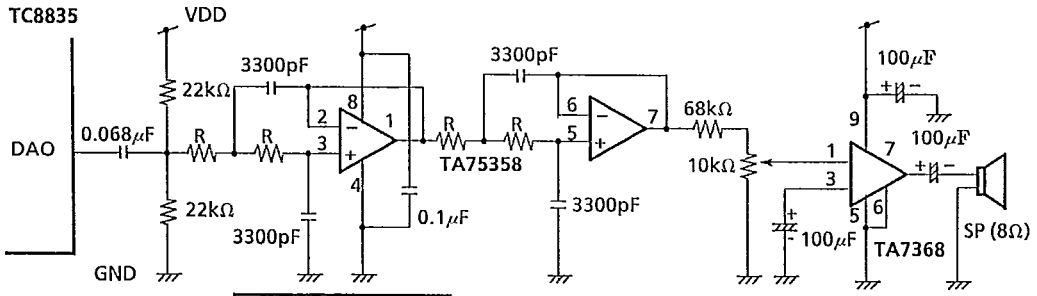
Bit Rate	R
32kbps	1.2kΩ
16kbps	10kΩ

Adjust the resistance and the capacity to improve the voice quality.

Fig 5.20 Example of Connecting Filter Circuit.

5.7.2 The DAO Pin

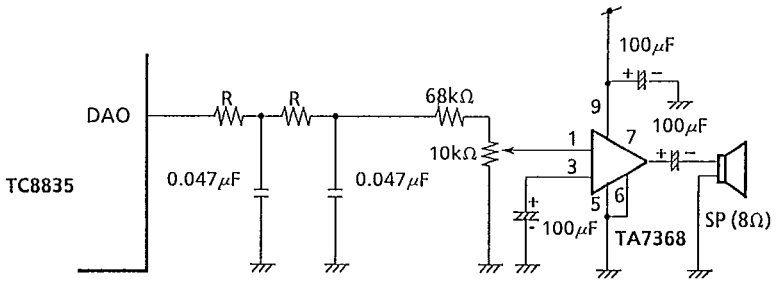
The example of connection of DAO pin with a filter and a speaker amplifier are shown in Fig 5.21 and Fig 5.22.



Bit Rate	R
32kbps	15kΩ
16kbps	18kΩ

Adjust the resistance to improve the voice quality.

Fig 5.21 Example of connecting audio circuit. (active filter)



Bit rate	R
22kbps	7.5kΩ
16kbps	10kΩ

Adjust the resistance to improve the voice quality.

Fig 5.22 Example of connecting audio circuit (passive filter)

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	−0.3 ~ 6.0	V
V_{IN}	Input voltage	−0.3 ~ V_{DD} + 0.3	V
V_{OUT}	Output voltage	−0.3 ~ V_{DD} + 0.3	V
T_{STG}	Storage temperature	−55 ~ 125	°C

6.2 Recommended Operating Conditions

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	4.5 ~ 5.5	V
V_{IN}	Input voltage	0 ~ V_{DD}	V
V_{OUT}	Output voltage	0 ~ V_{DD}	V
T_{OPR}	Operating temperature	−10 ~ 70	°C
f_{CLK1}	Operating frequency 1 (Ceramic/RC Oscillation)	780 ~ 1200	kHz
f_{CLK2}	Operating frequency 2 (4M clock input)	3.9 ~ 6.0	MHz

6.3 DC Characteristics (V_{DD} = 5V ± 10%, Ta = 25°C)

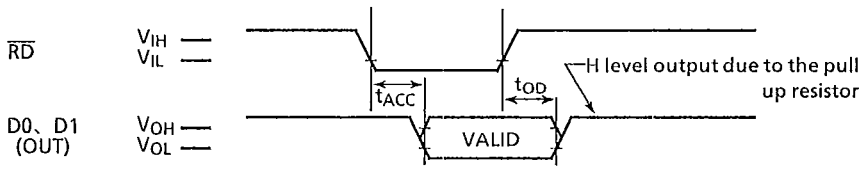
SYMBOL	ITEM	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input current (D0,D1,$\overline{WR}$,$\overline{RD}$ / $\overline{RESET}$、DAIO)	V_{IN} = 0V	100	300	550	μA
I_{ILK}	Input leakage current	V_{IN} = 0~V_{DD}、CPUM = H	–	–	10	
V_{IH1}	Input high voltage 1	DAIO、D0、D1、$\overline{WR}$、$\overline{RD}$	2.4	–	–	
V_{IH2}	Input high voltage 2	Except above	4.1	–	–	
V_{IL1}	Input low voltage 1	DAIO、D0、D1、$\overline{WR}$、$\overline{RD}$	–	–	0.8	V
V_{IL2}	Input low voltage 2	Except above	–	–	0.4	
I_{OH}	Output high current	V_{OUT} = 2.4 V	0.5	–	–	
I_{OL}	Output low current	V_{OUT} = 0.8 V	0.5	–	–	mA
I_{DD}	Supply current	Under no signal (V_{DD}) I_{OUT} = 0 mA	–	2.0	3.0	

NOTE. Values above are in VDD = 5.0V, Ta = 25°C. Max and min values are defined as absolute value.
In the supply current, clock frequency is 655kHz on ceramic or RC oscillation and 4MHz in clock direct in.

6.4 AC Characteristics (V_{DD} = 5V ± 10%, Ta = 25°C, f_{CLK} = 800kHz, CL = 50pF)

6.4.1 Data Read (Read Status Register)

SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{ACC}	Read access time	—	—	150	ns
t_{OD}	Output disable time	—	—	100	

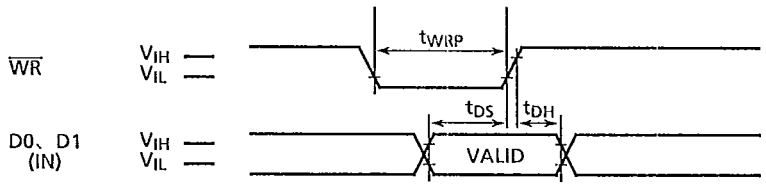


Input level
- V_{IH} = 2.6V
- V_{IL} = 0.6V

Comparison level
- V_{IH} = 2.4V
- V_{IL} = 0.8V
- V_{OH} = 2.4V
- V_{OL} = 0.8V

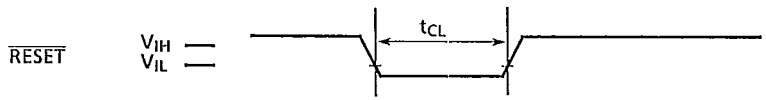
6.4.2 Data Write (Write of Command)

SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{DS}	Data set up time	100	—	—	ns
t_{DH}	Data hold time	150	—	—	
t_{WRP}	$\overline{WR}$ pulse width	150	—	—	



6.4.3 $\overline{RESET}$ Pulse Width

SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{CL}	$\overline{RESET}$ pulse width	500	—	—	ns



6.5 Characteristics of Analog Circuit

6.5.1 Audio In

SYMBOL	ITEM	PIN NAME	CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	ADI	–	–	1.2	1.6	V_{P-P}
R_{IN}	Input impedance	ADI	–	–	50	–	kΩ

6.5.2 Audio Out

SYMBOL	ITEM	PIN NAME	CONDITION	MIN	TYP	MAX	UNIT
R_{OUT}	Output impedance	DAO	–	–	5	–	kΩ

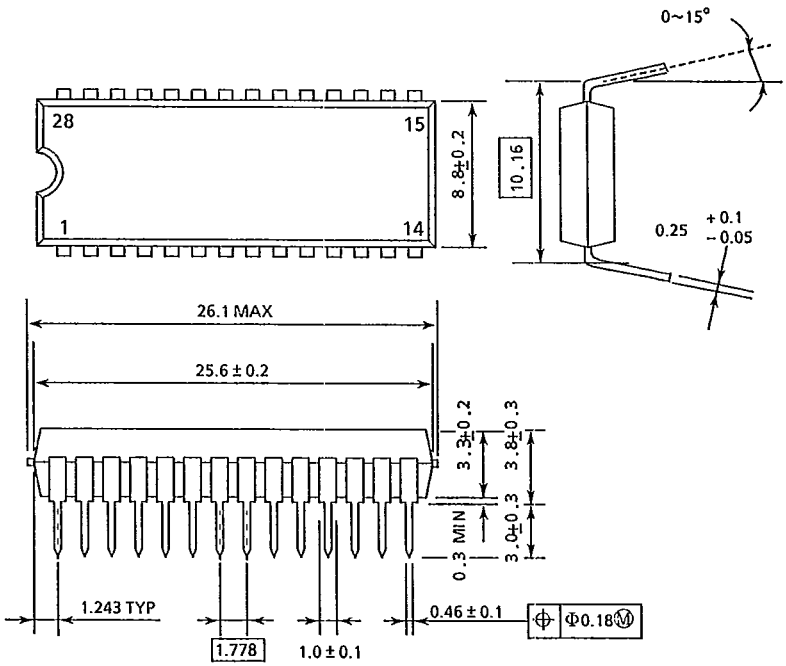
NOTE. : Values of input voltage range are measured as signals biased to 1/2VDD.

7. OUTLINE DRAWINGS

(1) 28 pin Shrink Dual In-Line Package (SDIP28-P-400)

TC8835N
TC8835AN
TC8835BN

unit : mm

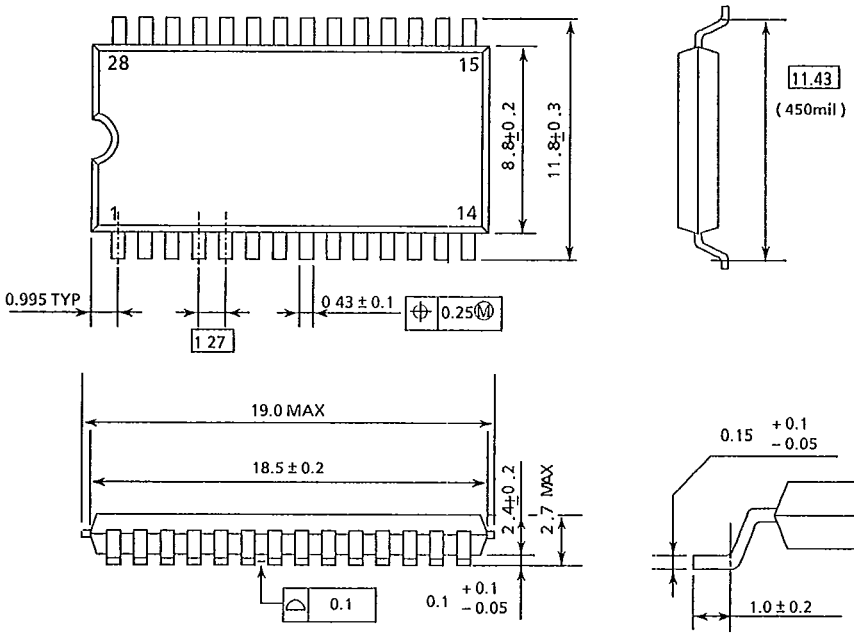


NOTE . Tolerance of lead position : Φ0.18Ⓜ ows that the leads exist in all circles with a radius of {(0.46 + 0.1) + 0.18}/2 mm against the center position of lead (geometrical position).

(2) 28 pin Small outline Package (SOP28-P-450)

TC8835F
TC8835AF
TC8835BF

unit : mm



NOTE . Tolerance of lead position : ⌖ 0.25 Ⓜ shows that the lead flat positions exist in all range of $\{(0.43 + 0.1) + 0.5\}/2$ mm against the center position of lead (geometrical position).

Lead coplanarity : ⌓ 0.1 shows the uniformity of bottom of leads, Maximum value is 0.1.

8. APPLICATION CIRCUIT

Manual Control Type