1. GENERAL

The speaker dependent isolated word recognition device set consists of TC8861F, TC8865F-01 and 64kbit static RAM. The device set contains the whole circuits and functions necessary to recognize voices, and is applied to mobile instruments easily. The device set operates with commands given by a host computer.

2. FEATURES

- ☐ Reference pattern generation* with Differential Filter Method**. Three utterances per word required.
- ☐ Pattern matching with Multiple Similarity Method***.
- ☐ Multiple word boundary candidates are detected, and the device set uses these candidates to avoid miss detection.
- ☐ The recognition device set makes two reference patterns for each word. One is for lower noise environment and the other is for higher noise environment.
- ☐ Configuration: TC8861F, TC8865F-01 and 64kbit static RAM.
- ☐ Recognition rate: 93%
  (20 place names, 5 males and 1 female voice, environmental noise level : 45dBA in registration mode, 70dBA in test mode.)
- ☐ Vocabulary numbers: Maximum 20.
- ☐ Response time: 0.3~1 seconds.
  (Defined as the time length from the utterance end point to the time point of result return to the host computer.)
- ☐ Input voice time length allowed: 0.12~1.6 seconds.
- ☐ Recommended distance between microphone and mouth is 5 through 15 centimeters and the distance more than 15 centimeters reduces system performance.
- ☐ Signal to Noise ratio (S/N) at the microphone location needs over 15dB.
- ☐ Reference pattern bank setting: Every reference pattern can be, if necessary, allocated to one of 8 banks so that the device set executes pattern matching with vocabularies in the designated bank.

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☐ Rejection:

On registration: If three utterances for a word shows characteristic differences among them, the device set rejects these three utterances and then requires another three for the same word again.

On recognition: If a voice to be recognized presents low similarity to all the vocabularies registered, the device set rejects input voice and requests another input voice.

☐ Directly connectable to a voice input microphone.

☐ Power saving mode available.

☐ +5 single power supply (Caution : The separate second power supply is recommended to be employed to TC8861F in order to improve the recognition rate.)

* Reference patterns must be readily generated on 64kbit static RAM through registration process requiring users to store vocabularies by their own voices. These patterns are examined to choose the most possible vocabulary candidate when voice to be recognized enters the device set.

** The method uniquely developed by Toshiba.

*** The method jointly developed by the Agency of Industrial Science & Technology of MITI in Japanese Government, and Toshiba. The device set adopts the Patent "Multiple Similarity Method" (Japanese Patent No.739890) under license of the Japanese Industrial Technology Association. Details are to be referred to references (1), (2).

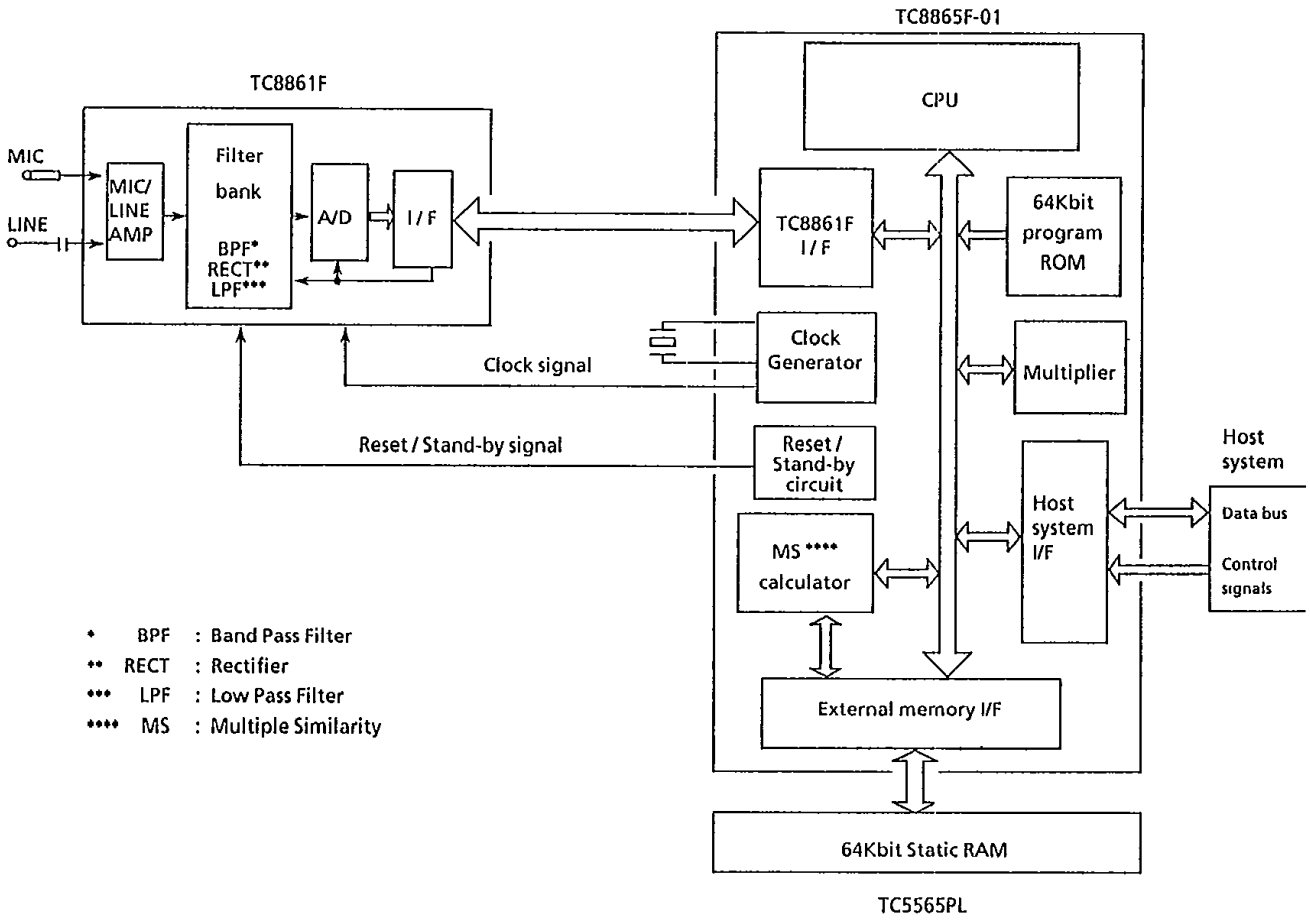
References

(1) Y.Takebayashi, et al., "Telephone Speech Recognition Using a Hybrid Method", IEEE 7th International Conference on Pattern Recognition Proc., pp.1232-1235, 1984.

(2) H.Sekiguchi, et al., "A Three-Chip LSI System for Speaker Independent Isolated Word Recognition by Multiple Similarity Method", IEEE ICCE Dig. of Tech. Papers pp.240-241, 1987.

3. BLOCK DIAGRAM AND SYSTEM CONFIGURATION

3.1 TC8861F/TC8865F-01 Block Diagram



3.2 Description of Block Diagram

3.2.1 TC8861F (Analog Processor)

(1) MIC / LINE AMP

Two types of amplifiers respectively for a microphone input or for an audio line input. A microphone can connect with MIC AMP directly.

(2) Filter bank

Built-in 7 channel band-pass filters.

(3) A / D

Built-in analog-to-digital convertor

(4) I/F

Interface with TC8865F-01.

3.2.2 TC8865F-01 (Digital Processor)

(1) CPU

Built-in central processing unit with system architecture compatible with TMPZ84C00A

(2) TC8861F I/F

Interface with TC8861F.

(3) 64kbit program ROM

This ROM contains the speaker dependent word recognition program codes.

(4) Multiplier

Multiplier speeds up registration process, used by CPU.

(5) MS calculator

This block calculates the similarity between the input voice data and reference patterns for each words.

(6) External memory I/F

Interface for a external RAM.

(7) Host system I/F

Interface for a host system.

(8) Reset/Stand-by circuit

This block makes system reset and stand-by signal.

(9) Clock Generator

Built-in oscillation circuit for ceramic resonator. This block makes 8MHz system clock.

3.2.3 64Kbit Static RAM

This memory stores scratchpad data and reference patterns.

3.3 System Configuration

The recognition device set is comprised of 3 chips. They are TC8861F analog processor, TC8865F-01 digital processor and 64kbit CMOS static RAM.

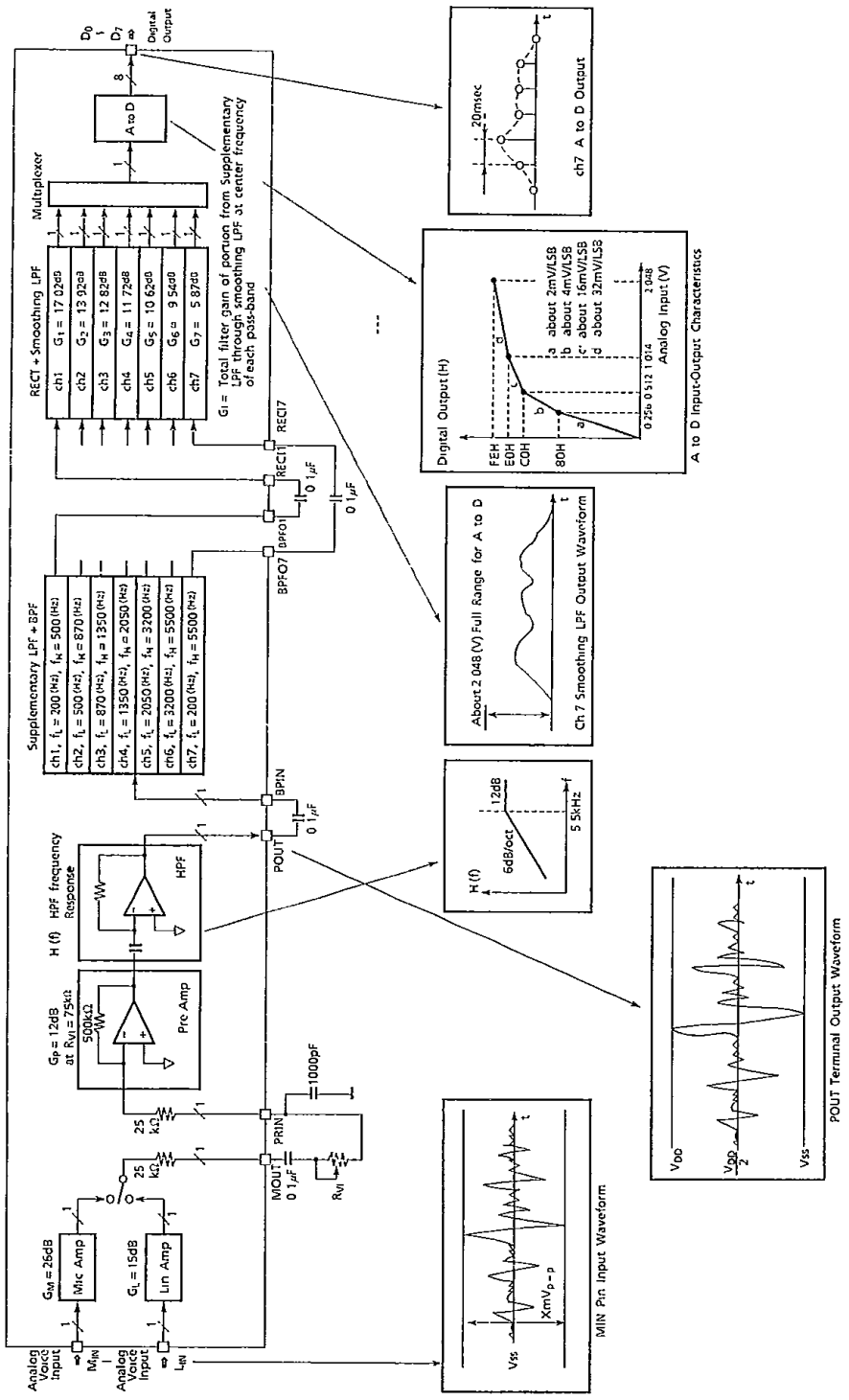
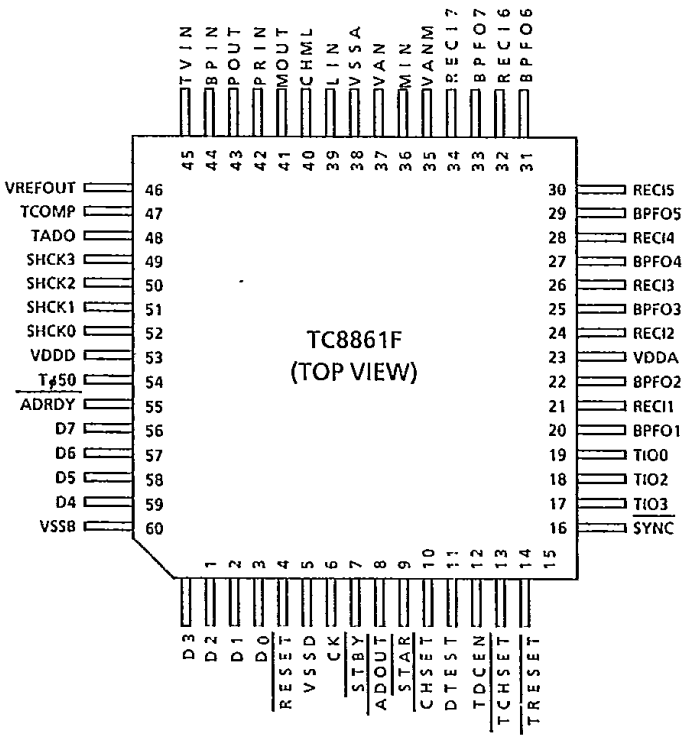


Fig. 5.38 TC8861F Block Diagram

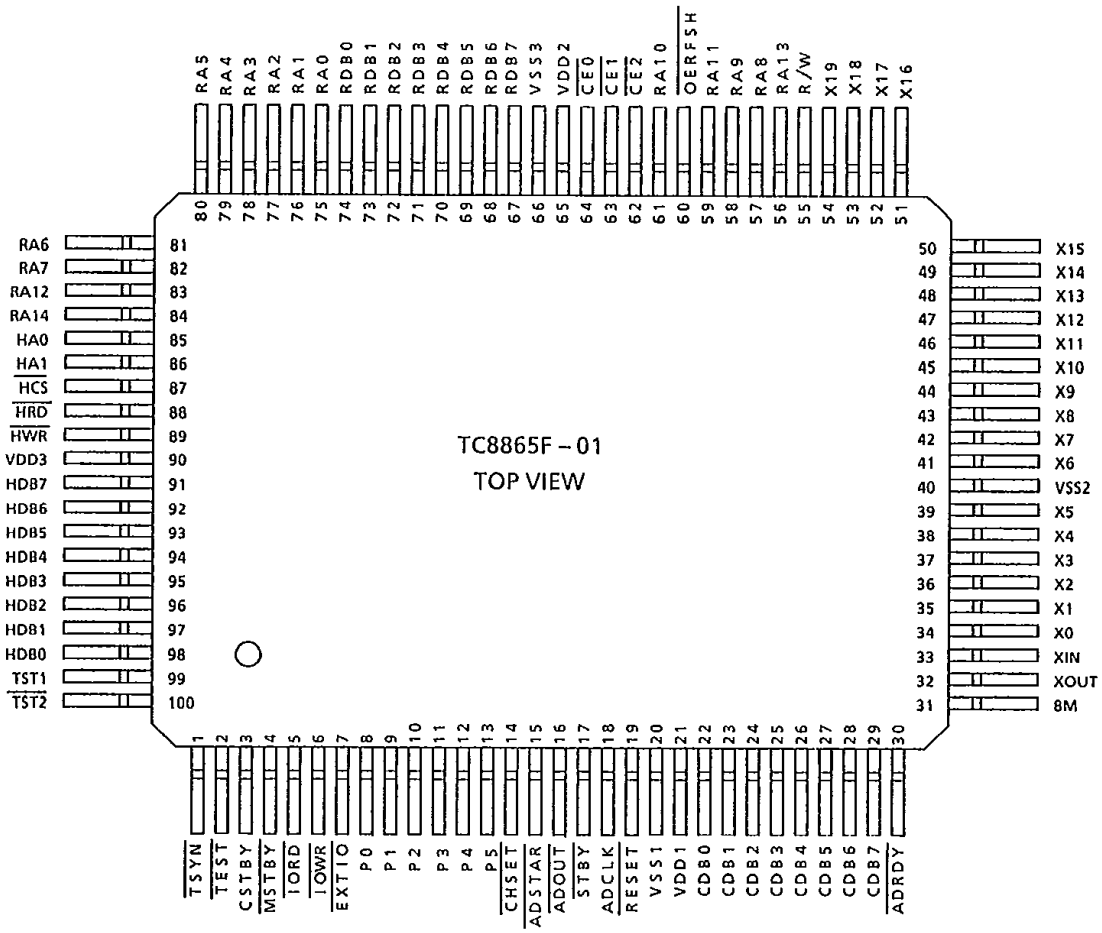
4. PIN ASSIGNMENTS

4.1 Pin Assignments

4.1.1 TC8861F



4.1.2 TC8865F-01



4.2 Pin Descriptions

4.2.1 TC8861F

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
D0	4	I/O, 3-State	System controller data bus	*Hz
D1	3	I/O, 3-State	System controller data bus	*Hz
D2	2	I/O, 3-State	System controller data bus	*Hz
D3	1	I/O, 3-State	System controller data bus	*Hz
D4	59	I/O, 3-State	System controller data bus	*Hz
D5	58	I/O, 3-State	System controller data bus	*Hz
D6	57	I/O, 3-State	System controller data bus	*Hz
D7	56	I/O, 3-State	System controller data bus	*Hz
$\overline{CHSET}$	11	Input	Control signal from TC8865F-01	-
$\overline{ADOUT}$	9	Input	Control signal from TC8865F-01	-
$\overline{STAR}$	10	Input	Control signal from TC8865F-01	-
CK	7	Input	Clock input	-
$\overline{RESET}$	5	Input	Reset input	-
$\overline{STBY}$	8	Input	Stand-by input	-
$\overline{ADRDY}$	55	Output	TC8861F A/D operational status	H
MIN	36	Input	Microphone input	-
LIN	39	Input	Line input	-
CHML	40	Input	Analog input change-over signal	-
MOUT	41	Output	Output of MIC Amplifier or LIN Amplifier	*Hz
PRIN	42	Input	Preamplifier input	-
POUT	43	Output	Preamplifier output	*Hz
BPIN	44	Input	Band-pass filter input	-
VAN	37	Output	Ground level of analog signal on analog circuit (except MIN amplifier, LIN amplifier and preamplifier)	L
VANM	35	Output	Ground level of analog signal on MIN amplifier, LIN amplifier and preamplifier	L
VREFOUT	46	Output	Reference voltage for A/D circuit	L
BPF01	20	Output	Band-pass filter 1 output	*Hz
RECI1	21	Input	Rectifier 1 input	-
BPF02	22	Output	Band-pass filter 2 output	*Hz
RECI2	24	Input	Rectifier 2 input	-
BPF03	25	Output	Band-pass filter 3 output	*Hz
RECI3	26	Input	Rectifier 3 input	-
BPF04	27	Output	Band-pass filter 4 output	*Hz
RECI4	28	Input	Rectifier 4 input	-
BPF05	29	Output	Band-pass filter 5 output	*Hz
RECI5	30	Input	Rectifier 5 input	-
BPF06	31	Output	Band-pass filter 6 output	*Hz
RECI6	32	Input	Rectifier 6 input	-
BPF07	33	Output	Band-pass filter 7 input	*Hz

* HZ = High impedance

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
RECI7	34	Input	Rectifier 7 input	-
TIO0	19	Input/Output	Test Pin	*Hz
TIO2	18	Input/Output	Test Pin	*Hz
TIO3	17	Input/Output	Test Pin	*Hz
TVIN	45	Input	Test Pin	-
$\overline{SYNC}$	16	Input	Test pin: with a built-in pull-up resistor	-
$\overline{TRESET}$	15	Input	Test pin: with a built-in pull-down resistor	-
$\overline{TCHSET}$	14	Input	Test pin: with a built-in pull-up resistor	-
TDCEN	13	Input	Test pin: with a built-in pull-down resistor	-
DTEST/ TDCSET	12	Input	Test pin: with a built-in pull-down resistor	-
TADO	48	Input	Test pin: with a built-in pull-down resistor	-
TΦ50	54	Output	Test pin	L
TCOMP	47	Output	Test pin	L
SHCK0	52	Output	Test pin	L
SHCK1	51	Output	Test pin	L
SHCK2	50	Output	Test pin	L
SHCK3	49	Output	Test pin	L
VDDD	53	–	Digital circuit power supply pin	-
VDDA	23	–	Analog circuit power supply pin	-
VSSD	6	–	Digital circuit ground pin	-
VSSB	60	–	Data bus buffer ground pin	-
VSSA	38	–	Analog circuit ground pin	-

*HZ = High impedance

(1) D0 ~ D7 (Data bus) [Input/Output]

8-bit bidirectional data bus. To be connected to the inner bus of the recognition system. These pins are used by TC8865F-01 to write data into TC8861F and read data from TC8861F.

(2) $\overline{\text{CHSET}}$ (CHannel SET strobe) [Input]

When L to H rising signal is input to this pin, D0-D7 data (To select multiplexer input filter channel) is written in the internal register of TC8861F. This pin is connected to the $\overline{\text{CHSET}}$ pin of TC8865F-01.

(3) $\overline{\text{ADOUT}}$ (A/D read OUT strobe) [Input]

When L level signal is input to this pin, D0-D7 become the output mode and data (A/D output data) of the output register on TC8861F is output on D0-D7. This pin is to be connected to the $\overline{\text{ADOUT}}$ pin of TC8865F-01.

(4) $\overline{\text{STAR}}$ (a to d STARt signal) [Input]

A/D conversion start signal for A/D converter to be connected to the $\overline{\text{ADSTAR}}$ pin of TC8865F-01.

(5) CK (ClocK) [Input]

Clock input pin. By being connected to the ADCLK pin of TC8865F-01, system clock (Typ. 2MHz) is supplied from TC8865F-01.

(6) $\overline{\text{RESET}}$ (system RESET) [Input]

Reset input pin. To be connected to the $\overline{\text{RESET}}$ pin of TC8865F-01. When L level signal is input to this pin, TC8861F is reset.

(7) $\overline{\text{STBY}}$ (STand-BY) [Input]

Stand-by input pin. To be connected to the $\overline{\text{STBY}}$ pin of TC8865F-01. When L level signal is input to this pin, TC8861F is put in the stand-by state. At this time, however, the $\overline{\text{RESET}}$ pin must have been set at L level in advance.

(8) $\overline{\text{ADRDY}}$ (A/D ReaDY) [Output]

This pin is H level when the A/D converter is in the conversion operation and is L level after end of the conversion. This pin is to be connected to the $\overline{\text{ADRDY}}$ pin of TC8865F-01.

(9) MIN (Microphone INput) [Input]

Microphone signal input pin. A microphone can be directly connected. When the CHML pin is at L level, this pin is valid. The microphone signal ground level must be equal to Vss (ground) level of the LSI.

(10) LIN (Line INput) [Input]

Line input pin. Voice signal is input to this pin through the coupling capacitor. When the CHML pin is at H level, this pin is valid.

(11) CHML (CHange input pin between Min and Lin) [Input]

Control signal to select whether a signal to be processed by TC8861F is input signal from the MIN pin or that from the LIN pin.

(12) MOUT (Min/lin amplifier OUTput) [Output]

Output pin of the MIN or LIN input amplifier selected by the CHML pin. To be connected to the PRIN pin through a capacitor and a variable resistor.

(13) PRIN (PReamplifier INput) [Input]

Preamplifier input pin. Output signal from the MOUT pin is input to this pin. A capacitor 1000pF (deviation within ±30%) is to be placed between this pin and Vss (ground) level in order to stabilize analog characteristics. Without the capacitor, TC8861F does not operate properly.

(14) POUT (Preamplifier OUTput) [Output]

Preamplifier output pin. To be connected to the BPIN pin through a capacitor.

(15) BPIN (Band-Pass-filter INput) [Input]

Band-pass filter input pin. Output signal from the POUT pin is input to this pin.

(16) VAN (Voltage level of ANalog ground) [Output]

Ground level of analog signal on analog circuit except the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(17) VANM (Voltage level of ANalog ground for Mic amplifier) [Output]

Ground level of analog signal on the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(18) VREFOUT (Voltage level of REFerence OUTput for A/D) [Output]

Reference voltage monitor pin for A/D converter.

(19) BPF01~BPF07 (Band-Pass-Filter Output) [Output]

Output pins for 7 band-pass filters. These pins are respectively to be connected to the rectifier input pins (RECI1-7) correspondent to each channel.

(20) RECI1~RECI7 (RECtifier Input) [Input]

Input pins of 7 rectifiers.

(21) TIO0, TIO2, TIO3 (Test Input/Output) [Input/Output]

Test input/output pins. Nothing should be connected to these pins.

(22) TVIN, $\overline{\text{TRESET}}$ [Input]

Test input pins. $\overline{\text{TRESET}}$ pin contains pull down resistor.

Set them at L level. (Connect to the system ground Vss.)

(23) $\overline{\text{SYNC}}$, $\overline{\text{TCHSET}}$, TDCEN, DTEST/TDCSET, TAD0 [Input]

Test input pin with pull-up or pull-down resistor. Nothing should be connected to these pins.

(24) TΦ50, TCOMP [Output]

Test output pin. Nothing should be connected.

(25) SHCK0~SHCK3 (Sample & Hold ClocK) [Output]

Test output pin. Nothing should be connected.

(26) VDDD, VDDA

VDDD is the TC8861F digital circuit power supply pin. VDDA is the TC8861F analog circuit power supply pin. Both should be connected to the plus side of the power supply.

(27) VSSD, VSSB, VSSA

Ground pins. VSSD is the ground for TC8861F digital circuit, VSSB is the ground for TC8861F data bus buffer and VSSA is the ground for TC8861F analog circuit.

4.2.2 TC8865F01

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
CDB0	22	I/O, 3-State	Internal data bus	*Hz
1	23	I/O, 3-State	Internal data bus	*Hz
2	24	I/O, 3-State	Internal data bus	*Hz
3	25	I/O, 3-State	Internal data bus	*Hz
4	26	I/O, 3-State	Internal data bus	*Hz
5	27	I/O, 3-State	Internal data bus	*Hz
6	28	I/O, 3-State	Internal data bus	*Hz
7	29	I/O, 3-State	Internal data bus	*Hz
ADCLK	18	Output	Clock output for TC8861F	H
$\overline{\text{CHSET}}$	14	Output	TC8861F control signal	H
$\overline{\text{ADSTAR}}$	15	Output	TC8861F control signal	H
$\overline{\text{ADOUT}}$	16	Output	TC8861F control signal	H
$\overline{\text{ADRDY}}$	30	Input	TC8861F status signal	–
$\overline{\text{RESET}}$	19	Output	System reset output	L
$\overline{\text{STBY}}$	17	Output	System stand-by output	L
HDB0	98	I/O, 3-State	Host system data bus	*Hz
1	97	I/O, 3-State	Host system data bus	*Hz
2	96	I/O, 3-State	Host system data bus	*Hz
3	95	I/O, 3-State	Host system data bus	*Hz
4	94	I/O, 3-State	Host system data bus	*Hz
5	93	I/O, 3-State	Host system data bus	*Hz
6	92	I/O, 3-State	Host system data bus	*Hz
7	91	I/O, 3-State	Host system data bus	*Hz
HA0	85	Input	Address signal input from Host system	–
1	86	Input	Address signal input from Host system	–
$\overline{\text{HCS}}$	87	Input	Control signal input from Host system	–
$\overline{\text{HRD}}$	88	Input	Control signal input from Host system	–
$\overline{\text{HWR}}$	89	Input	Control signal input from Host system	–
RDB0	74	I/O, 3-State	External memory data bus	H or L
1	73	I/O, 3-State	External memory data bus	H or L
2	72	I/O, 3-State	External memory data bus	H or L
3	71	I/O, 3-State	External memory data bus	H or L
4	70	I/O, 3-State	External memory data bus	H or L
5	69	I/O, 3-State	External memory data bus	H or L
6	68	I/O, 3-State	External memory data bus	H or L
7	67	I/O, 3-State	External memory data bus	H or L
$\overline{\text{CE0}}$	64	Output	External memory chip selection signal	H
$\overline{\text{CE1}}$	63	Output	External memory chip selection signal	H
$\overline{\text{CE2}}$	62	Output	External memory chip selection signal	H
$\overline{\text{OERFSH}}$	60	Output	Control signal for external memory	L
R/W	55	Output	Control signal for external memory	H

* Hz = High Impedance

Pin Name	Pin No.	Input/Output	Function	Status st stand-by
RA0	75	Output	External memory address bus	H
1	76	Output	External memory address bus	H
2	77	Output	External memory address bus	H
3	78	Output	External memory address bus	H
4	79	Output	External memory address bus	H
5	80	Output	External memory address bus	H
6	81	Output	External memory address bus	H
7	82	Output	External memory address bus	H
8	57	Output	External memory address bus	H
9	58	Output	External memory address bus	H
10	61	Output	External memory address bus	H
11	59	Output	External memory address bus	H
12	83	Output	External memory address bus	H
13	56	Output	External memory address bus	H
14	84	Output	External memory address bus	H
CSTBY	3	Input	For producing rising startup timing	–
$\overline{\text{MSTBY}}$	4	Input	Manual stand-by input	–
XIN	33	Input	Ceramic resonator connecting pin	–
XOUT	32	Input	Ceramic resonator connecting pin	–
$\overline{\text{IORD}}$	5	Output	External I/O control signal	H
$\overline{\text{IOWR}}$	6	Output	External I/O control signal	H
$\overline{\text{EXTIO}}$	7	Output	External I/O control signal	H
P0	8	I/O, 3-State	External I/O port	*Hz
P1	9	I/O, 3-State	External I/O port	*Hz
P2	10	I/O, 3-State	External I/O port	*Hz
P3	11	I/O, 3-State	External I/O port	*Hz
P4	12	I/O, 3-State	External I/O port	*Hz
P5	13	I/O, 3-State	External I/O port	*Hz
8M	31	Output	Clock output	H
X0	34	Output	Test pin	H
1	35	Output	Test pin	H
2	36	Output	Test pin	H
3	37	Output	Test pin	H
4	38	Output	Test pin	H
5	39	Output	Test pin	H
6	41	Output	Test pin	H
7	42	Output	Test pin	H
8	43	Output	Test pin	H
9	44	Output	Test pin	H
10	45	Output	Test pin	H

* Hz = High Impedance

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
X11	46	Output	Test pin	H
X12	47	Output	Test pin	H
X13	48	Output	Test pin	H
X14	49	Output	Test pin	H
X15	50	Output	Test pin	H
X16	51	Output	Test pin	H
X17	52	Output	Test pin	H
X18	53	Input	Test pin	–
X19	54	Input	Test pin	–
$\overline{\text{TEST}}$	2	Input	Test pin	–
TST1	99	Input	Test pin	–
$\overline{\text{TST2}}$	100	Input	Test pin	–
$\overline{\text{TSYN}}$	1	Input	Test pin	–
VDD1	21	–	Power supply pin	–
VDD2	65	–	Power supply pin	–
VDD3	90	–	Power supply pin	–
VSS1	20	–	Ground pin	–
VSS2	40	–	Ground pin	–
VSS3	66	–	Ground pin	–

TC8861F I/F Signals

(1) CDB0~CDB7 (Cpu Data Bus) [Input/Output]
8bit bidirectional data bus connected to the internal bus in the recognition system for address and data input/output. These pins are to be connected to DB0~7 of TC8861F.

(2) ADCLK (A - D CLocK) [Output]
TC8861F clock output pin. 2MHz, duty 50% signal is output. This pin is to be connected to the CK pin of TC8861F.

(3) $\overline{\text{CHSET}}$(CHannel SET strobe) [Output]
TC8861F channel set signal output pin. This pin is to be connected to the $\overline{\text{CHSET}}$ pin of TC8861F.

(4) $\overline{\text{ADOUT}}$(A - D read OUT strobe) [Output]
TC8861F A/D output data read out signal outputpin. This pin is to be connected to the $\overline{\text{ADOUT}}$ pin of TC8861F.

(5) $\overline{\text{ADSTAR}}$(A - D STARt signal) [Output]
TC8861F A/D conversion start signal output pin. To be connected to the $\overline{\text{STAR}}$ pin of TC8861F.

(6) $\overline{\text{ADRDY}}$(A - D ReaDY) [Input]
TC8861F A/D conversion end signal input pin. To be connected to the $\overline{\text{ADRDY}}$ pin of TC8861F.

Host System I/F Signals

(7) HDB0~HDB7 (Host Data Bus) [Input/Output]
8bit bidirectional data bus. These pins are to be connected to the data bus of a host system and used for transferring all kinds of data such as commands, status and recognition result.

(8) HA0 , HA1 (Host Port Address 0, 1) [Input]
These pins are to be connected to the address output of a host system and used to specify the kind of data transferred through HDB0~7.

(9) $\overline{\text{HCS}}$ (Host Chip Select) [Input]
A low on this pin enables the TC8865F-01 host system I/F to be active and the $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ pins described below become valid.

(10) $\overline{\text{HRD}}$ (Host ReaD strobe) [Input]
When L level signal is input to this pin at $\overline{\text{HCS}}$=L, the HDB0~7 pins are set to the output mode, and recognition result, status, etc. are output according to the signals of the HA0 and HA1 pins. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ pins must not be put at L level at the same time.

(11) $\overline{\text{HWR}}$ (Host WRite strobe) [Input]
At the rising edge of this pin at $\overline{\text{HCS}}$=L as described above, HDB0~7 data are latched in TC8865F-01. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ pins should not be put at L level simultaneously.

Signals to Reset & Standby Circuits, Clock Oscillator, Test Circuits

(12) CSTBY (Capacitor for STand-BY) [Input]
This pin is connected with a capacitor to the ground to produce the system start sequence control timing when the power supply becomes ON.

(13) $\overline{\text{MSTBY}}$ (Manual STand-BY) [Input]
Manual standby pin. This pin should be set at High level in normal operation.

(14) $\overline{\text{RESET}}$ [Output]
System reset signal output pin. This pin is to be connected to $\overline{\text{RESET}}$ pin of TC8861F.

(15) $\overline{\text{STBY}}$ (STand-BY) [Output]
System standby signal output pin. To be connected to $\overline{\text{STBY}}$ pin of TC8861F.

(16) XIN, XOUT (Xtal-IN, OUT) [Input]
Ceramic resonator connecting pins. An 8MIIz ceramic resonator and capacitor are connected.

(17) $\overline{\text{TEST}}$, TST1, $\overline{\text{TST2}}$ [Input]
Test input pin. These pins should be set at IIigh level in normal operation.

(18) $\overline{\text{TSYN}}$ [Input]
Test input pin. This pin should be set at IIigh level in normal operation.

External memory I/F Signals

(19) RDB0~RDB7(Reference memory Data Bus) [Input/Output]
8bit bidirectional external memory data bus. These pins are to be connected to the external memory data bus.

(20) RA0~RA14 (Reference memory Address) [Output]
The 15bit external pattern memory address bus. These pins are to be connected to the external memory address bus.

(21) $\overline{\text{CE0}}$ (Chip Enable 0) [Output]
This pin is a chip select output available for CPU to accesses memory data addressed 4000H through 5FFFH. This pin should be connected to a chip select pin of 64K static RAM because program codes in TC8865F-01 are located within this address space.

(22) $\overline{\text{CE1}}$ (Chip Enable 1) [Output]
This pin is a chip select output available for CPU to access memory data addressed 6000H through 7FFFH. $\overline{\text{CE1}}$ should not be connected to any signals.

(23) $\overline{CE2}$ (Chip Enable 2) [Output]
This pin is a chip select output available for CPU to access memory data addressed 8000H through FFFFH. $\overline{CE2}$ should not be connected to any signals.

(24) R / W (Read / Write) [Output]
This pin is to be connected to R / W pin of 64kbit static RAM.

(25) $\overline{OERFSH}$ (Output Enable /ReFreSH enable) [Output]
$\overline{OERFSH}$ should not be connected to any signals.

Internal general purpose interface signals

Following pins are not supported by TC8865F-01 system.

(26) $\overline{IOWR}$ (I/O WRite strobe) [Output]
This pin is enabled when CPU writes to a specified I/O port.

(27) $\overline{IORD}$ (I/O ReaD strobe) [Output]
This pin is enabled when CPU reads from a specified I/O port.

(28) $\overline{EXTIO}$ (EXTernal I/O select) [Output]
This pin is a chip select output using with $\overline{IOWR}$, $\overline{IORD}$ pins.

(29) P0~5 (Port 0~5) [Input/Output]
P0 through P5 pins are 6bit general purpose I/O ports, but not available in TC8865F-01 system. These pins should not be connected any signals.

(30) 8M (8MHz clock output) [Output]
This pin outputs 8MHz clock.

(31) X0~X17 [Output]
These pins are test output pins, and should not be connected any signals.

(32) X18,X19 [Input]
These pins are test input pins and should be connected to VSS pin.

Power Supply Signals

(33) VDD1, VDD2, VDD3
The power supply pins. All pins are to be connected to the plus side of the power supply.

(34) VSS1, VSS2, VSS3
The ground pins. All pins are to be connected to the ground side of the power supply.

5. OPERATION AND FUNCTION

5.1 Device Set Functional Organization

The device set provides 11 functions as described in Fig. 5.1. These functions are embedded in 3 LSI hardware and software program on the TC8865F-01 on-chip Mask ROM *.

* Toshiba holds the copyright for the programs embedded in the Mask ROM.

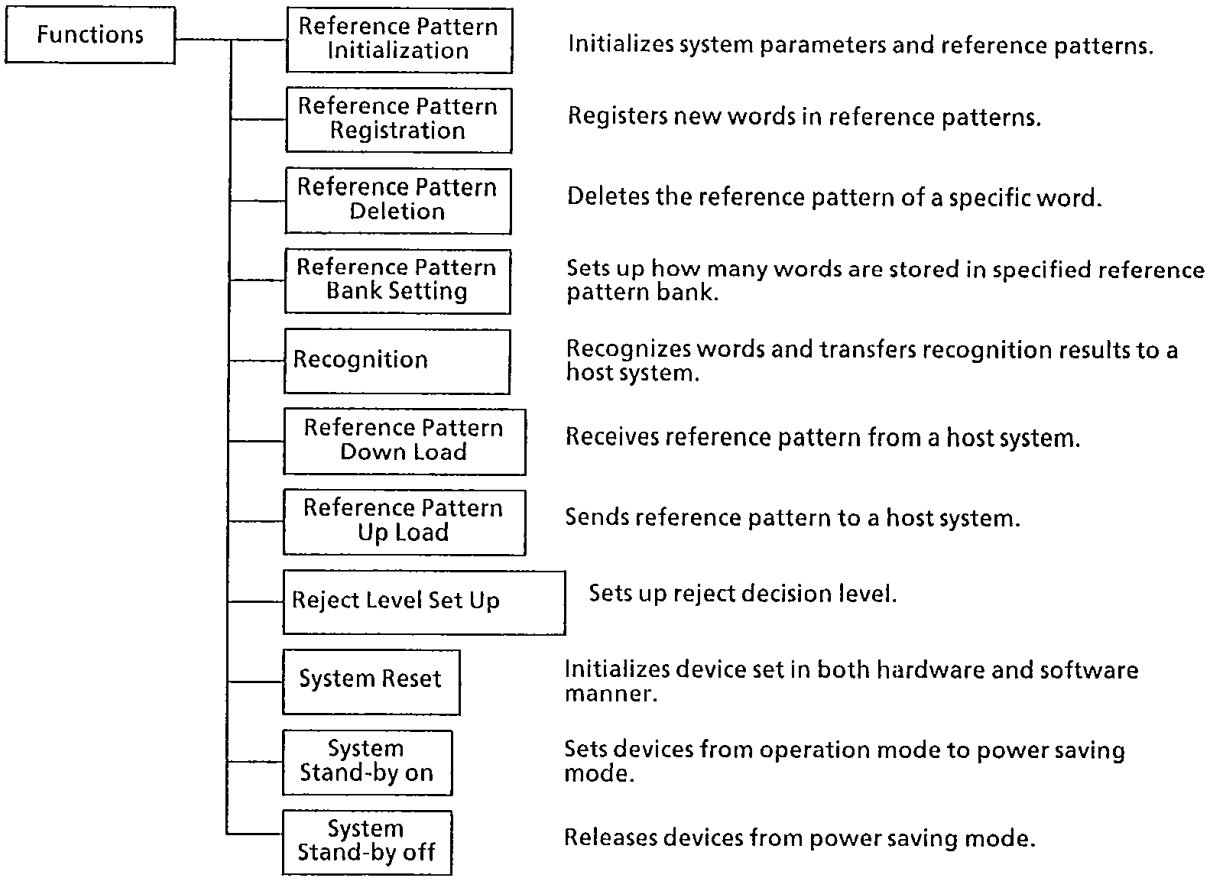


Fig. 5.1 Functional organization of device set

5.1.1 Reference Pattern Registration

Reference patterns for vocabularies to be recognized must be stored in external static RAM before recognition. To store reference patterns is called registration. A reference pattern for a word is made by analyzing three utterances. The sequence of reference pattern production is itemized below and is illustrated in Fig. 5.2.

(1) TC8861F receives three utterances per word to analyze them and to digitize the analyzed analog signals with A/D.

(2) CPU detects word boundaries with A/D output signals. Then it prepares a reference pattern.

(3) The prepared reference pattern is, through external memory I/F, transferred to and is stored in external static RAM.

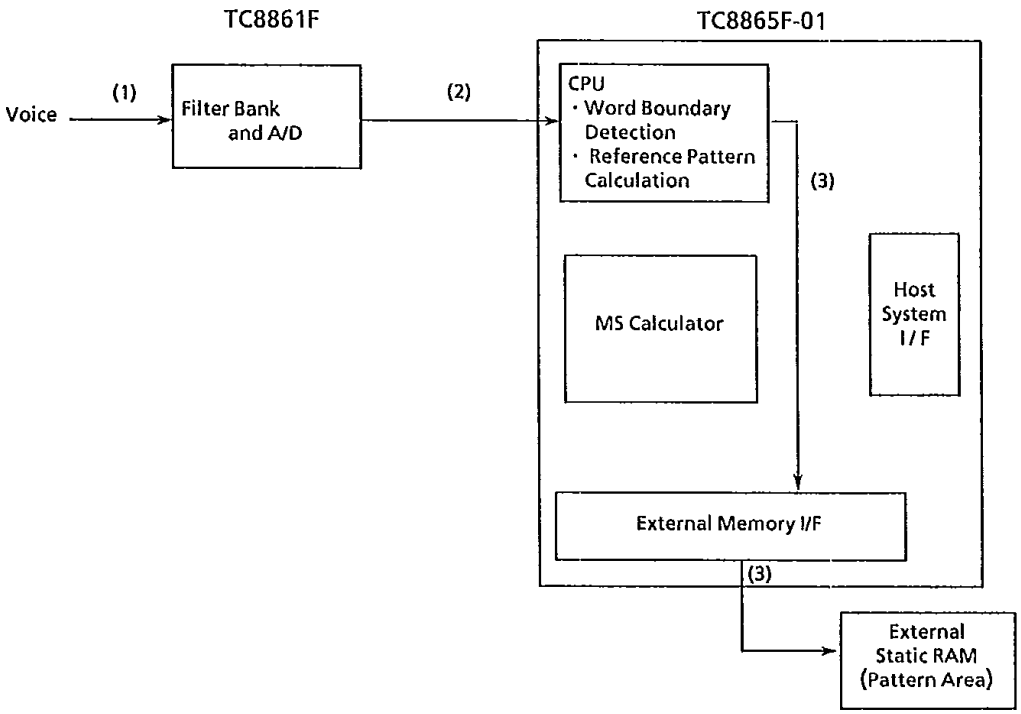


Fig. 5.2 Data flow in reference pattern registration

5.1.2 Recognition

The device set recognizes voices in a way that it compares input voice features with vocabulary reference patterns beforehand stored in an external static RAM. The recognition results indicating most possible word candidates for input words are transferred to a host computer. The functional process is itemized below and is charted in Fig. 5.3.

(1) TC8861F receives a voice to be recognized, analyzes acoustically, and digitizes the analyzed analog signals with A to D.

(2) CPU detects word boundary of A/D output signals. Then the detected signals are transmitted to a data RAM in the MS calculator.

(3) The similarity of the detected signals to all reference patterns stored in external static RAM is examined.

(4) All similarity scores with the whole vocabularies are transferred to CPU.

(5) CPU arranges the scores in reverse-numerical order. And the top three scores and their word numbers are sent to the host system I/F on TC8865F-01.

(6) The top three scores and their word numbers are transferred to a host system.

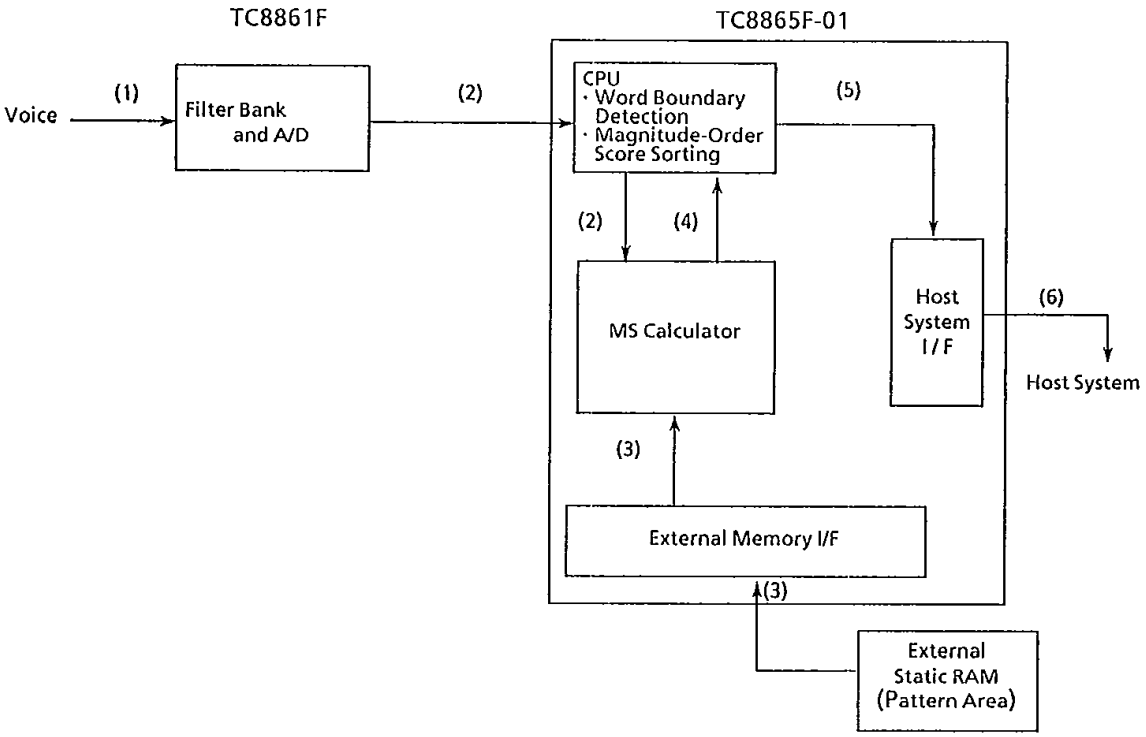


Fig. 5.3 Data flow in recognition

5.1.3 System Inner State Transfer Chart

The device set state transfer chart is described below. This chart is drawed on the view of reference pattern exists or not.

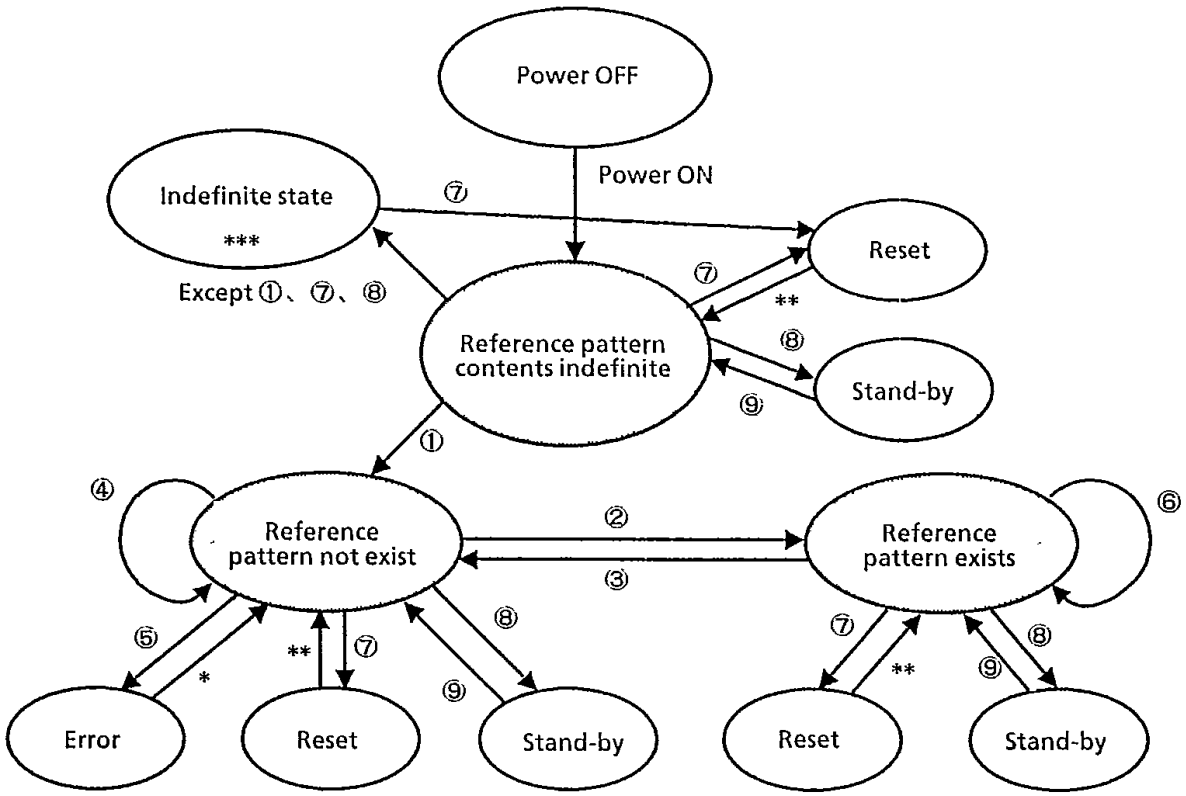


Fig.5.4 System inner state transfer chart

① Reference Pattern Initialization
② Reference Pattern Registration, Reference Pattern Down Load
③ Reference Pattern Initialization, Reference Pattern Deletion (All word)
④ Reference Pattern Initialization, Reference Pattern Bank Setting, Reject Level Set Up
⑤ Recognition, Reference Pattern Up Load
⑥ Reference Pattern Registration, Reference Pattern Deletion(A part),Reference Pattern Bank Setting,Recognition,Reference Pattern Down Load,Reference Pattern Up Load,Reject Level Set Up
⑦ System Reset
⑧ System Stand-by on
⑨ System Stand-by off

* Host system can know that the recognition device set is in error state from reading the return code. After reading return code, the device set status returns command waiting mode.

** Reset state is released automatically.

***The recognition device set status is indefinite because the system work area contents are not defined.

5.1.4 Definition of Recognition Rate

Recognition rate varies with a vocabulary, a voice quality and a recognition rate calculation method. Though many calculation method for unbiased recognition rate have been proposed, there is no standard formula for recognition rate. In this manual, recognition rate is calculated by following definition.

Expression:

$$\text{Recognition rate} = \frac{N-E-R}{N}$$

Where : N means all test voice count. N = 2 (times per words) × m (words).
E means incorrect result count.
R means reject count.

Evaluation method:

(1) The voice is recorded to an audio tape 5 times for each word.

(2) The tape is played back, and 3 utterances of each word are sent to the device set and are analyzed for the reference pattern. Here the audio signal line is fed into LIN pin of TC8861F.

(3) Remaining 2 utterances per word in the audio tape are used for the test data to calculate recognition rate.

Condition:

Reject flag, Too Long flag, Too Low flag and Too High flag are all available and they are counted as R in the above expression. Too Long flag, Too Low flag and Too High flag are mentioned at 5.3.4 (2).

5.1.5 Reject

In the recognition command, the device set calculates the similarity between the input voice and the word in the reference pattern memory. If the device set outputs the most similar word as recognition result unconditionally, there are some problems when the user speaks unregistered word. Therefore, when similarity is lower than the decided level, the device set returns reject status to show that the similarity between input voice and whole reference patterns are low. The device set can not decide from comparison of the similarity and a constant value because the similarity varies with not only input voice but also reference pattern contents. So the device set decides reject state from comparison the value, multiplied calculated value from input voice by the constant value, and the similarity of each word. Host system can change this constant value by using reject level set up command. Reject level set up command is described in 5.3.3 (8).

5.1.6 To Get Optimal Performance

To achieve optimal performance of the device set, it is recommended to follow several notes and advise mentioned below.

Notes about a vocabulary:

(1) This system can deal with an isolated word recognition, but it can hardly recognize connected words and sentences which are spoken continuously.

(2) A vocabulary must be made of 2 through 5 syllables words. A word with one syllable or over six syllables decreases system performance. Especially the alphabet is similar to each other, leading to low performance.

Notes about an utterance:

(1) On registration, at least three utterances are needed and each utterance must be same as much as possible. Different utterances will be rejected.

(2) On recognition, an utterance should be same as registered voice as possible.

(3) The dynamic range of input voice signal is 10 through 15 dB for maintaining high performance.

(4) Two factors to decide the level of input voice signal exist, one is the speaker's voice volume and the other is the distance from the speaker's mouth to a microphone. The recommended distance between the mouth and the microphone is roughly 5 through 15 centimeters according to voice level.

(5) A microphone must observe following conditions:

Frequency characteristics: Flat gain from 200Hz to 7KHz.
Gain deviation is within ±2.5dB.

Directivity : Single directional.

Limitations about an environment noise:

The recognition device set made on the assumption that it is used in a mobile. But the device set may not recognize in all mobile condition because noise level in a mobile varies drastically. The device set is made on the assumption that it is used in regular about 70dBA noise condition. We decide a this 70dBA noise level from environment noise in the mobile which runs with close window and with 100km/h speed on the free way. Usually user registers the reference pattern when the mobile stops and the engine is in idling state. At this time we assume that noise level is about 50dBA. Then the device set is used by executing recognition command even when the mobile runs. At this time we assume that stereo doesn't operate so louder, people except user doesn't speak so louder and the mobile windows are closed in order to shut out external noise. The performance of the device set will decrease under the condition that many pop noise comes from load joint.

Limitation of candidates :

In the case that only a part of the words in reference patterns are previously known as targets, reference pattern bank setting command and specified-bank recognition command are recommended. The unnecessary words for recognition are removed and better performance is achieved.

5.1.7 Improvements on TC8861F/TC8864F-00

Followings are TC8861F/TC8865F-01 improvements on TC8861F/TC8864F-00.

1. TC8861F/TC8865F-01 detects multiple candidates for word duration and uses most possible candidate to register and recognize. This algorithm leads fewer errors in word boundary detection.
2. When the device set is used in a mobile. There are many cases that recognition is executed when the mobile stops and recognition is executed when the mobile runs. Therefore the device set makes two different reference patterns for each word. One is for fewer noise environment and the other is for larger noise environment.
3. At registration and recognition, the environment noise measured at word boundary detection is subtracted from input voice to reduce effects of environment noise.
4. The host system can register all word to each bank. Therefore the word can register to plural banks. For example when bank 0 contains word 1 though word 5, bank 1 can contain word 1 and word 10 TC8861F/TC8864F-00 can not register a word to plural banks.

By above measures the performance of TC8861F/TC8865F-01 increases in regular noise condition. But the device set uses TC8861F and is applied more complicated algorithm, following restrictions still exist.

1. The device set uses two conventional word area for one reference pattern, so maximum recognizable word becomes 20.
2. The device set contains TC8861F for feature extraction, the distance between a microphone and user's mouth needs within 5 though 15 centimeters. If the distance becomes over 15 centimeters, the recognition performance will decrease.
3. The recognition performance will also decrease on the noisy condition such as existing other human's voices or audio sounds. Signal to Noise ratio (S/N) needs about 15dB or larger.

5.2 Host System Interface

5.2.1 Introduction to Interface Hardware

A host system operates the recognition device set with both commands and data transferred through the host system interface circuit on TC8865F-01. The circuit reads or writes 8bit parallel data bus like a general purpose 8bit parallel interface TMP82C55AP-5. TC8865F-01 pins for the operations are HDB0~7, $\overline{HCS}$, $\overline{HRD}$, $\overline{HWR}$, HA0~1. Functional description for the pins are given in Table 5.1.

Table 5.1 Host interface pins and their functions

Pin Names	Number of Pins	Input/ Output	Description
HDB0~7	8	3 state Input/ Output	8 bit 3-state bidirectional data bus. Used for transferring commands, data and status between host system and device set. HDB7 = MSB *, HDB0 = LSB **
$\overline{HCS}$	1	Input	Chip select input. At "L" level, data transfer with host system is enabled. At "H" level, all signals given by host system are ignored.
$\overline{HRD}$	1	Input	Read strobe signal. At "L" level, HDB0~7 is put in the output mode so that host system may read data on HDB0~7. (at $\overline{HCS}$ = HA1 = "L")
$\overline{HWR}$	1	Input	Write strobe signal. At rising edge, command or data are written from HDB0~7 into a specific register. (at $\overline{HCS}$ = HA0 = "L")
HA1, HA0	2	Input	Addresses selecting command/data register, status register or reset/stand-by register. Generally connect to lower 2bits of address bus of host system.

* MSB : Most Significant Bit

** LSB : Least Significant Bit

5.2.2 Interface Hardware Configuration and Its Timing

TC8865F-01 host interface circuit hardware block diagram is illustrated in Fig.5.5. The circuit contains three registers, command/data register (8bit), status register (8bit) and reset/stand-by register (1bit). Host systems reading/writing operations with these registers run the device set. The registers are distinguished among themselves by two address pins (HA0, HA1). The command/data register can be read/written and the status register is dedicated to reading only. The reset/stand-by register is dedicated to writing only.

Table 5.2 shows the pin setting to realize the above mentioned functions. Switching timings in reading or writing operations are illustrated in Fig.5.6 and Fig.5.7.

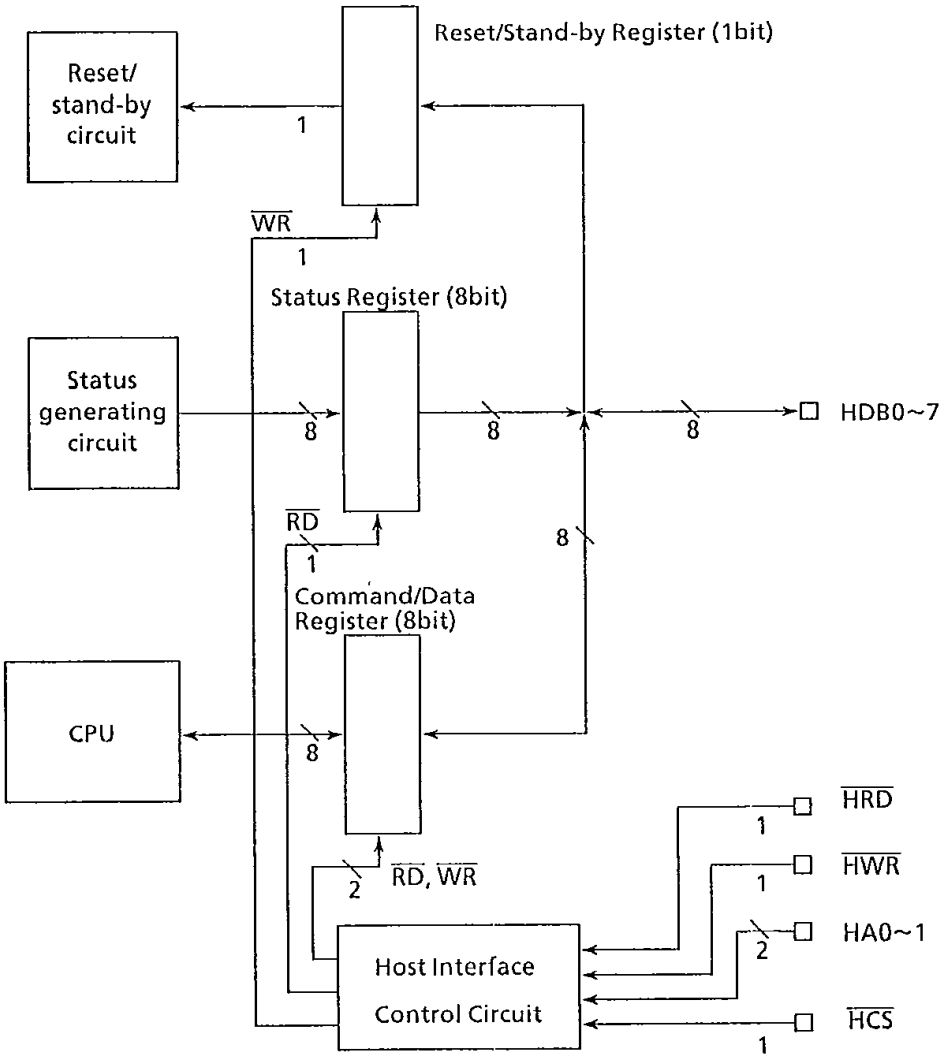


Fig.5.5 Host interface circuit block diagram

Table 5.2 Pin setting for functions

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Functions
0	0	0	0	1	Data Reading.
0	0	0	1	0	Command/Data Writing.
0	1	0	0	1	Status Reading.
1	0	0	1	0	Reset/Stand-by Command Writing.
×	×	0	1	1	Device Set remains unchanged.
×	×	1	×	×	Device Set remains unchanged.
0	1	0	1	0	Device Set remains unchanged.
1	0	0	0	1	Device Set remains unchanged.
1	1	0	0	1	Device Set remains unchanged.
1	1	0	1	0	Device Set remains unchanged.
×	×	0	0	0	Not Allowed.

0 = L level, 1 = H level, × = Don't care

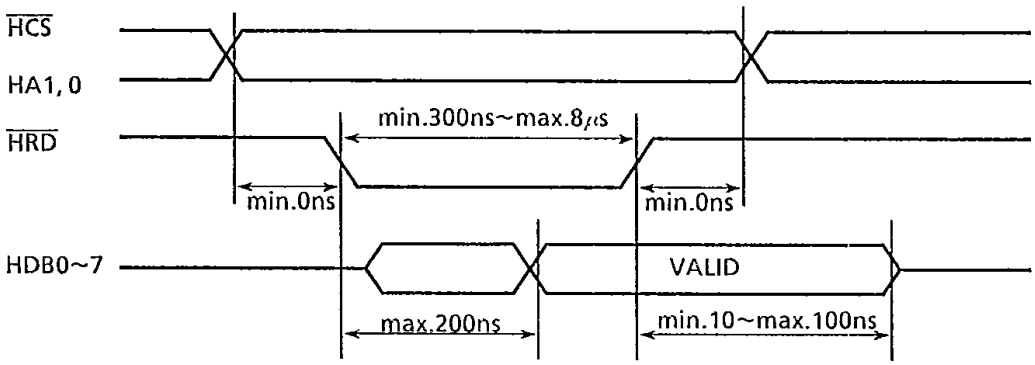


Fig.5.6 Host interface reading cycle timing

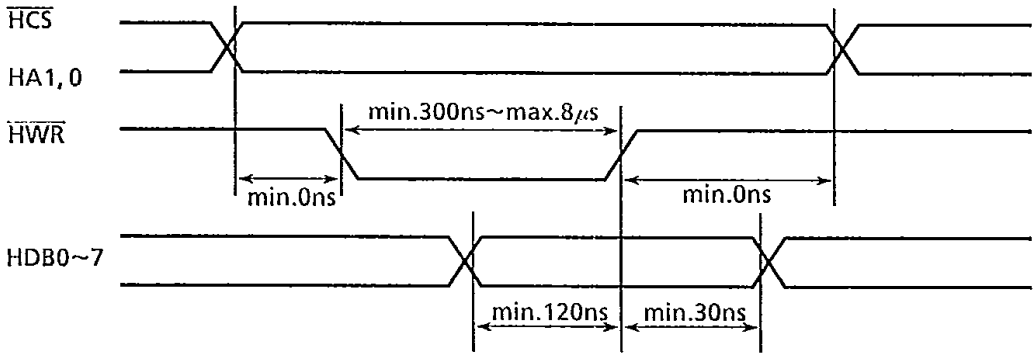


Fig.5.7 Host interface writing cycle timing

5.2.3 How to Use Command/Data Register

Command/data register with 8bit data is used for "command"/"data" writing operation and data reading operation. Here "command code" is defined as 8bit code given into this register by a host computer on waiting state for the next command. On the other hand, "data" are defined as 8bit data transferred through the register while the device set is executing commands. Examples of "data" are "word number" given by a host system and "control code" output to a host system in registration command execution.

Table 5.3 shows a command list to with the command/data register.

Table 5.3 Commands with command/data register

Command	HDB0~7	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$
Reference Pattern Initialization	28H	0	0	0	1	0
Reference Pattern Registration	29H					
Reference Pattern Deletion	2AH					
Reference Pattern Bank Setting	2CH					
Recognition 1,2 *	08H~0FH、18H~1FH *					
Reference Pattern Down Load	22H					
Reference Pattern Up Load	23H					
Reject Level Set Up	3CH					

1 = H Level, 0 = L Level

* Recognition command consists of Recognition 1 command and Recognition 2 command. In Recognition 1 command the device set uses average noise data that is measured before recognition command is entered as decision data for detecting word boundary. In Recognition 2 command the device set uses noise data that is measured just after recognition command is entered. Recognition 1 command code number is from 08H to 0FH and Recognition 2 command code number is from 18H to 1FH. If the host system has not executed bank setting command, command code 08H though 0FH has same effects as Recognition 1 command and command code 18H though 1FH has same effects as Recognition 2 command. On the other hand, if the host system has executed bank setting command, command code 08H and 18H only effects bank 0 and 09H and 19H effects bank 1 and 0AH and 1AH effects bank 2 and so on.

5.2.4 Hand Shake with Command/Data Register

Communication between the host system and the device set with the command/data register employs "hand shake" protocol. This protocol uses two status signals HRRDY (Host Read ReaDY) and HWRDY (Host Write ReaDY), offered as flag bits on the status register.

HRRDY = 1 indicates that the device set is ready to send some data to the host system. HWRDY = 1 means that the device set is waiting for command code and data to come from the host system. Note that the two status signals will not be 1 simultaneously.

Host system operational sequence is as follows:

(1) When commands/data are written into the device set,

① Check whether HWRDY 1.

② Go to ① when HWRDY is 0 (when the device set is not ready to receive command / data from the host system).

③ Write command code or data into the device set when HWRDY is 1 (when the device set is waiting for command code or data). The finish of writing operation automatically leads to HWRDY = 0. (The device set is released from the command / data waiting state.) Exit.

(2) When data are read out from the device set

① Check whether HRRDY = 1.

② Return to ① when HRRDY is 0.

③ Read data from the device set when HRRDY is 1 (when the device set is ready to output date to the host system). Reading operation automatically leads to HRRDY = 0. (The device set is released from the sending-data ready state.) Exit.

Fig.5.8 illustrates the "hand shake" protocol timing chart.

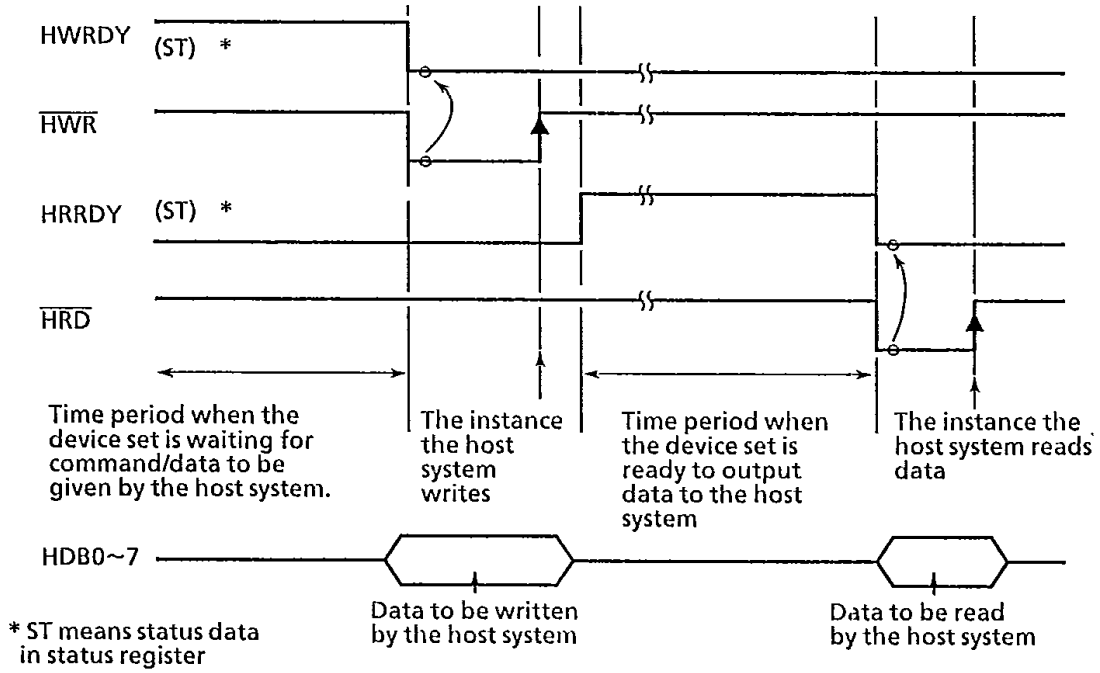
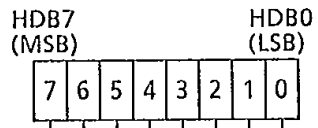


Fig.5.8 "Hand shake" timing chart

5.2.5 How to Use Status Register

Status register with 8bit flags indicating the device set state is allowed only to be read. Reading operation doesn't require the "hand shake" protocol described in 5.2.4. Instead reading is permitted in any instance. Each bit flag meaning is explained in the following figure.



HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$
0	1	0	0	1

1 = H Level, 0 = L Level

HWRDY — HWRDY "1" indicates that command/data register is ready to receive data given by a host system.

HRRDY — HRRDY "1" indicates that command/data register contains data to be read by a host system.

STBY — STBY "1" means the device set is in power saving mode.

RESET — RESET "1" means the device set in reset period with no data transfer allowed.

TMGER — TMGER becomes "1" when writing operation to command/data register is executed during reset period. Note that the writing operation is dealt invalid. The consecutive writing operation to command/data register releases TMGER from "1" with its original function executed.

CFER — CFER becomes "1" within 150μs when undefined command or recognition command with no reference pattern registered is executed. The consecutive normal command writing operation to command/data register releases CFER from "1". The host system can also know the availability of later command by checking the error bit in the return code because the host system must read the return code after all command entry. The return code is mentioned at 5.3.4(3).

Undefined — This bit is always "0".

DISRST — DISRST "1" shows entering reset command causes destruction of reference pattern in executing reference pattern registration command. So when DISRST is "0" or the command without reference pattern registration command is in executing, the host system can initialize the device set with no attention by using reset command. But in this case the host system must enter the reset command within 20ms after checking the DISRST status.

Fig.5.9 Flag meanings of status register

5.2.6 How to Use Reset/Stand-by Register

Reset/stand-by register with a 1bit writing only flipflop offers three kinds of functions determined by combination of the current device set state (power saving mode or operating mode) and 1bit datum, 0 or 1, to be written.

Writing with the least significant bit (LSB) of 0 (ex. 00H) to the reset/stand-by register in the operating mode results in reset command execution, which initializes the device set in hardware way and then returns it back to a waiting state for host system commands. Also writing with LSB of 1 (ex. 01H, FFH) in the operating mode leads to the power saving mode in the device set; which ceases all operations. Writing with LSB of 0 in the power saving mode releases the device set from the power saving mode to the operating mode.

Table 5.4 describes pin settings and functions. Note that writing to the reset/stand-by register do not require the "hand shake" protocol described in 5.2.4, and is allowed to be executed any time.

Table 5.4 Reset/stand-by register function

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	HDB0 (LSB)	Description	The Device Set State on Writing
1	0	0	1	0	0	Reset the device set	Operating Mode
1	0	0	1	0	1	Place the device set in power saving mode	Operating Mode
1	0	0	1	0	0	Release the device set from power saving mode	Power Saving Mode

1 = H level, 0 = L level

5.3 Host System Command

5.3.1 Command List

All commands available are listed in Table 5.5. These commands are 8bit data written into the device set by a host system. The commands are divided into two categories, one employing command/data register and the other using reset/stand-by register.

Table 5.5 Command list (1 = H level, 0 = L level)

Command Name	Command Code	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Notes
Reference Pattern Initialization	28H	0	0	0	1	0	Command/data Register used
Reference Pattern Registration	29H	0	0	0	1	0	
Reference Pattern Deletion	2AH	0	0	0	1	0	
Reference Pattern Bank Setting	2CH	0	0	0	1	0	
Recognition 1,2 *	08H~0FH, 18H~1FH *	0	0	0	1	0	
Reference Pattern Down load	22H	0	0	0	1	0	
Reference Pattern Up load	23H	0	0	0	1	0	
Reject Level Set Up	3CH	0	0	0	1	0	
Reset	HDB0 = 0	1	0	0	1	0	Reset/stand-by Register used
Stand-by On	HDB0 = 1	1	0	0	1	0	
Stand-by Off	HDB0 = 0	1	0	0	1	0	

* Recognition command consists of Recognition 1 command and Recognition 2 command. In Recognition 1 command the device set uses average noise data that is measured before recognition command is entered as decision data for detecting word boundary. In Recognition 2 command the device set uses noise data that is measured just after recognition command is entered. Recognition 1 command code number is from 08H to 0FH and Recognition command 2 code number is from 18H to 1FH. If the host system has not executed bank setting command, command code 08H though 0FH has same effects as Recognition 1 command and command code 18H though 1FH has same effects as Recognition 2 command. On the other hand, if the host system executed bank setting command, command code 08H and 18H effects only bank 0 and 09H and 19H effects bank 1 and 0AH and 1AH effects bank 2 and so on.

Table 5.6 Recognition 1, 2 command list (1 = H level, 0 = L level)

Command Name	Command Code	Test Condition
Bank 0 Recognition	08H、18H	HA1 = HA0 = $\overline{HCS}$ = $\overline{HWR}$ = 0 $\overline{HRD}$ = 1
Bank 1 Recognition	09H、19H	
Bank 2 Recognition	0AH、1AH	
Bank 3 Recognition	0BH、1BH	
Bank 4 Recognition	0CH、1CH	
Bank 5 Recognition	0DH、1DH	
Bank 6 Recognition	0EH、1EH	
Bank 7 Recognition	0FH、1FH	

5.3.1 (1) Reference Pattern Initialization Command (28H)

Reference pattern initialization command initlalizes reference patterns and CPU scratchpad memory so that it may enable the device set to be ready for initial registration. The reference pattern memory is cleared to zero. This command should be executed at least once after power supply to the device set is turned on.

Process in the device set:

Start.
↓
CPU scratchpad area in the external static RAM is initialized.
↓
Reference pattern area is cleared to zero.
↓
command waiting.

5.3.1 (2) Reference Pattern Registration Command (29H)

This command registers voice features on reference pattern RAM segments designated by word numbers. Usually three utterances per word are required to be input through analog input pin on TC8861F. Reference pattern is generated by calculating these three utterances. If the similarity among the spoken three is low, another three utterances for the word are required.

Process in the device set:

Start.
↓
Voice through analog input pin on TC8861F is input.
Three utterances per word.
↓
Word boundary is detected.
↓
Validity of the input voice is checked.
↓
Reference pattern is prepared.
↓
Reference pattern is registered to external static RAM.
↓
command waiting.

5.3.1 (3) Reference Pattern Deletion Command (2AH)

Reference pattern deletion command clears into zero reference pattern data of a specified word.

Process in the device set:

Start.
↓
Reference pattern data for the designated word is cleared to zero.
↓
command waiting.

5.3.1 (4) Reference Pattern Bank Setting Command (2CH)

This command specifies connection with bank number and word number in each bank. After execution of reference pattern initialization command, whole words in the reference pattern connects with whole bank. After execution of reference pattern bank setting command, at the recognition command, only the registered words in the specified bank become recognition object.

Process in the device set:

Start.
↓
Validity of written bank setting parameters for each bank is examined.
↓
Bank setting parameters are registered to the specified area in scratchpad area.
↓
command waiting.

5.3.1 (5) Recognition Command 1,2 (08H~0FH , 18H~1FH)

These commands perform recognition of input voice with the reference pattern which is registered in reference pattern registration command. If the reference pattern doesn't exist (the case happens if any registration has not been executed after reference pattern initialization), the recognition command does not proceed any longer and returns command error code 02H and leads to command waiting state.

Process in the device set:

Start.
↓
Voice through analog input pin on TC8861F is input.
↓
Word boundary is detected.
↓
Similarity scores between input voice and reference patterns are calculated.
↓
Similarity scores are arranged in reverse numerical order.
↓
Final recognition result is decided according to above similarity score order.
↓
Recognition result is transferred to host system.
↓
command waiting.

5.3.1 (6) Reference Pattern Down Load Command (22H)

Reference pattern down load command receives the reference patterns from a host system and then stores them to the external static RAM. When reference patterns already exist in the external static RAM, contents of reference pattern are replaced with the new data from the host system.

Process in the device set:

Start.
↓
Header data (212 bytes) are received and stored to the scratchpad area.
↓
Reference pattern data are transferred to device set until end of data code (80H) is met. They are all stored to the reference pattern area.
↓
command waiting.

5.3.1 (7) Reference Pattern up Load Command (23H)

Reference pattern up load command sends the reference patterns to a host system. Reference patterns are transferred with the format explained in 5.3.4(4). When there is no reference patterns, if the host system sends this command, the device set returns the error code 04H and becomes command waiting mode.

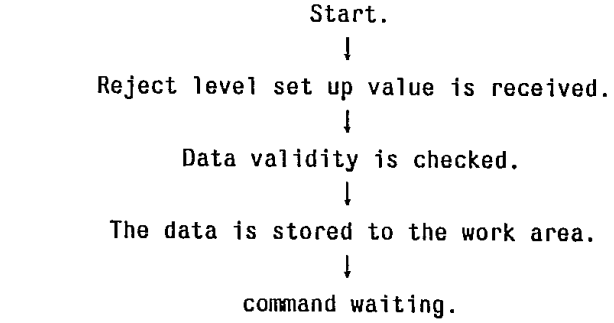
Process in the device set:

Start.
↓
Number of words (212 byte) is sent to host system.
↓
Reference pattern data and end of data code (80H) are sent.
↓
command waiting.

5.3.1 (8) Reject Level set up Command (3CH)

The device set tells information about that recognition result has low reliability by setting reject bit in recognition header. The decision whether reject or not is made by comparison similarity and criterion. This criterion is set up by reject level set up command. The initial reject level is set up as 01H by Reference pattern initialization command.

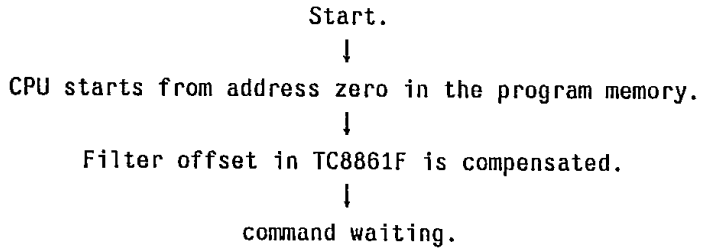
Process in the device set:



5.3.1 (9) System Reset Command (Reset / Stand-by Register)

This command initializes the device set in hardware manner. The data in the external static RAM keeps its contents after this command. But in some cases, the device can't keep the contents of the external static RAM. Refer to 5.3.3(14) Notes on system Reset Command Usage for more details.

Process in the device set:



5.3.1 (10) System Stand-by on Command (Reset / Stand-by Register)

The device set has the power saving function. In the power saving mode, internal system clock is stopped and system power consumption becomes less than 10μA. This state is called stand-by mode. The data in the scratchpad area and reference patterns keep their contents even in the stand-by mode. To release from stand-by mode, system stand-by off command should be executed.

Process in the device set:

Start.
↓
To stand-by mode (system clock is stopped).

5.3.1 (11) System Stand-by off Command (Reset / Stand-by Register)

This command releases the device set from stand-by mode to normal mode. In normal mode internal system clock operates normally.

Process in the device set:

Start.
↓
System clock starts.
↓
CPU starts from address zero in the program memory.
↓
Filter offset in TC8861F is compensated for.
↓
Command waiting.

(Note) : Offset values vary by individual TC8861F or its assembly condition. Offset degrades frequency analysis accuracy of TC8861F and then reduces recognition performance. To eliminate this harmful influence, TC8861F is equipped with offset compensation function.

5.3.2 Host System Operation Flow Chart Example

Here described is a flow chart example to operate the device set in the following sequence:

(1) Reference pattern initial registration.

(2) Reference pattern registration.

(3) Recognition.

(4) Reference pattern deletion.

These three activities are essential to any recognition device. Fig.5.10 illustrates the flow chart. More details in each operation in Fig.5.10 are referred to 5.3.3.

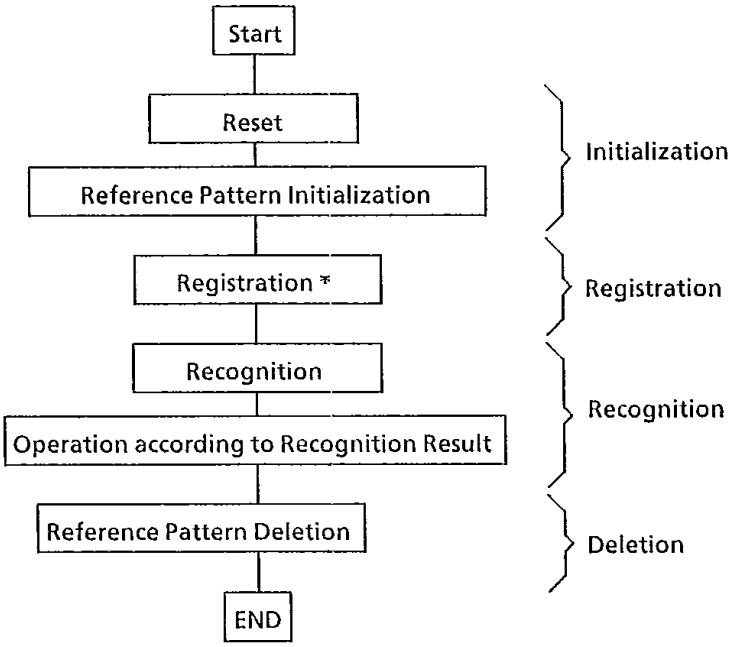


Fig.5.10 Host system operation flow chart example

* More than 3 utterances per word may be required in some cases.
See details in 5.3.3 (2) Reference Pattern Registration Command.

5.3.3 Command Description

This section describes a host system operational flow chart and a timing diagram for each command.

5.3.3 (1) Reference Pattern Initialization Command (28H)

Reference pattern initialization command initializes reference patterns and CPU scratch-pad memory so that it may enable the device set to be ready for initial registration. System parameters stored in the scratch-pad RAM are initialized. Reference patterns on external RAM are initialized to zero from word number 1 to the word number 20. This command should be executed at least once after power supply to the device set is turned on.

(1) Flow chart

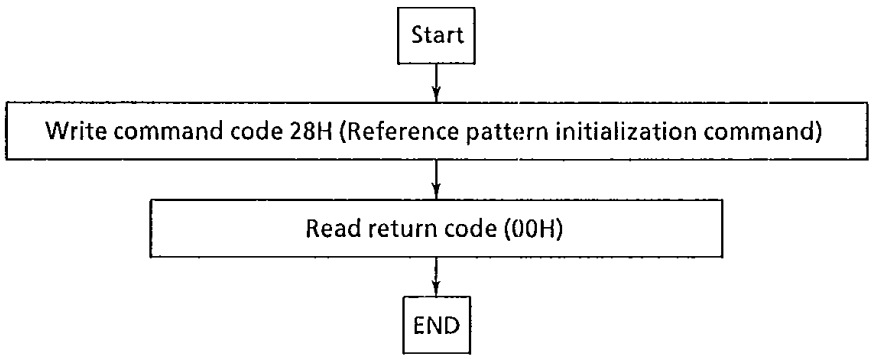
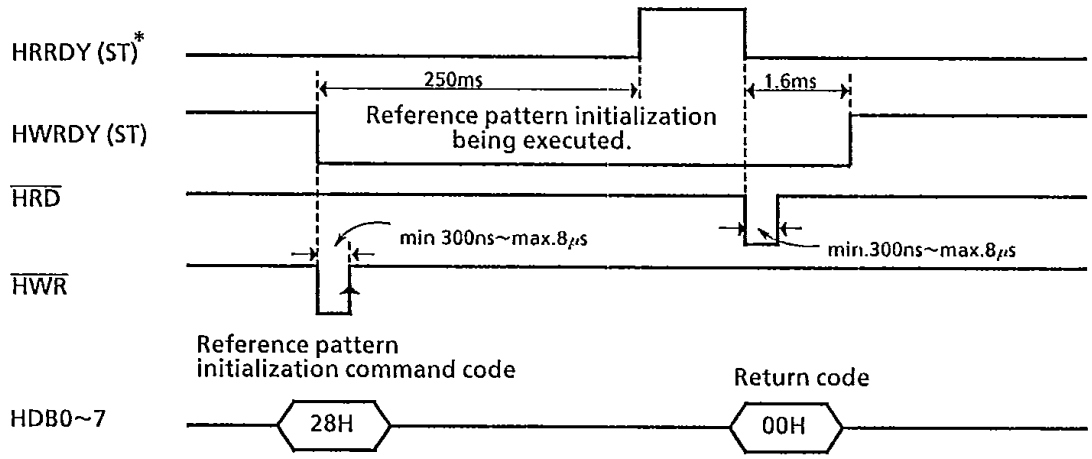


Fig.5.11 Reference pattern initialization command flow chart

(2) Timing chartand HWRDY before transmission .



* ST means status in status resister. Status logic on the timing chart is shown by "0" or "1" , and the device pin signal is shown by "L" or "H".

Fig.5.12 Reference pattern initialization command timing chart

5.3.3 (2) Reference Pattern Registration Command (29H)

This command registers voice features on reference pattern RAM segments designated by word number, It allows multiple words to be registration in single execution, When reference pattern already exists in designated word area, contents of reference pattern are replaced with new data, Fig. 5.13 shows the flow chart for a host system, After registration command (29H) is written to command/data register, the device set returns return code (00H) and asks for a word number to be registered, When the word number is written, usually three utterances per word are required to be input through analog input pin on TC8861F, In some cases where similarity among the spoken three is low, another three utterances for the word is required, The device set may request utterance up to 9 times per word, Writing "FFH" as a word number starts arithmetic operations to create reference patterns and then output return code which means normal end state, Reading this code leads the device set to the state waiting for another command, The arithmetic operations for more number of words stored require more processing time, Typical processing time is 10 seconds for 20 words.

(1) Flow chart

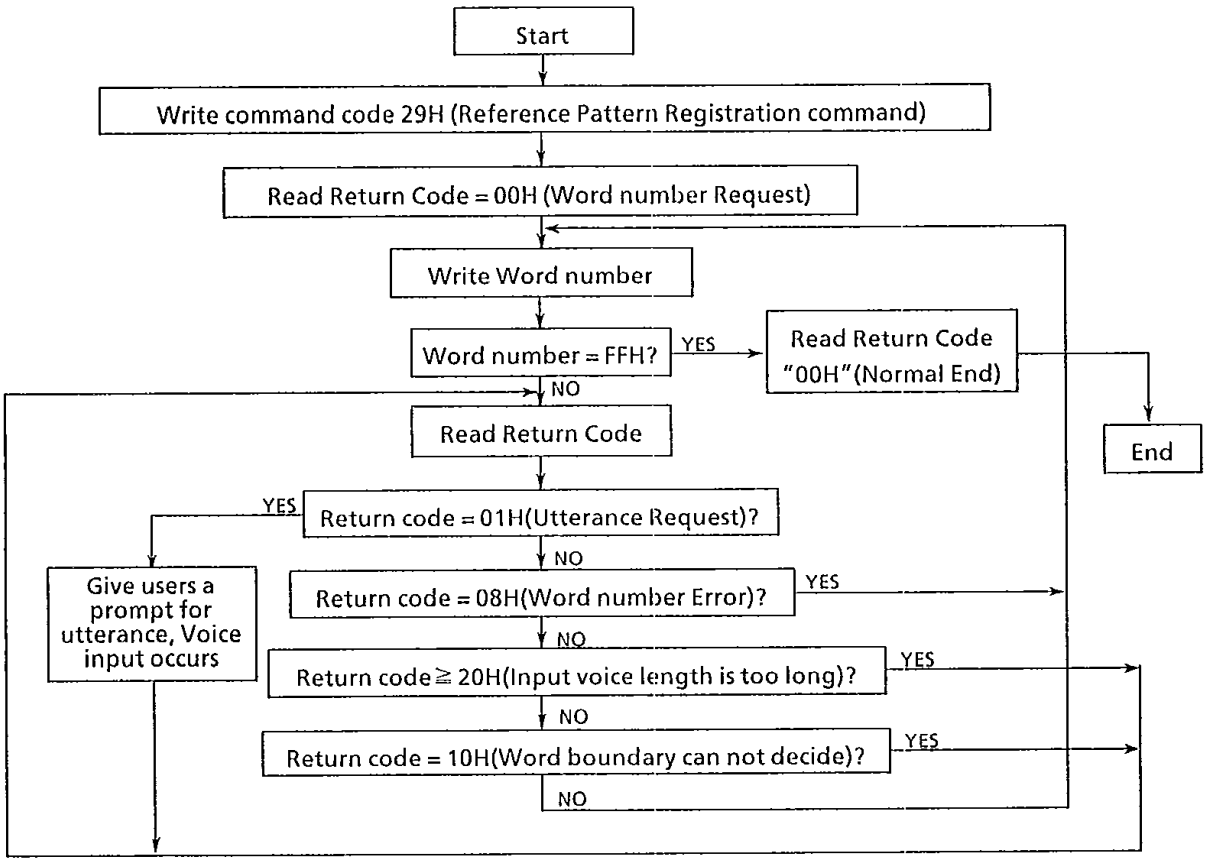


Fig. 5.13 Reference pattern registration command flow chart

(2) Timing chart

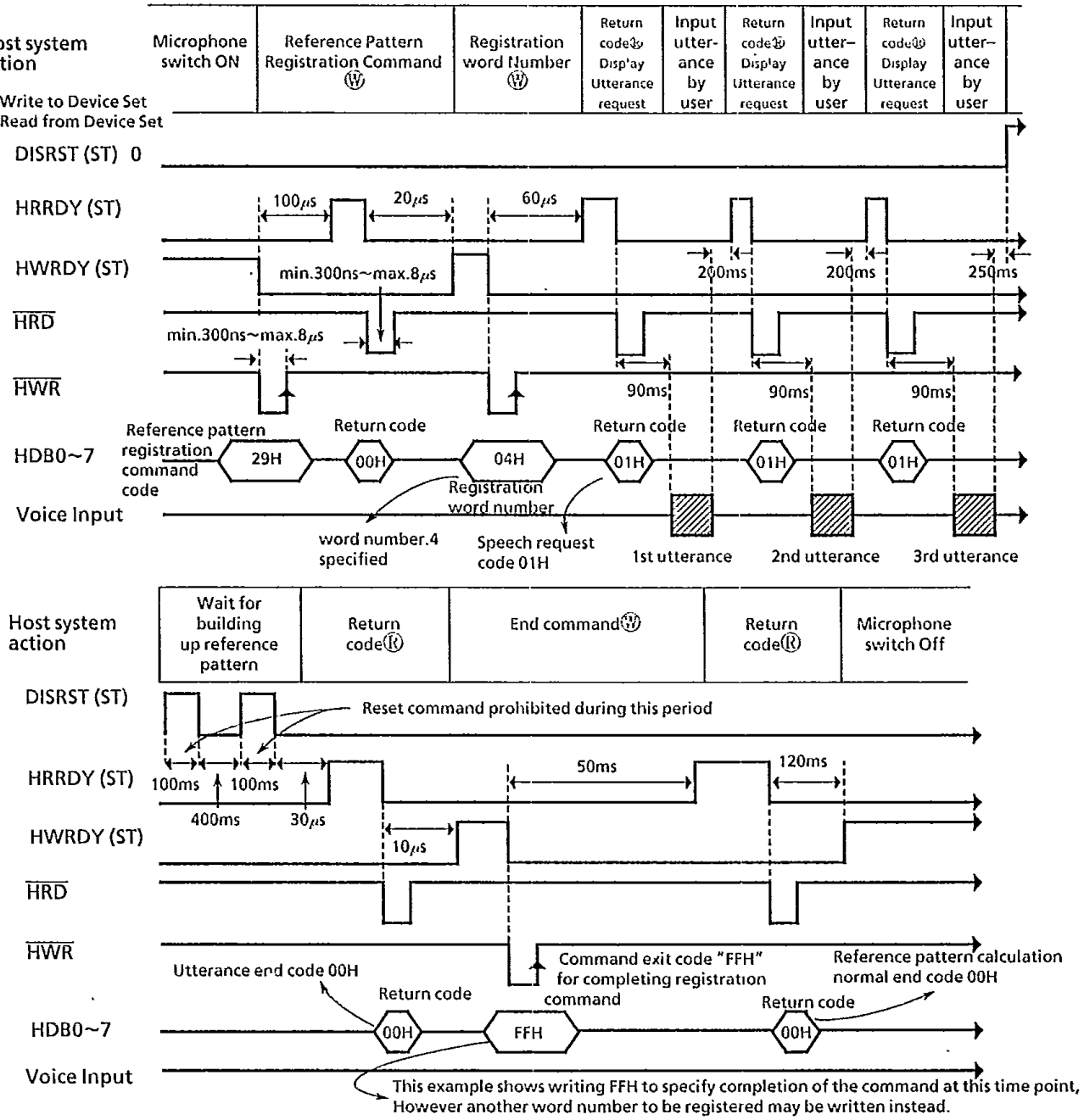


Fig. 5.14 Reference pattern registration command timing chart (In the case of three times utterance for word)

(Note) Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents , The host system must check HRRDY and HWRDY before transmission .

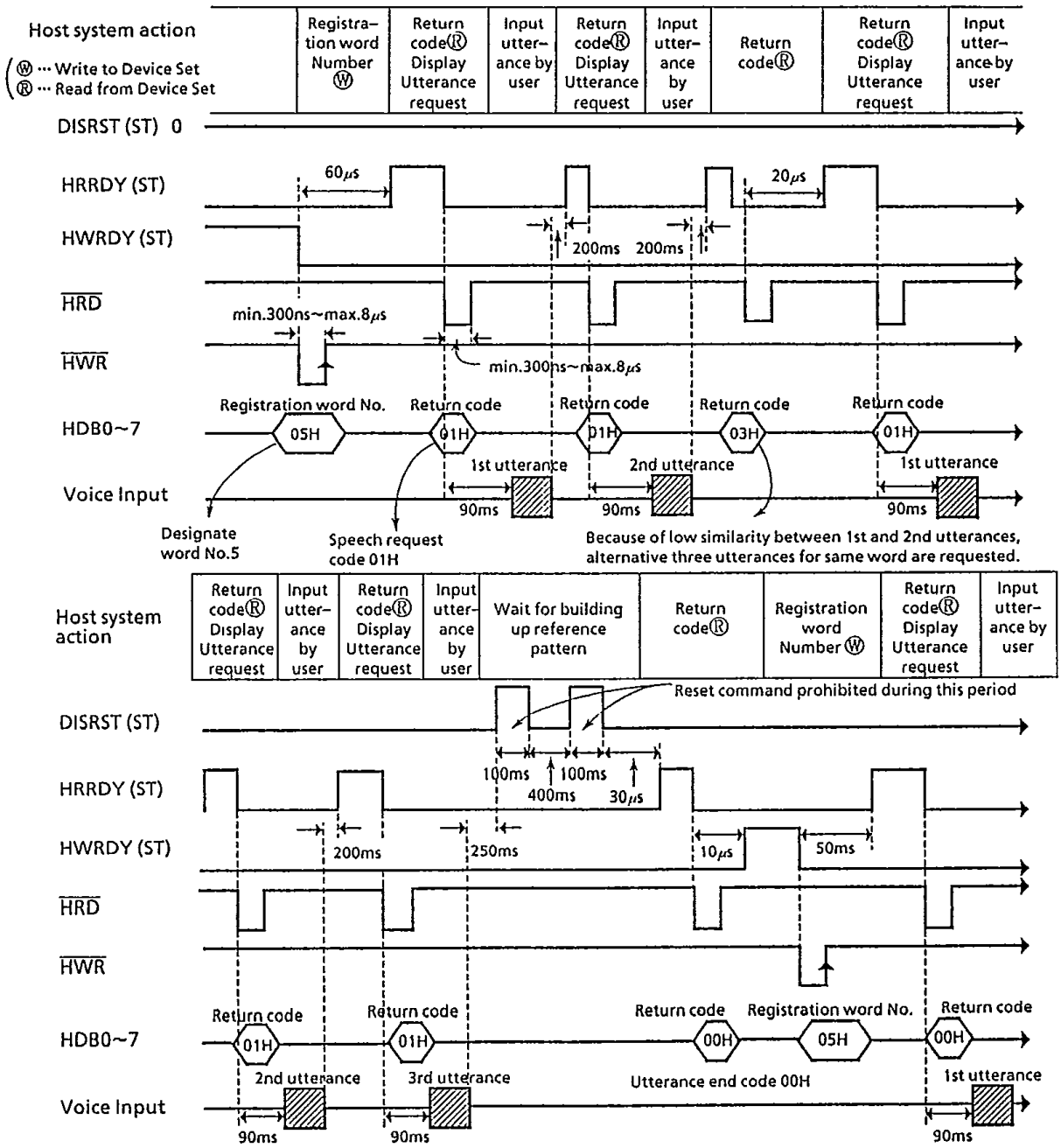


Fig.5.15 Reference pattern registration command timing chart (The case of low similarity between 1st and 2nd utterance)

(Note) Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents, The host system must check HRRDY and HWRDY before transmission.

(3) Cautions in Using Reference Pattern Registration.

A host system is required to observe cautions described below when it uses reference pattern registration command, Refer to Fig. 5.14 and Fig. 5.15 for thorough understanding.

① Microphone must be on and ready to transmit voice signal to TC8861F by the time the host system writes word number to be registered, When multiple of words are to be registered sequentially in a single registration command, the microphone may not be turned off word by word, Instead, it is allowed to be kept on all the time when reference pattern registration command is executing.

② After word number is written, the control code must be read out both to confirm the utterance request code 01H and to give users a prompt for utterance within 90ms from the time point when $\overline{\text{HRD}}$ pin changes from H to L.

③ However, a speaker is prohibited to give utterance in this 90ms time period, The reason is that the device set monitors environmental noise level to determine a threshold for discrimination of voice signal from background noise, This monitor is done immediately before the device set is ready to receive input voice signal, Thus the period is called environmental noise level monitoring period, So microphone must be on to receive background noise then, Also note that every utterance request is accompanied by the monitoring period.

④ Nevertheless, a prompt to urge utterance can still be given to speakers within the period, It is because response time of human being is not less than 100ms, Therefore there is no risk that a speaker actually gives utterance in that period even if the speaker recognizes a prompt and utters immediately.

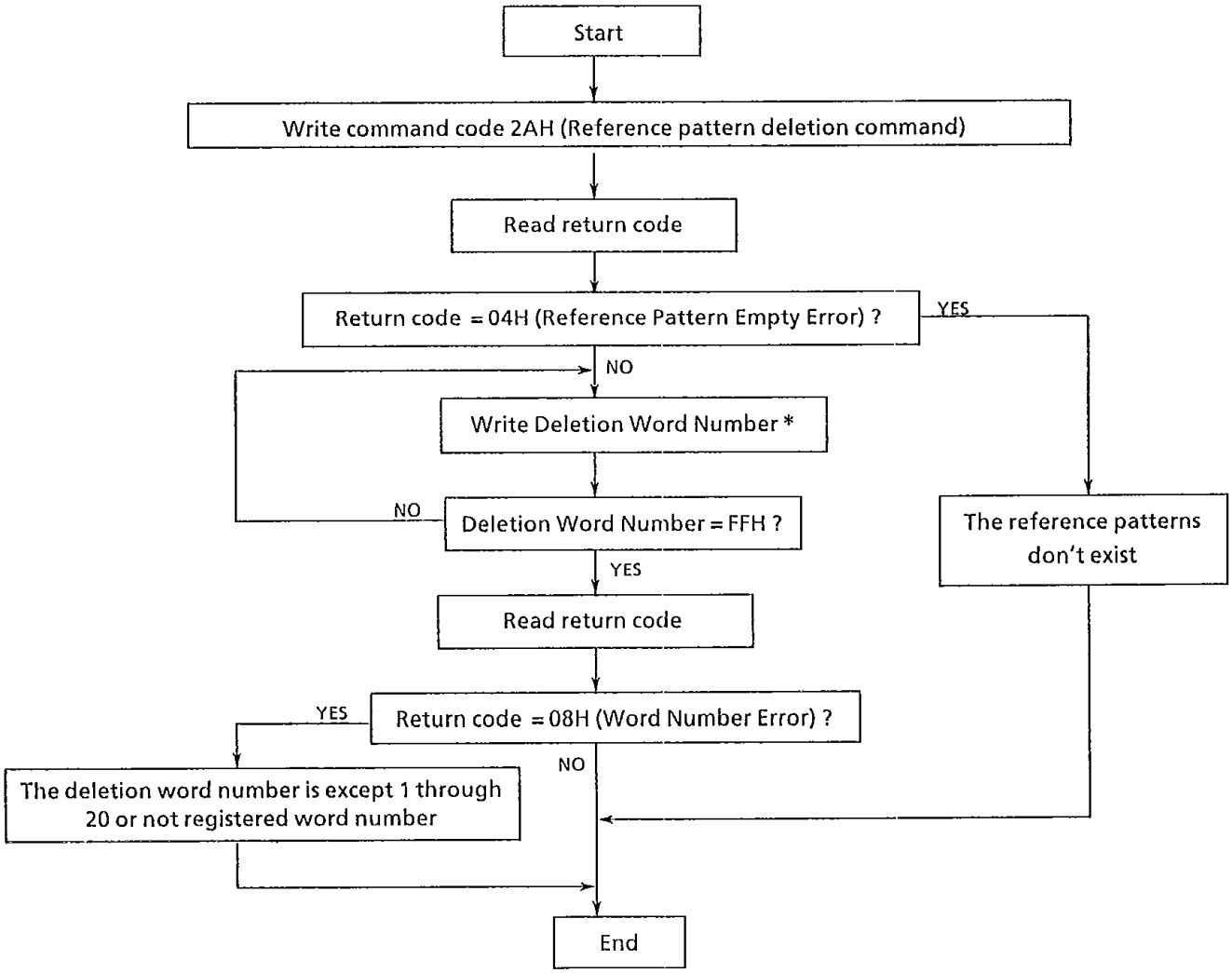
⑤ A prompt given far behind the period may cause the device set to mistake meaningless voice signal for targeted utterance, So a prompt is strongly recommended to be given within the period.

⑥ Once an utterance is given, the device set analyzes the utterance acoustic signal and sets HRRDY status flag to 1 at its completion, The control code is then read out to check whether the given utterance is normally accepted, The control codes 00H or 01H indicates normal completion of voice input activity but the others mean abnormal completion, 00H indicates that three utterances for a word have been successfully given, whereas 01H shows that more utterances for the word are to be given next, Other codes than 00H and 01H urge the host system to read out another control code successively, Then the device set retries a prompt again for the first utterance of the word.

5.3.3 (3) Reference Pattern Deletion Command (2AH)

Reference Pattern Deletion command clears reference pattern data of a specified word into zero, Word numbers and their reference patterns of words other than the specified remains unchanged.

(1) Flow Chart



* If the host system writes the word number which is not registered or not 1 through 20 , the reference pattern or work area contents are not destroyed .

Fig.5.16 Reference pattern deletion command flow chart

(2) Timing Chart

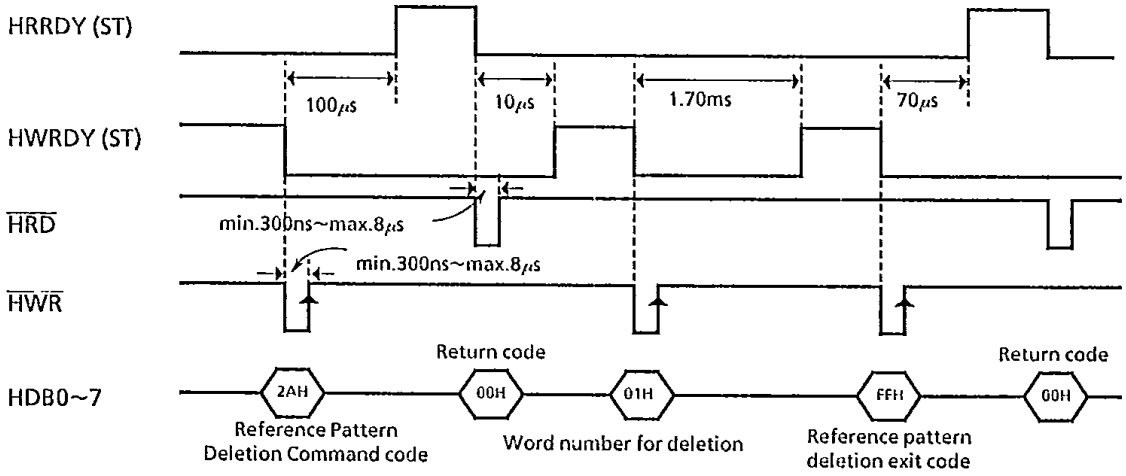


Fig.5.17 Reference pattern deletion command timing chart

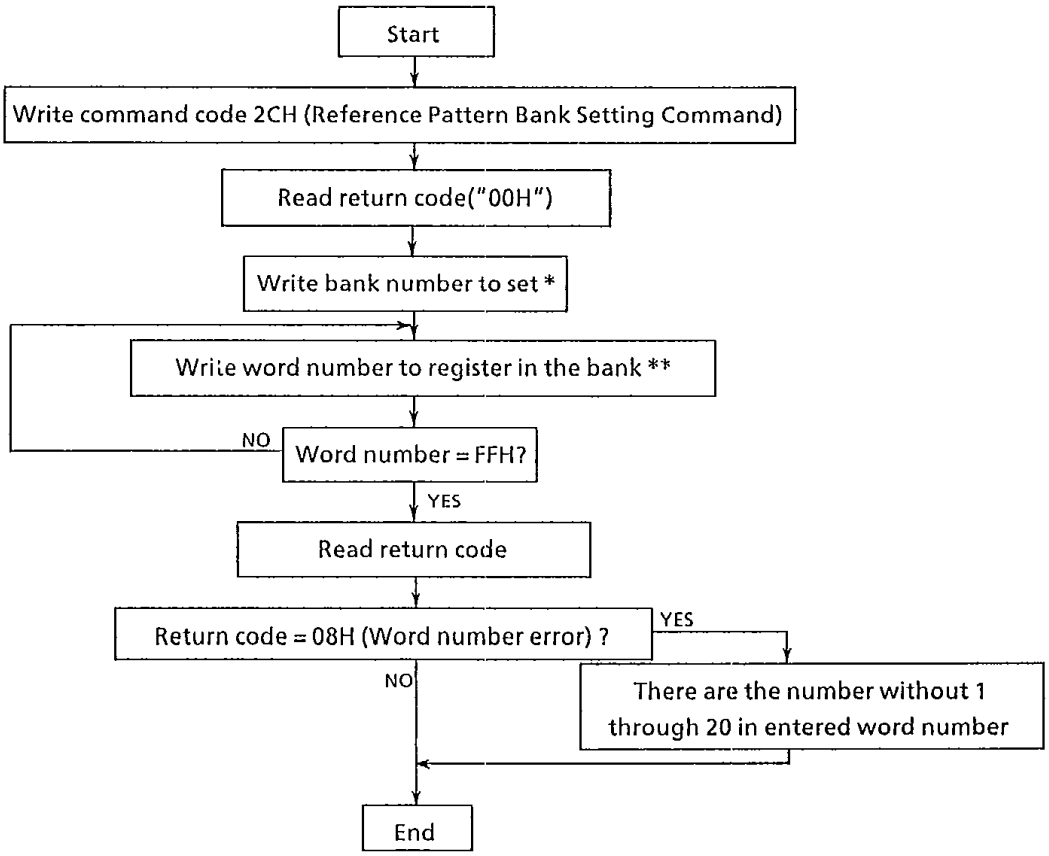
(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents , The host system must check HRRDY and HWRDY before transmission .

5.3.3 (4) Reference Pattern Bank Setting Command (2CH)

This command specifies connection with bank number and word number in each bank , After execution of reference pattern initialization command , whole words in the reference pattern connects with whole bank, After execution of reference pattern bank setting command , at the recognition command , only the registered words in the specified bank become recognition object. Each word in the reference pattern can set multiple bank. For example , word number 2 can set into bank 0 and bank 3 , If the host system write word number FFH right after writing bank number , the bank holds no word and if the host system select this bank at recognition command , error status will be returned.

(1) Flow Chart



* The device set uses lower 3 bit and doesn't check the validity of input data.

** The word number 1 through 20 is available , If the host system enters the number without 1 through 20 , the input data is ignored and the device set returns 08H as word number error .

Fig.5.18 Reference pattern bank setting command flow chart

(2) Timing Chart

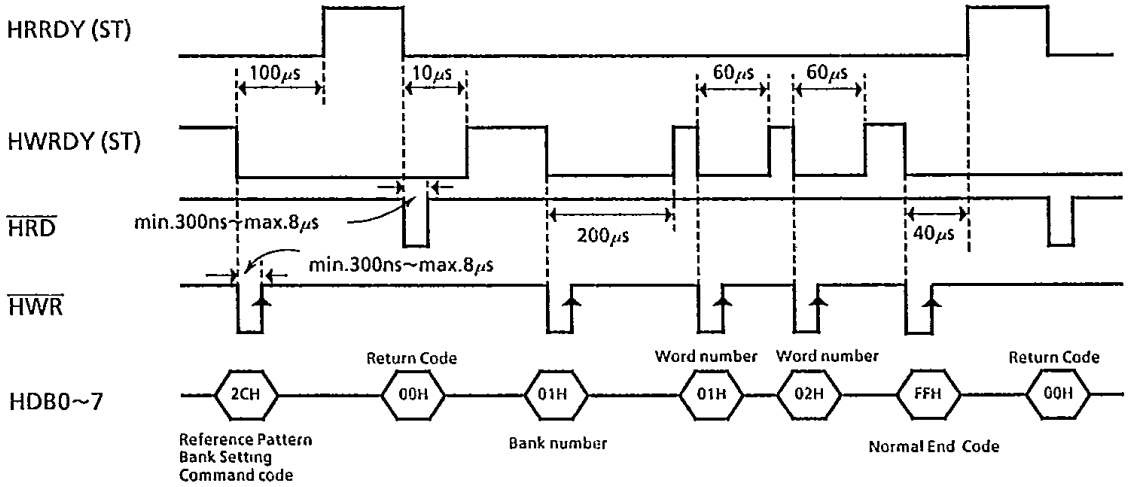


Fig.5.19 Reference pattern bank setting command timing chart

(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred ata contents , The host system must check HRRDY and HWRDY before transmission .

5.3.3 (5) Recognition Command 1,2 (08H~0FH , 18H~1FH)

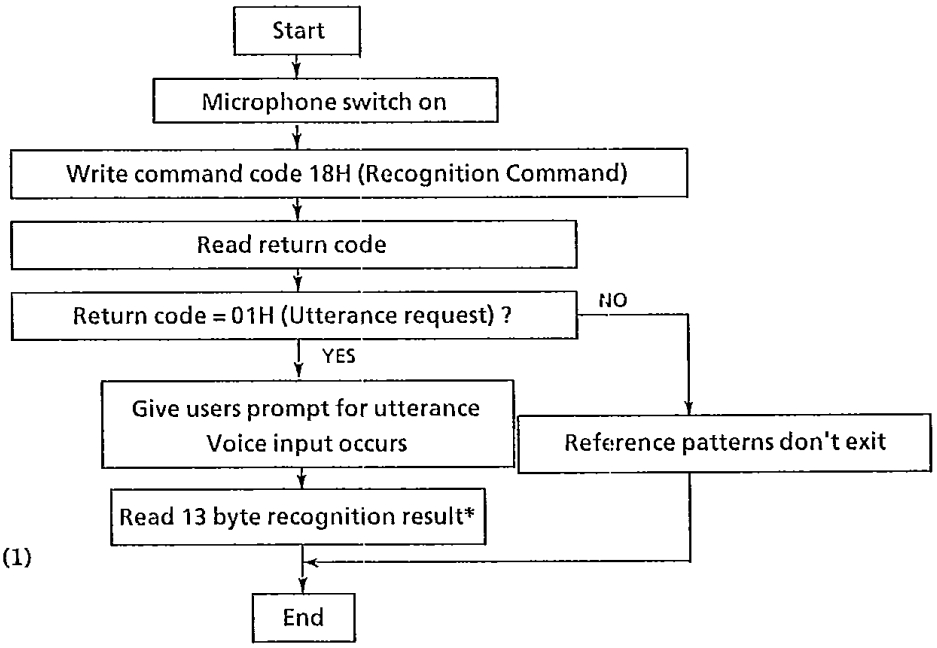
The command performs recognition of input voice on vocabulary reference patterns registered by reference pattern registration command. As a result 13byte data returns back to a host system.

If the reference patterns don't exist (the case happens if any registration has not been executed after reference pattern initialization), the recognition command does not proceed any longer and the device set returns command error code 02H to host system and becomes command waiting state.

The device set has two recognition commands. The device set monitors environmental noise by the different measures. Recognition 1 command (08H~0FH) uses the background noise measured about 1 second before command input to determine a threshold for detecting voice signal. On the other hand recognition 2 command (18H~1FH) uses the environmental noise measured just after command input. Therefore two recognition commands should be used according to environment where the device set uses. Recognition 1 command applies to the case of environmental noise level strongly changes. This command can determine a threshold for detecting voice signal even if the noise level varies to some extent, because the device set uses average noise measured about 1 second. Recognition 2 command applies to the case that environmental noise level is almost regular. Recognition 1 command monitors environmental noise level before this command is entered, so the device set may determines wrong threshold if the user carelessly speaks in this duration.

In recognition 1, 2 command, without bank setting command has executed, all banks contains all reference patterns. Therefore in this case, command code 08H through 0FH or 18H through 1FH is valid. When the bank is correctly assigned by bank setting command, the host system can specify the words in designated bank to recognition object. Specified - bank recognition command code for bank 0 is 08H and 18H, that for bank 1 is 09H and 19H and that for bank 7 is 0FH and 1FH. After reference pattern bank setting command execution, recognition command for the bank which has no reference patterns leads error condition and the device set returns error code.

(1) Flow Chart



* Refer to 5.3.4 (1) Recognition Result Data Format

Fig. 5.20 Recognition command flow chart

Following points must be strictly observed in the procedure until start time point of voice input after waiting recognition command 2. At least 90ms must be needed until starting time point of voice input after return code change to "01H (utterance request)". In this period, the device set determines parameters for detecting voice signal from environment noise signal by monitoring environment noise signal. Therefore a microphone should be operated in this period and a host system forbids users to enter voice to the device set. On the other hand, this 90ms period is suitable for giving users a prompt to start utterance. Even if the prompt is acknowledged by users in the 90ms period, the users utterance period doesn't overlap forbidden period because humans reaction time is over 100ms.

(2) Timing Chart

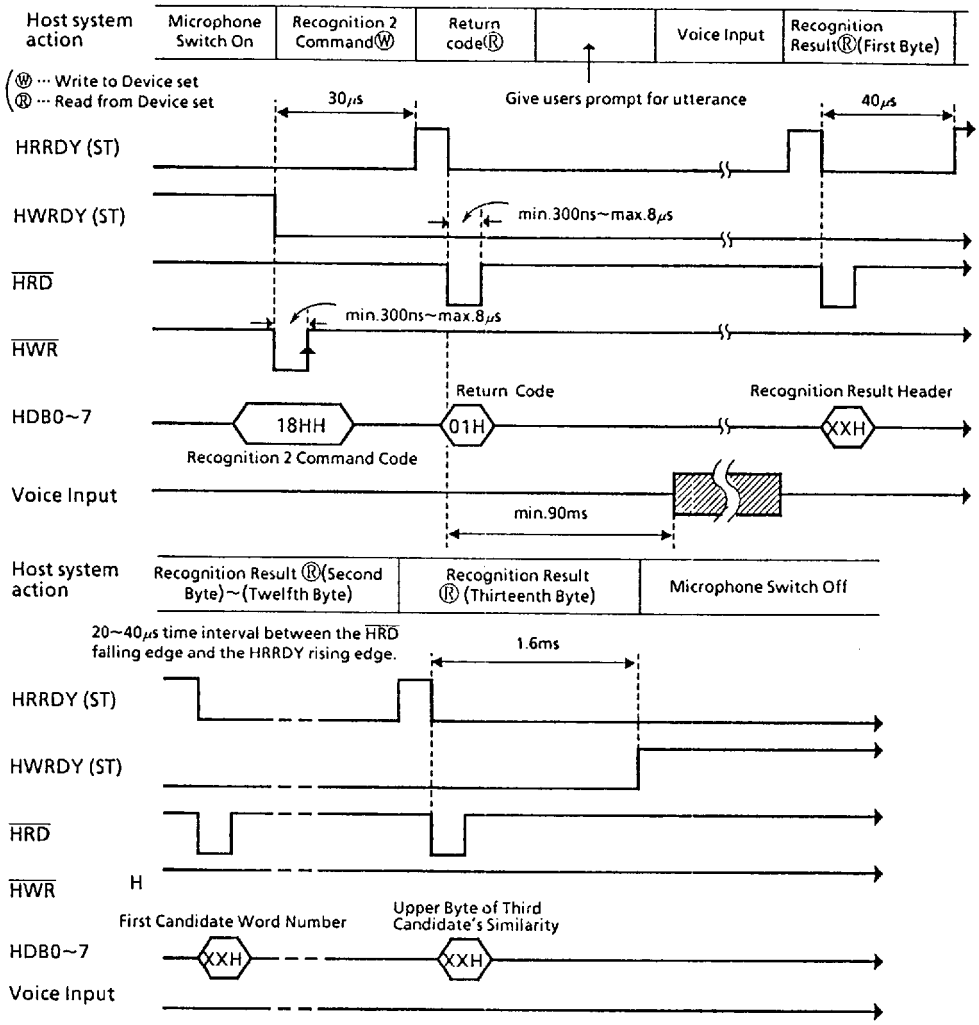


Fig. 5.21 Recognition 2 command timing chart

(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents. The host system must check HRRDY and HWRDY before transmission.

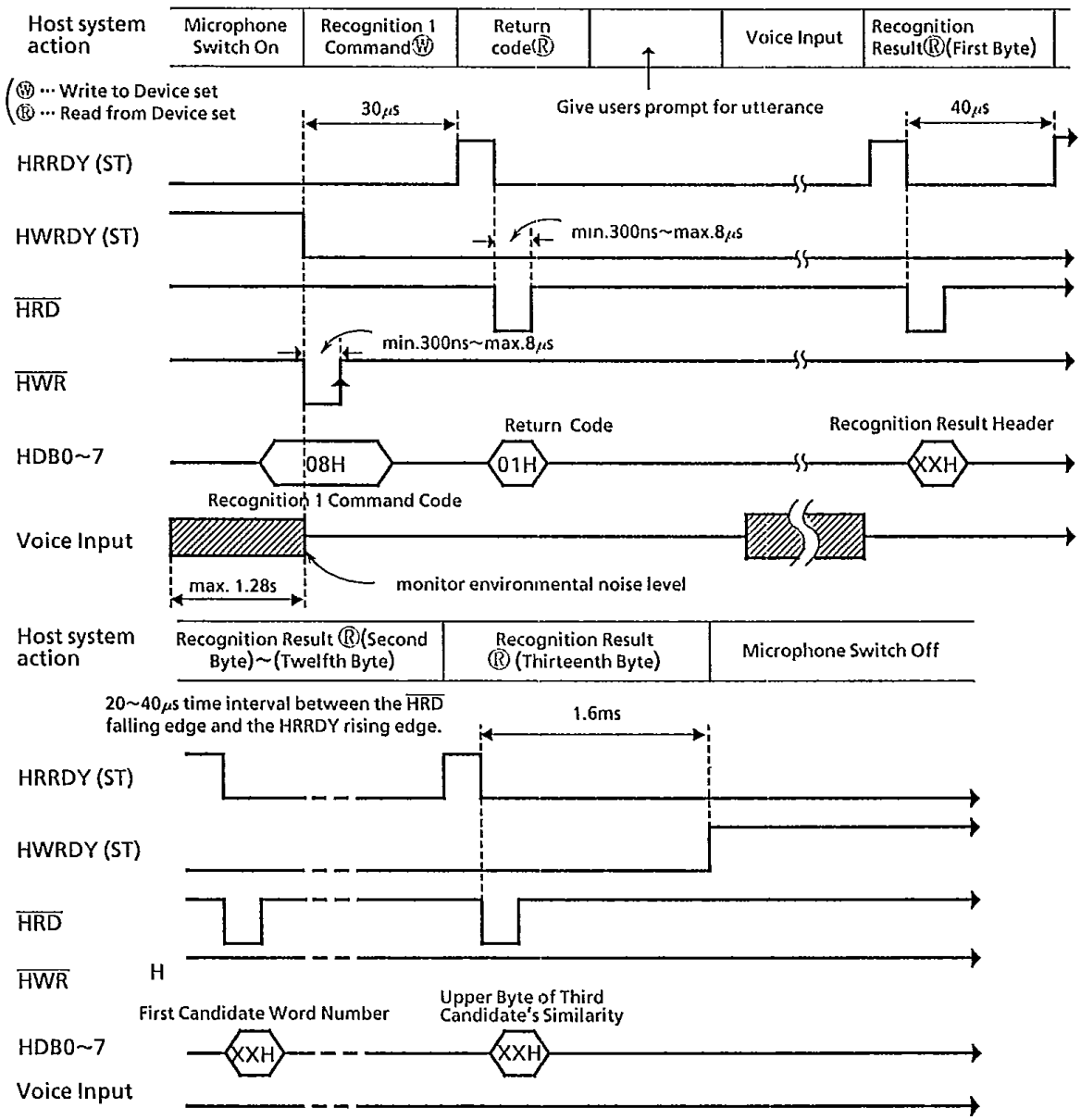


Fig. 5.22 Recognition 1 command timing chart

(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents . The host system must check HRRDY and HWRDY before transmission .

5.3.3 (6) Reference Pattern Down Load Command (22H)

A host system can get reference patterns by reference pattern up load command. When reference patterns already exist in external static RAM, this reference pattern down load command replaces the old reference patterns with patterns transferred from the host system. A reference pattern is transferred in the format described in 5.3.4(4).

(1) Flow Chart

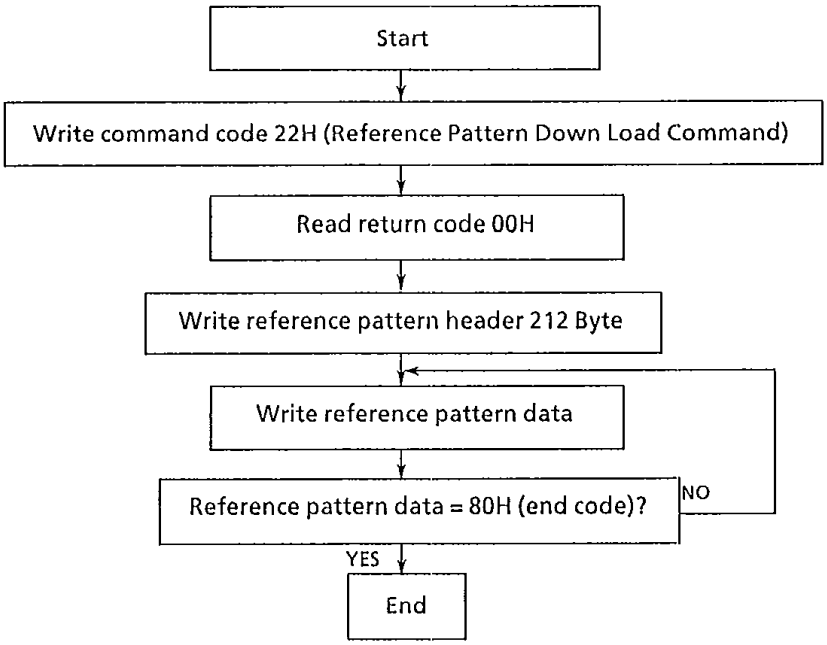
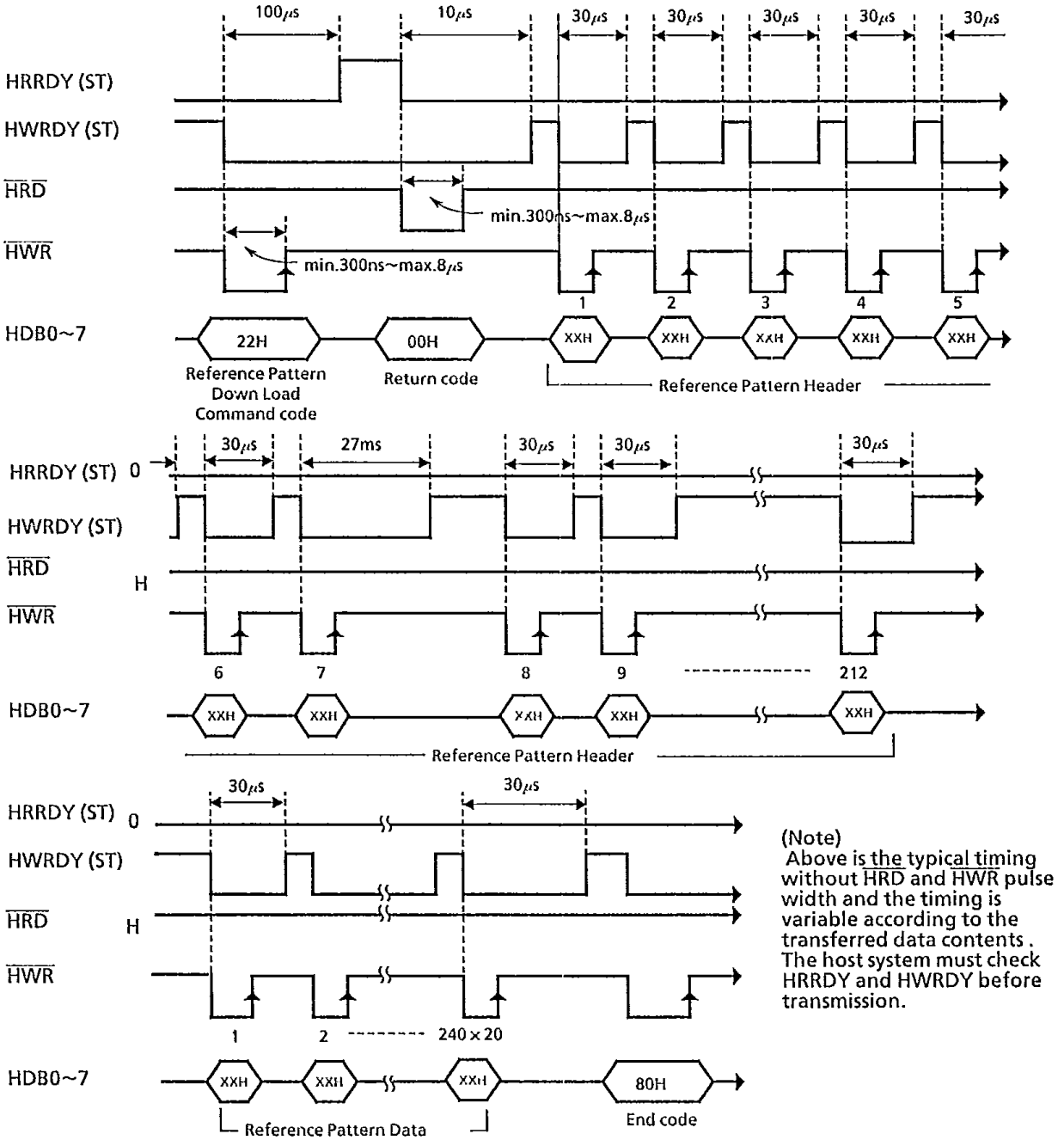


Fig. 5.23 Reference pattern down load command flow chart

(2) Timing Chart



(Note)
Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents. The host system must check HRRDY and HWRDY before transmission.

Fig. 5.24 Reference pattern down load command timing chart

5.3.3 (7) Reference Pattern up Load Command (23H)

This command transfers reference patterns to a host system. Reference patterns are transferred with the format explained in 5.3.4 (4). When there is no reference patterns in a external RAM, this command leads error condition and the device set returns the error code 04H.

(1) Flow Chart

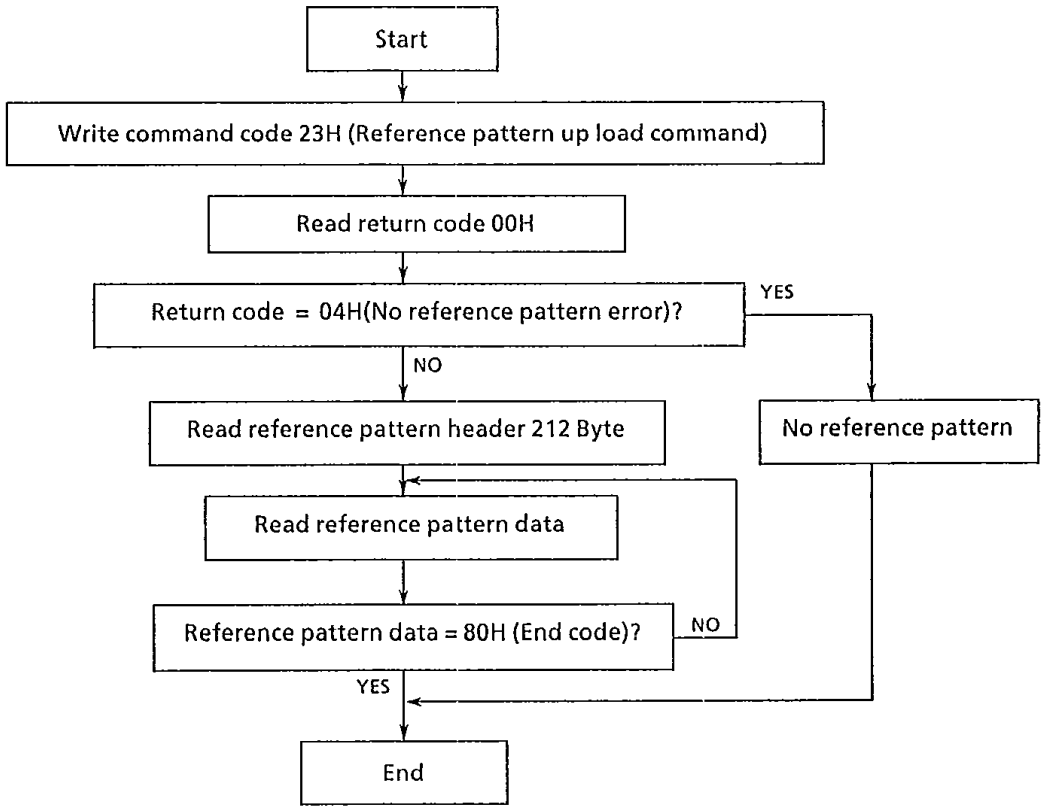


Fig. 5.25 Reference pattern up load command flow chart

(2) Timing Chart

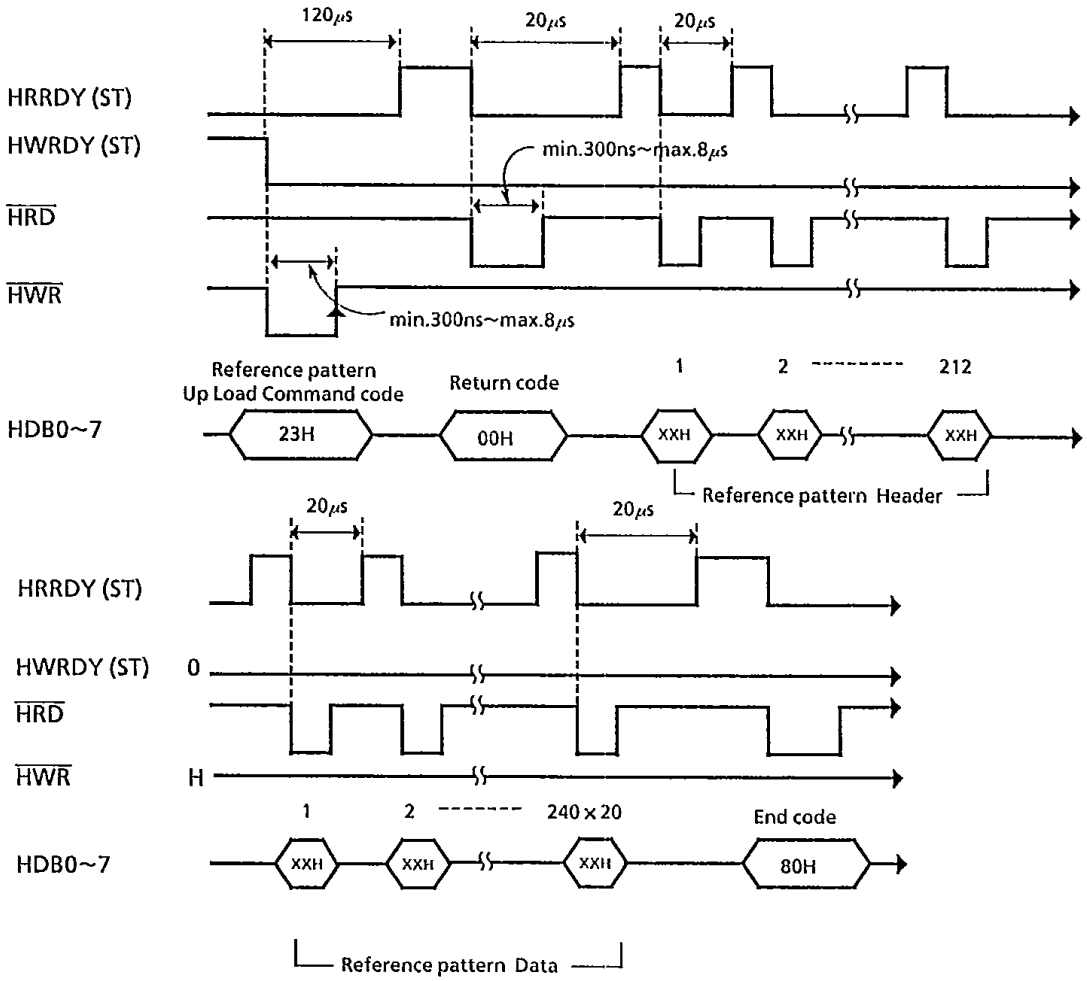


Fig. 5.28 Reference pattern up load command timing chart

(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents . The host system must check HRRDY and HWRDY before transmission.

5.3.3 (8) Reject Level Set up Command (3CH)

The device set tells information about recognition result has low reliability by setting a reject bit in recognition header. The decision whether reject or not is made by comparison similarity and criterion. This criterion is set up by reject level set up command. Initial reject level is set up to 01H by reference pattern initialization command. Available set up value is 00H through 02H and if the other value is entered, the device set becomes command waiting mode. The host system sets up reject level 00H (decrease reject results) through 02H (increase reject results). More details in reject are described at 5.1.5.

(1) Flow Chart

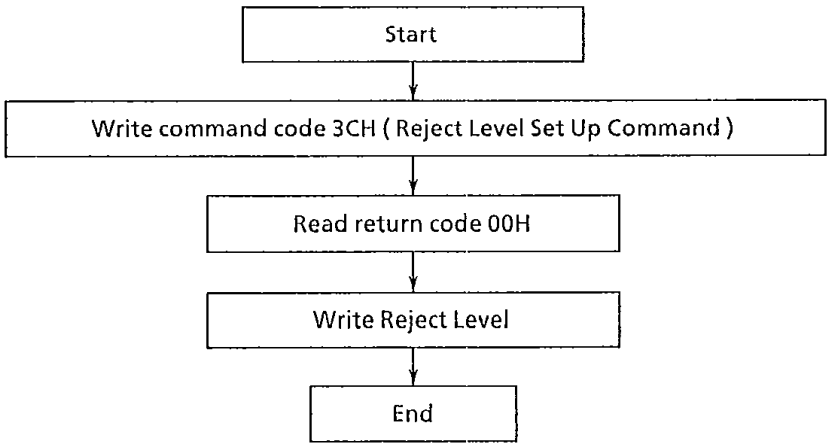


Fig. 5.27 Reject level set up command flow chart

(2) Timing Chart

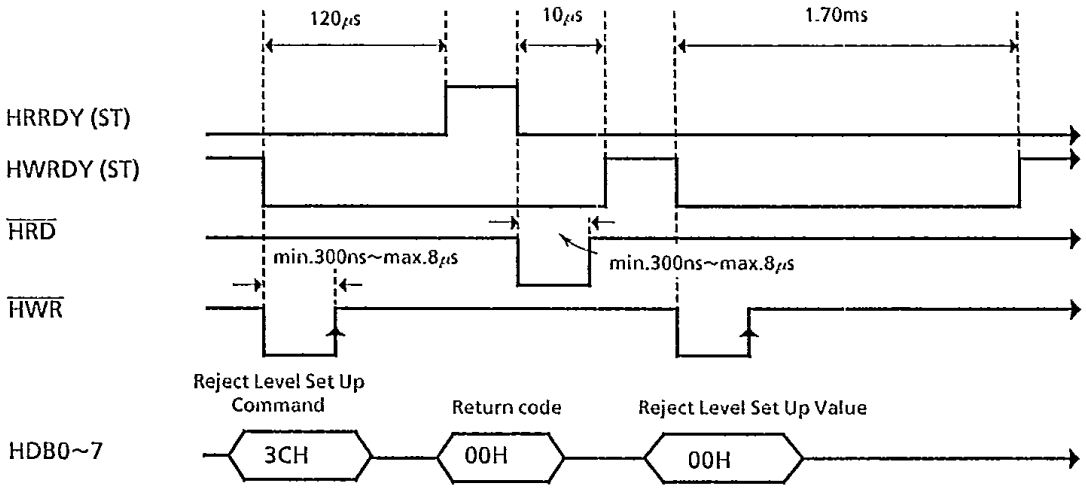


Fig. 5.28 Reject level set up command timing chart

(Note)

Above is the typical timing without $\overline{HRD}$ and $\overline{HWR}$ pulse width and the timing is variable according to the transferred data contents. The host system must check HRRDY and HWRDY before transmission .

5.3.3 (9) System Reset Command , System Stand-by off Command

Reset command is used to release the device set from hung up state to normal operation state. It is also used as a stand-by off command to release the power saving mode when the device is in the mode. In both cases it initializes the device set , but the device set saves all previous data in its scratchpad RAM and its reference pattern RAM. Actual actions are as follows. The command

- Initializes all registers on each device.
- Clears all flags on each device.
- Resets program counter (PC) on TC8865F-01 to 0000H and then starts program from PC=0000H.
- Compensates for TC8861F filter offset.
- Leads the device set to command waiting state.

During these reset command action, status register flag RESET keeps "1". So a host system operates as described below.

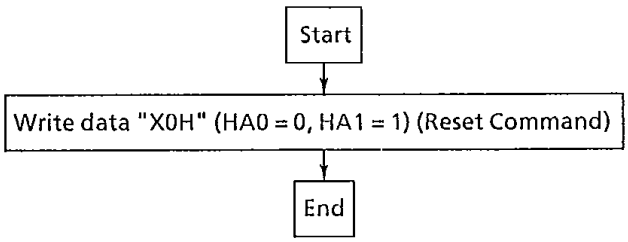


Fig.5.29 Reset command flow chart

5.3.3 (10) System Stand-by on Command (Reset/Stand-by Register)

Stand-by on command leads the device set to power saving mode, where TC8861F, TC8865F-01 hold their system clock to realize total device set power supply current less than 10μA. The command allows the device set to preserve their system parameters on both internal RAMs and external reference pattern RAMs. The mode can be detected by status register flags STBY = 1 and RESET = 1. Note that RESET flag is also 1 in the power saving mode. Stand-by off command releases the device set from power saving mode.

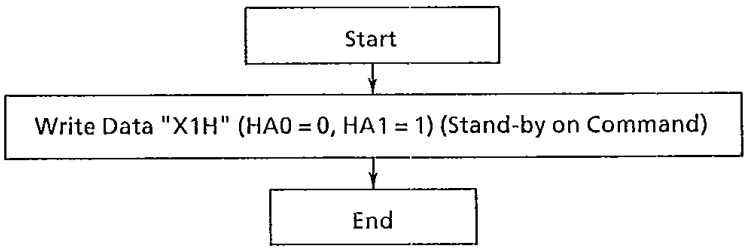


Fig.5.30 Stand-by on command flow chart

5.3.3 (11) Reset Timing

Fig.5.31 shows reset command timing.

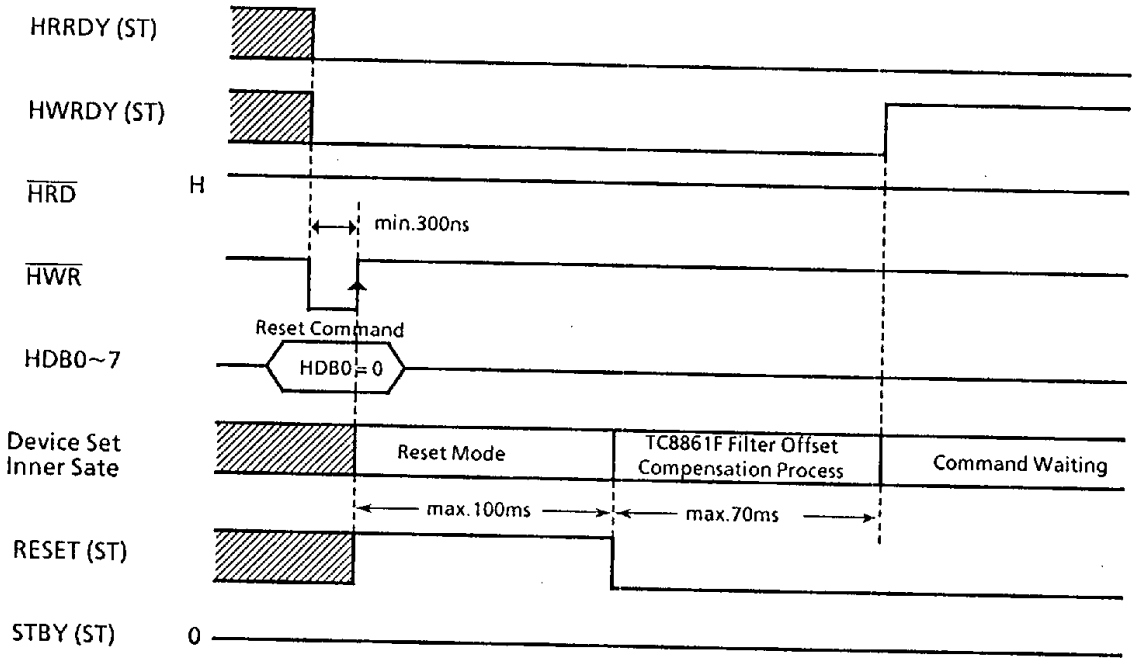


Fig.5.31 Reset timing chart (HA1 = 1, HA0 = 0, $\overline{HCS}$ = 0)

5.3.3 (12) Stand-by on / off Timing

Fig.5.32 shows stand-by on / off command timing.

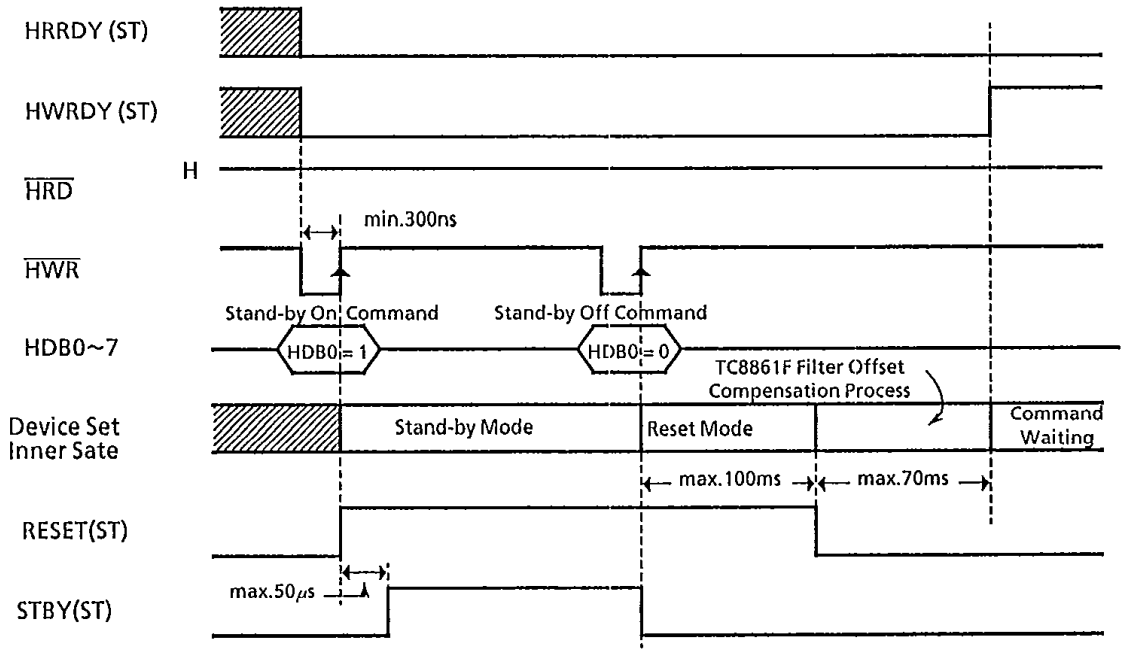


Fig.5.32 Stand-by on / off timing chart (HA1 = 1, HA0 = 0, $\overline{HCS}$ = 0)

5.3.3 (13) System Transition Timing When Power Supply Turns on

Fig.5.33 shows some pin timing when power supply turns on. Even though device set becomes reset mode in the transition period, reset command must be executed once for complete system initialization.

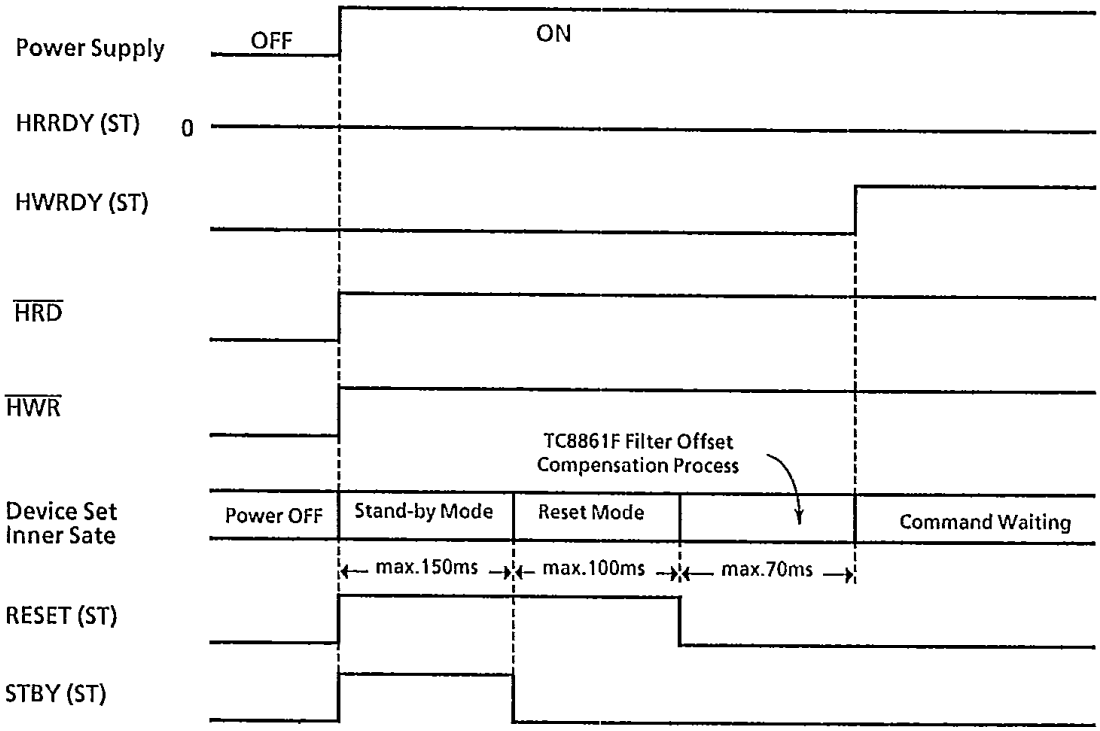


Fig.5.33 System transition timing chart when power supply turns on

5.3.3 (14) Notes on System Reset Command Usage

With a few exceptions stated below, a host system can operates reset command any time even when the device set performs a certain process. The process interrupted by reset command still allows following commands to operate with previous device set operation history alive, because the reset command can preserves essential system parameters of scratch-pad RAM and reference pattern RAM safely. As long as reset command is prohibited execution of in reference pattern registration status register flag DISRST is "1".

This data preservation capability provided by the reset command offers convenience to handle the device set in various applications. Several examples include cases where a host system intends to;

(1) Quit voice input waiting state in recognition command or reference pattern registration command forcefully when the voice will not come in.

(2) Quit infinite loops of recognition command, if it happens.

(3) Stop processes on their way driven by wrong commands.

(4) Recover from hung-up state in host computer program development.

The reset command can be executed in periods other than the prohibit time in reference pattern registration command. In this prohibit time, DISRST bit in status register becomes "1".

5.3.4 Data Format

5.3.4 (1) Recognition Result Data Format

HDB7 (MSB)		HDB0 (LSB)
Recognition Result Header (Refer to description in the next page)		
First Candidate Word Number		
Second Candidate Word Number		
Third Candidate Word Number		
First Candidate Word Similarity Score	(Lower Byte)	
First Candidate Word Similarity Score	(Middle Byte)	
First Candidate Word Similarity Score	(Upper Byte)	
Second Candidate Word Similarity Score	(Lower Byte)	
Second Candidate Word Similarity Score	(Middle Byte)	
Second Candidate Word Similarity Score	(Upper Byte)	
Third Candidate Word Similarity Score	(Lower Byte)	
Third Candidate Word Similarity Score	(Middle Byte)	
Third Candidate Word Similarity Score	(Upper Byte)	13 Bytes Data

Fig.5.34 Recognition result data format

5.3.4 (2) Recognition Result Header Format

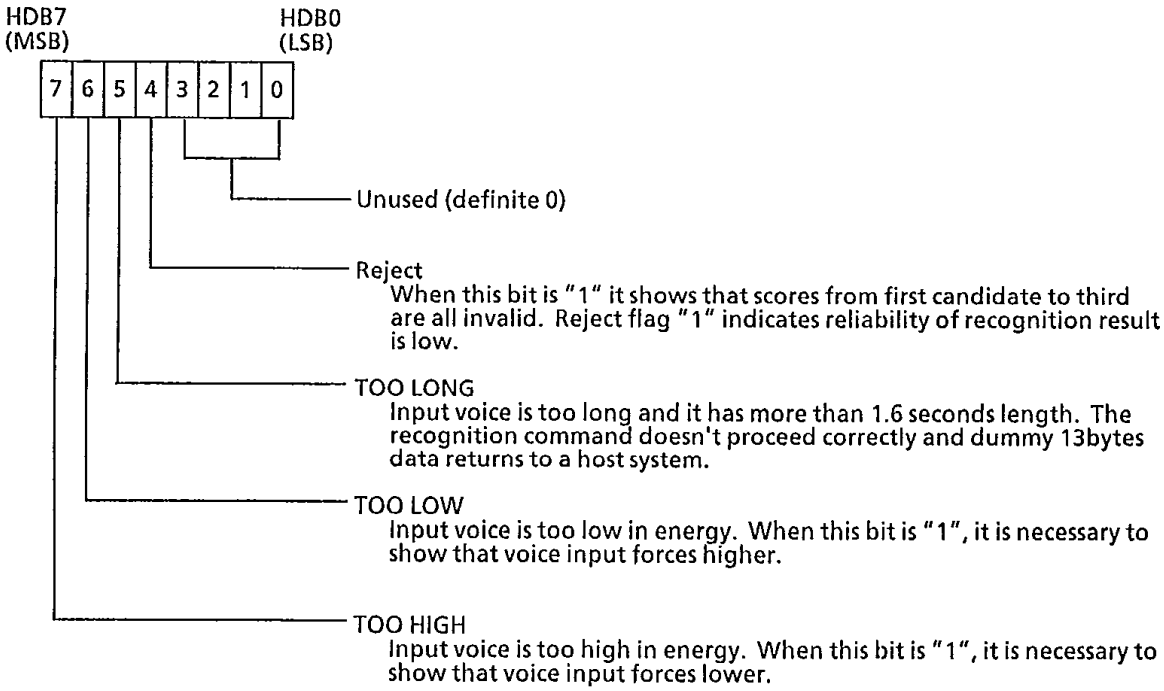


Fig.5.35 Recognition result header format

5.3.4 (3) Return Code Bit Assignment

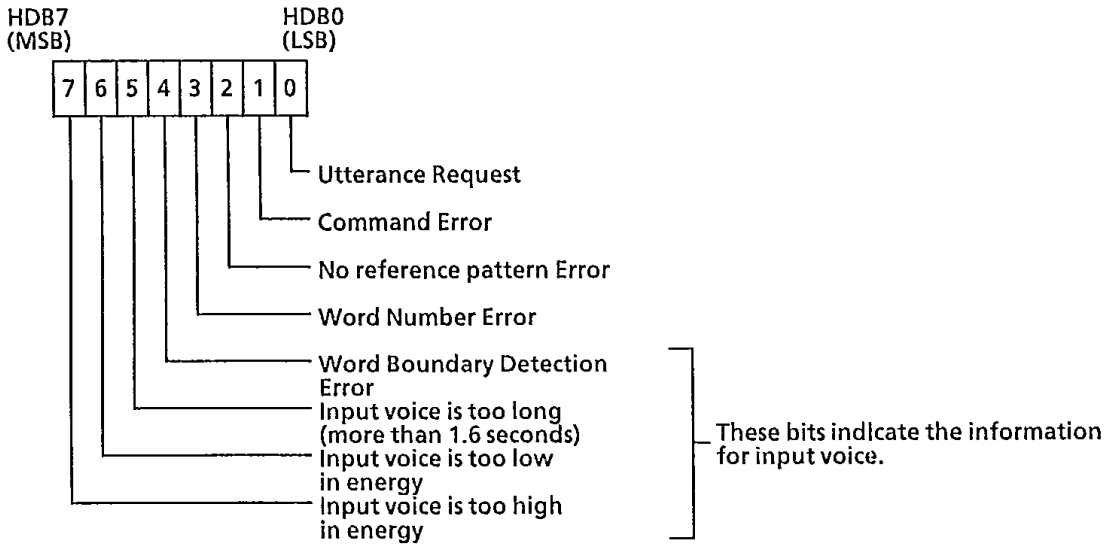


Fig.5.36 Return code bit assignment

5.3.4 (4) Reference Pattern Transfer Format

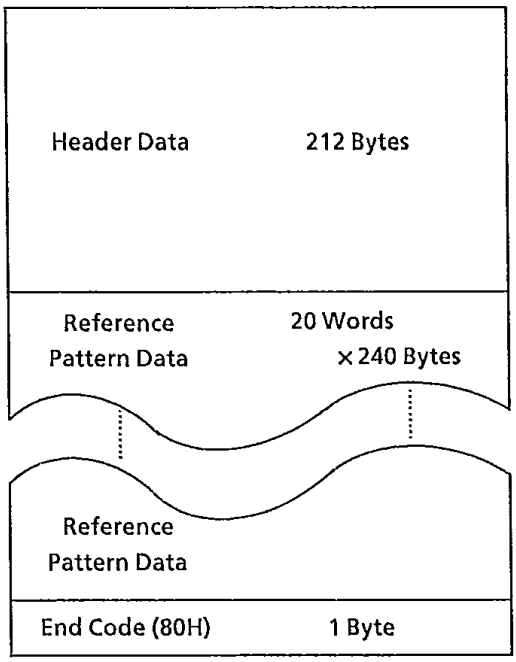


Fig.5.37 Reference pattern format

5.4 Detail Description on Each Device

5.4.1 TC8861F (Acoustic Processing Analog Device)

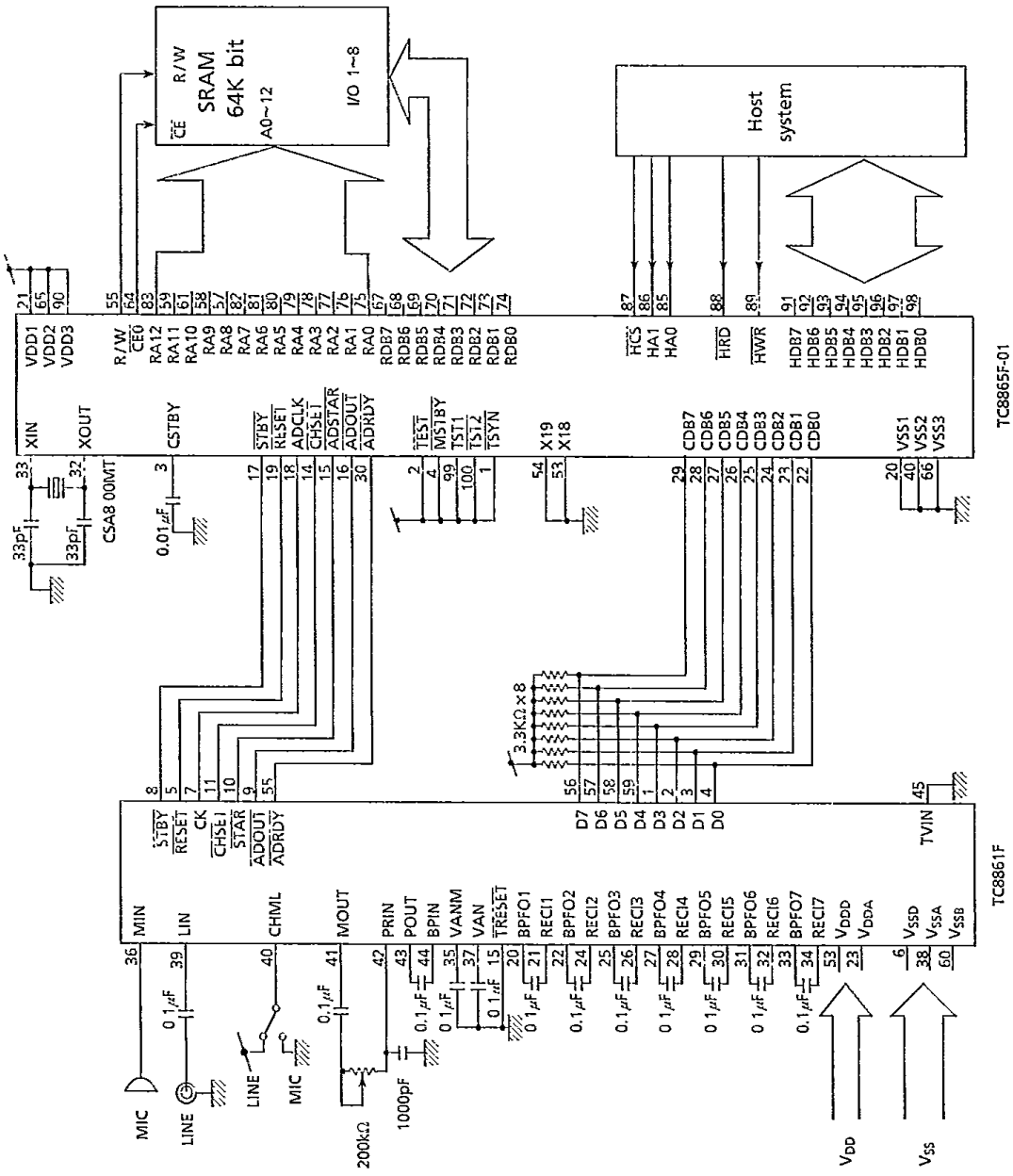
5.4.1 (1) Functional Description and Block Diagram

The device performs acoustic processing for analog voice input signal to prepare acoustic feature extraction parameters. The block diagram is presented in Fig.5.38 and signal processing flow is described in following paragraph.

Analog voice signal fed through either MIN pin or LIN pin is amplified first in either a microphone amplifier (Gain = 26dB) or a line amplifier (Gain = 15dB) and then is amplified again in a preamplifier. The preamplifier gain can vary by a variable resistor (RVI) from 0 dB (RVI = 450kΩ) to 20 dB (RVI = 0kΩ). The amplified signal is then fed to high pass filter (HPF) to emphasize high frequency component in consonant. Next, the signal is input into 7 channel filter bank for frequency analysis. Each filter bank channel consists of a supplementary low pass filter (LPF), a band pass filter (BPF), a rectifier and a smoothing low pass filter. The supplementary LPF and the BPF extracts a portion of signals lying in pass-band of frequency range between f_L and f_H shown in Fig.6.1 BPF block.

Then the rectifier rectifies the BPFed signal in an absolute manner and the smoothing LPF (cut frequency = 50Hz) smooths the rectified signal. Therefore the output from the smoothing LPF represents averaged amplitude time series of waveform in pass-band frequency region uniquely determined for each filter channel.

Single analog-to-digital converter (A/D) digitizes 7 outputs of smoothing LPFs from a multiplexer one by one. The A/D digitizes each channel every 20ms. The input-output digitizing characteristic in the A/D shows non-linearity with 8bit compressed output. The analog input signal full range for the A/D is approximately 2 (V).



* 200kΩ resistor is used for line amplifier. Whereas 50kΩ resistor is better for microphone amplifier.

5.4.1 (2) Method to Wire External Miscellaneous Parts

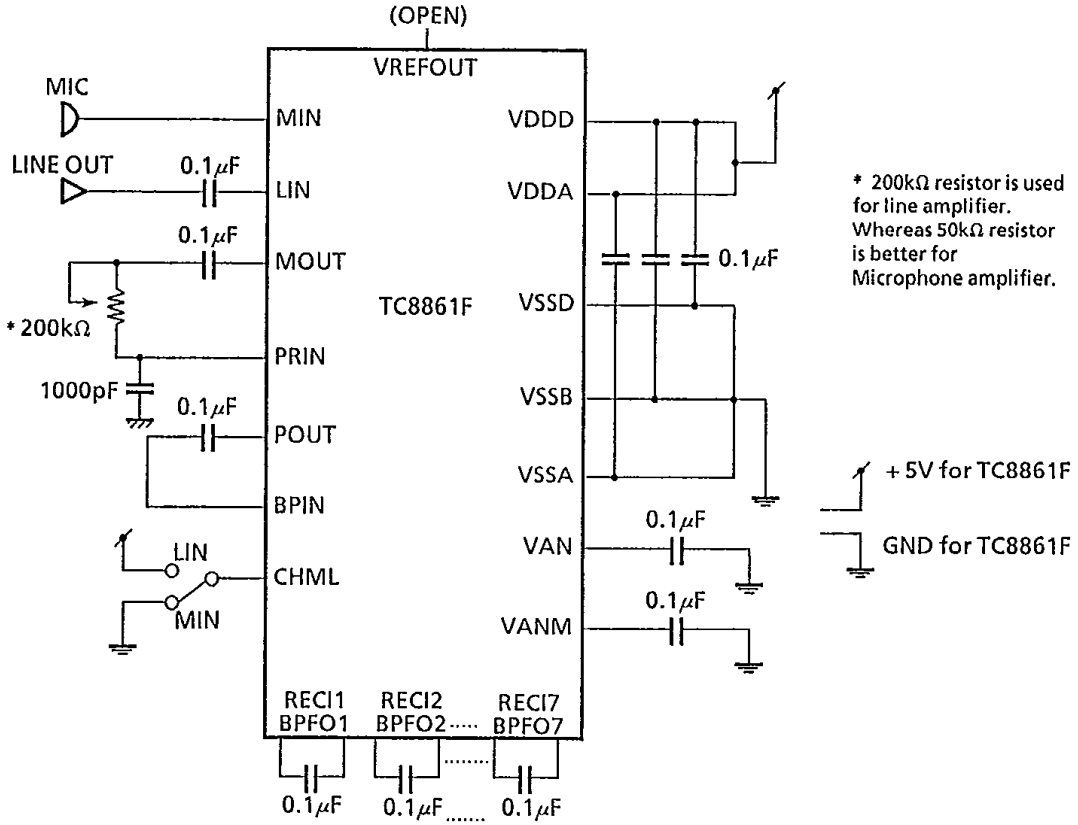


Fig.5.39 Wiring diagram

Because TC8861F is an analog device, special care must be taken of wiring external parts to maintain its analog characteristics. Following cautions must be carefully observed.

(1) Employ either MIN or LIN as an input pin so that input voice may always pass through either microphone amplifier or line amplifier. The reason is that filter offset calibration offered by the device requires one of them to be passed through by input signal.
Otherwise the lack of calibration will lead to degradation in recognition accuracy.

(2) Position a bypass capacitor 0.1μF between power supply pins (VSS-VDD) as close to the pins as possible. Total 3 capacitors should be placed between VDDD-VSSD, VDDD-VSSB, and VDDA-VSSA.

(3) Position VAN and VANM level stabilization capacitors close to the pins.

(4) Use shield wires or pattern wires guard-ringed by GND against disturbing noise for MIN and LIN pins. Also keep away PRIN, BPIN, RECIi (i=1~7), VAN, VANM, and VREFOUT pins from digital high frequency signals.

(5) Place parts between MOUT and PRIN, POUT and BPIN, BPFOi and RECIi (i=1~7) as close to the pins as possible and connect them to the pins with short wires.
Warning! Place certainly a preamplifier stabilizing capacitor 1000pF within ±30% deviation between PRIN and VSSA as close to the pins as possible. Otherwise the device will not operate properly.

5.4.1 (3) Method to Adjust Voice Level

Adjustment of voice level is important to maintain the high recognition performance. Two different stage adjustment are recommended.

(1) Variable Resistor (RVI) Setting: Adjustment by waveform amplitude on POUT.

Appropriate resistance setting on variable resistor (RVI) is usually once required after the device set is implemented in application product. RVI setting covers deviations in operational circumstance factors such as microphone sensitivity, distance between mouth and a microphone, and signal to Noise Ratio on MIN or LIN. Therefore it should not usually be done more than once after device set installation.

Concrete explanation about the setting is presented in the following: The criteria of appropriate setting is offered in such a way that maximum waveform amplitude of voice on POUT with analog GND 1/2 VDD (VDD: Supply power voltage) is equal or slightly more than full-range of GND-VDD. Although slight clipping of the signal on POUT due to a little louder voice do no harm, both too much clipping due to extremely loud voice and too little waveform due to too small voice reduces recognition performance.

An experiment with Japanese word "HAI", meaning "YES" in English, shows an equation about relationship between RVI value R (kΩ) and MIN or LIN maximum waveform amplitude X(mVp-p)or Y(mVp-p)producing full-range waveform on POUT as follows:

On MIN Pin:

$$X\,(\mathrm{mVp\text{-}p}) = 70\,(\mathrm{mVp-p}) \times \frac{\frac{500\mathrm{k}\Omega}{75\mathrm{k}\Omega+50\mathrm{k}\Omega}}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}} = 70\,(\mathrm{mVp-p}) \times \frac{4}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}}$$

On LIN Pin:

$$Y\,(\mathrm{mVp\text{-}p}) = 70\,(\mathrm{mVp-p}) \times \frac{4}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}} \times \frac{20\,(\mathrm{times})}{5.6\,(\mathrm{times})}$$

Table 5.6 indicates value relationships between R and X or between R and Y. Note that values indicated in the table are standard and will vary according to vocabulary.

Table 5.6 Relationship of values between R and X or between R and Y

R (kΩ)	X (mV_{p-p}) on MIN Pin	Y (mV_{p-p}) on LIN Pin
0	28	100
25	42	150
75	70	250
125	98	350
175	126	450
450	280	1000

Evaluation experience recommends around 15kΩ as R for condenser microphone.

(2) Input Voice Energy Flag in Recognition Result Header

Input voice energy flag mainly covers voice level deviation of individual utterance given by personal characteristics, like male or female. The flag is embedded in a 1byte recognition result header returned to a host system on recognition command execution. (See 5.3.4(2) Recognition Result Header Format.) Upper 2bits of the header categorize the level of voice just recognized in two stages (too low, OK). Indication of this 2bit information to users helps better input voice level setting for next recognition.

5.4.1 (4) Threshold for Word Boundary Detection

Word boundary detection threshold is used to determine valid voice signal period. Input signals with level exceeding the threshold, lasting over a certain period of time, is picked up as valid voice. The detection is followed by pattern matching activity.

The device set adaptively determines the threshold by monitoring background noise level when no voice exists, and changes the threshold level from '8H' (about 16mV) through '47H' (142mV) according to background noise. It sets lower threshold for lower background noise and higher threshold for higher background noise.

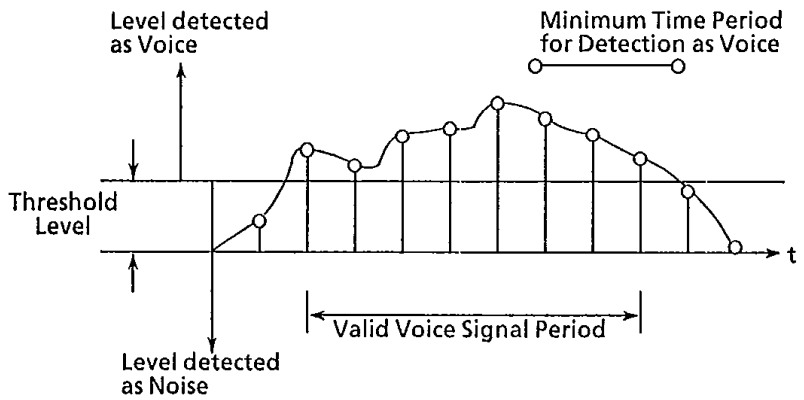


Fig.5.40 Word boundary detection scheme

5.4.1 (5) Remarks on Power Supply

Since TC8861F is an LSI with the analog circuit built in, its analog characteristics may be adversely affected by the noise of a power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate a power supply to TC8861F from that to other LSI's (TC8865F-01, Host System and other LSI's). (2 power supplies)
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the other power supply GND to the power supply GND of TC8861F.
- The power supply for TC8861F should have as less ripple as possible and a series regulator power supply is recommended for the best condition. If a switching regulator power supply is used, it should be stabilized by the three-pin regulator such as TA78DS05P. An example of a circuit, when a power supply is composed of a combination of a switching regulator power supply and a three-pin regulator, is shown below.

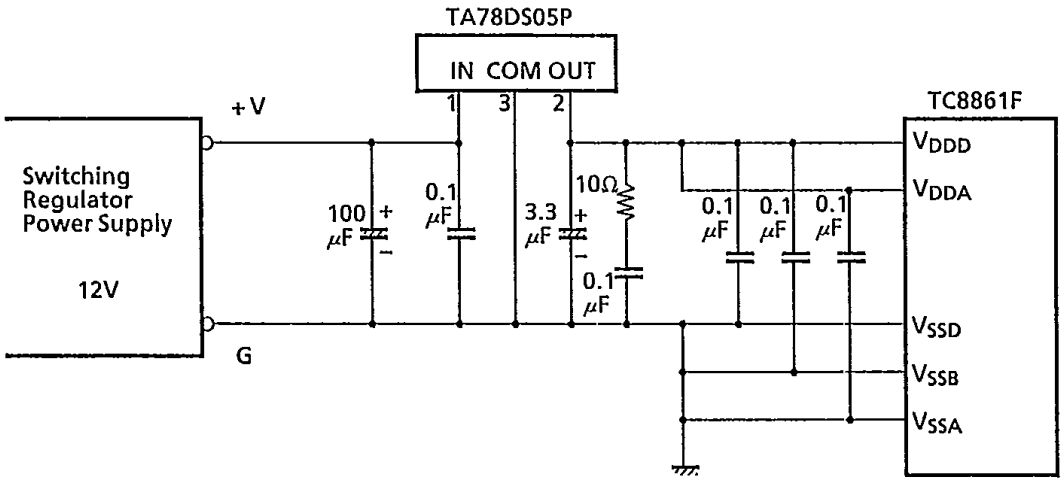


Fig.5.41 Recommended power supply circuit for TC8861F

5.4.2 TC8865F-01

(1) Method to Wire External Static ram

TC8865F-01 is used with a 64K bit static RAM as external memory. Method of wiring external memory is displayed at Fig.5.42.

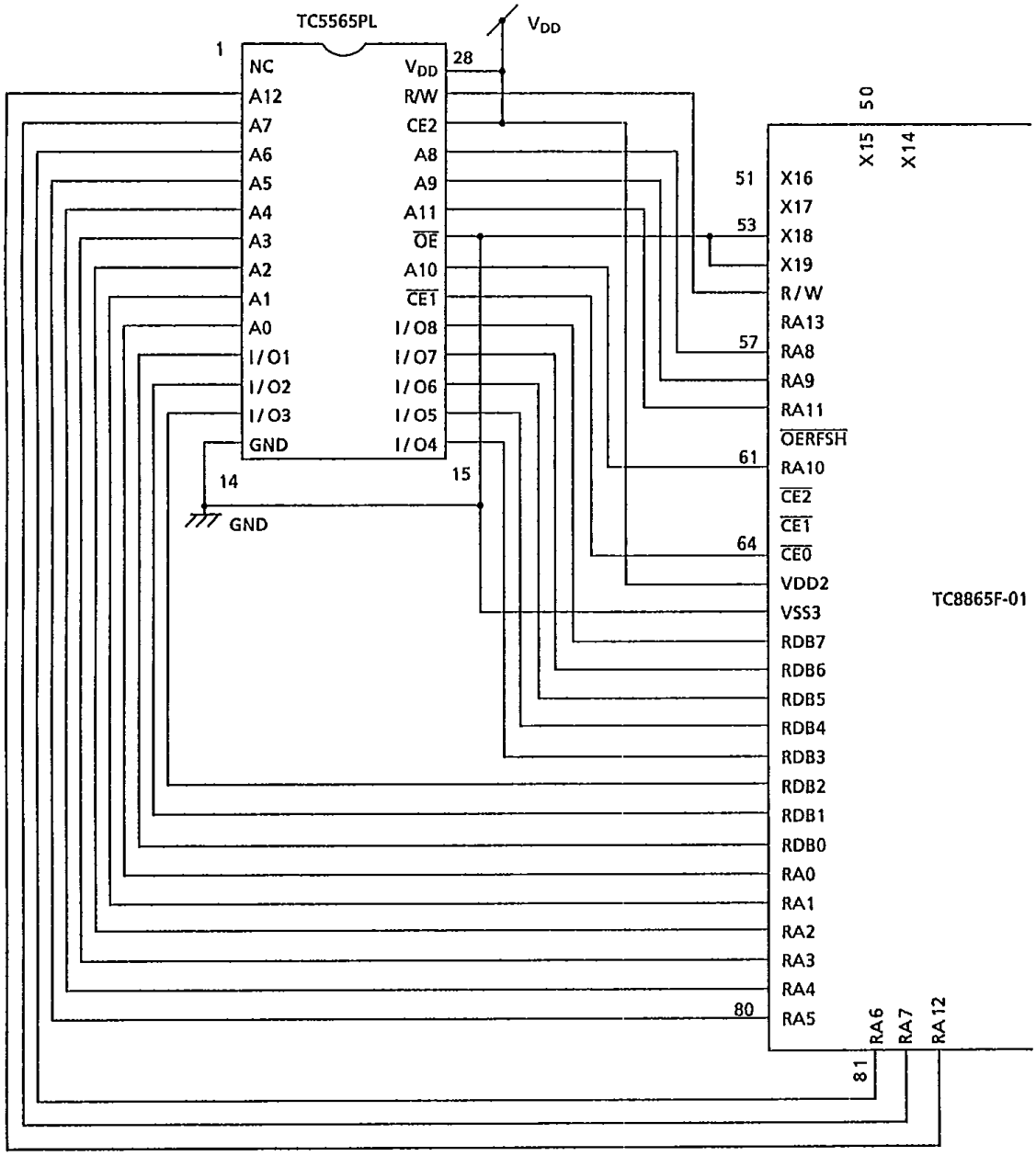


Fig.5.42 External memory wiring diagram

(2) Oscillation Circuit

TC8865F-01 obtains built-in oscillation circuit. Connect ceramic resonator and capacitors to XIN and XOUT pins. When clock is supplied from external circuit, connect this clock signal to XIN pin and don't connect any signal to XOUT pin.

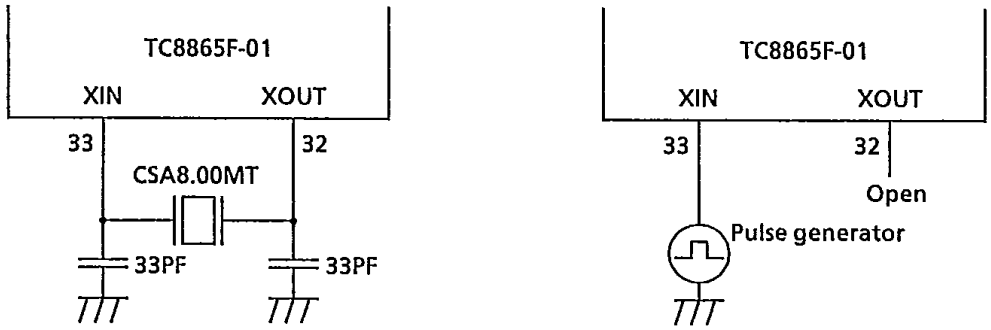


Fig.5.43 Oscillation circuit

(3) Method to Wire External Parts

Connect 0.01μF capacitor to CSTBY pin for making startup timing.

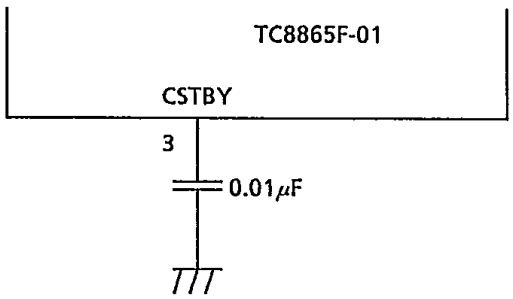


Fig.5.44 External parts

6. ELECTRICAL CHARACTERISTICS

6.1 TC8861F

6.1.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~+6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Output Voltage	V_{OUT}	−0.3~V_{DD}+0.3	V
Storage Temperature	T_{stg}	−55~+125	°C

6.1.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{DD}	V
Output Voltage	V_{OUT}	0~V_{DD}	V
Operating Frequency	f_{CLK}	1.9~2.1	MHz
Operating Temperature	T_{opr}	-10~+70	°C

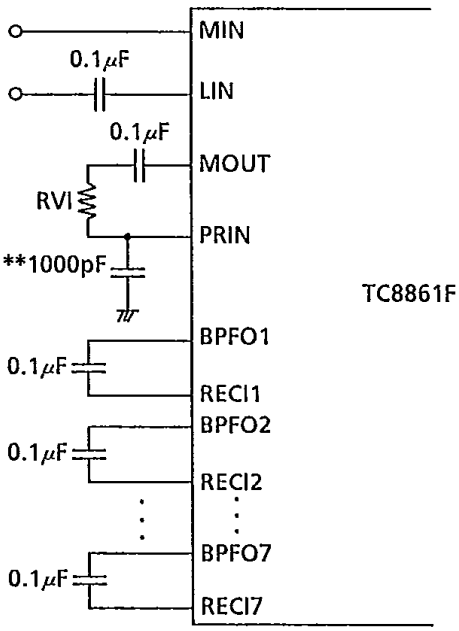
6.1.3 DC Characteristics (VDD = +5.0V ± 10%, Topr = -10 ~ +70°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Input Low Voltage		V_{IL}		–	–	0.8	V
Input High Voltage	D0~D7	V_{IH}		2.2	–	–	V
	Other than bove			VDD-0.8	–	–	
Input Low Current		I_{IL}	V_{IN} = 0V	–	–	−5	μA
Input High Current		I_{IH}	V_{IN} = V_{DD}	–	–	5	μA
Output Low Current		I_{OL}	V_{OUT} = 0.4V	1.76	–	–	mA
Output High Current		I_{OH}	V_{OUT} = V_{DD} − 0.4V	−0.44	–	–	mA
Supply Current (1)		I_{DD-OPR}	When A to D Converter not operating	–	13	25	mA
Supply Current (2)		$I_{DD-STBY}$	At stand-by state	–	–	3	μA

6.1.4 Analog Input Pin (VDD = +5.0V ± 10%, T_{opr} = -10~ +70°C)

ITEM		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Allowable input	MIN	V_{in}	RVI* = 0kΩ f = 1kHz	–	–	28	mVp-p
	LIN		RVI* = 75kΩ f = 1kHz	–	–	250	
Input Resistance	MIN	R_{in}	f = 1KHz	–	100	–	KΩ
	LIN			–	100	–	

* Condition: The following parts wiring scheme is employed.



** 1000pF capacitor is essential for normal operation

Fig.6.1 Wiring diagram

6.2 TC8865F-01

6.2.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~+6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Output Voltage	V_{OUT}	−0.3~V_{DD}+0.3	V
Storage Temperature	T_{stg}	−55~+125	°C

6.2.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{DD}	V
Output Voltage	V_{OUT}	0~V_{DD}	V
Operating Frequency	f_{CK}	7.6~8.4	MHz
Operating Temperature	T_{opr}	-10~+70	°C

6.2.3 DC Characteristics (VDD = +5.0V ± 10%, Topr = -10~+70°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	–	V
Input Low Current	I_{IL}	V_{IN} = 0V	–	–	−5	μA
Input High Current	I_{IH}	V_{IN} = V_{DD}	–	–	5	μA
Output Low Current	I_{OL}	V_{OUT} = 0.4V	1.76	–	–	mA
Output High Current	I_{OH}	V_{OUT} = V_{DD} − 0.4V	−0.44	–	–	mA
Supply Current (1)	I_{DD-OPR}	In no access state	–	20	30	mA
Supply Current (2)	$I_{DD-STBY}$	In stand-by state	–	–	3	μA

6.3 AC Characteristics (V_{DD} = +5.0V ± 10%, f_{CK} = 8MHz, Topr = -10~ + 70°C, CL = 50PF

6.3.1 Host System I/F Reading Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HRD}$ Pulse Width	t_{HRR}		300	–	8000	ns
Address Setup Time	t_{HAR}		0	–	–	ns
Output Delay Time	t_{HRD}		–	–	200	ns
Address Hold Time	t_{HRA}		0	–	–	ns
Output Disable Time	t_{HDF}		10	–	100	ns

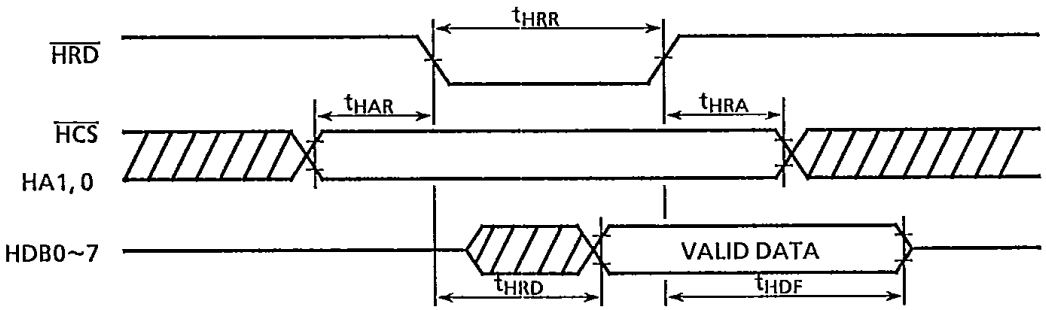


Fig. 6.3 Reading cycle timing diagram on TC8865F-01 host interface

6.3.2 Host System I/F Writing Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HWR}$ Pulse Width	t_{HWW}		300	–	8000	ns
Address Setup Time	t_{HAW}		0	–	–	ns
Data Setup Time	t_{HDW}		120	–	–	ns
Address Hold Time	t_{HWA}		0	–	–	ns
Data Hold Time	t_{HWD}		30	–	–	ns

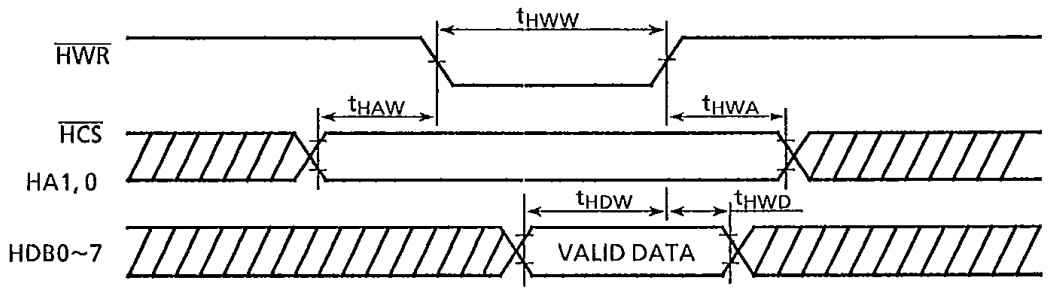


Fig. 6.4 Writing cycle timing diagram on TC8865F-01 host interface

(3) External Memory I/F Reading Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{CE}$ Pulse Width	t_{RCC1}	f_{CK} = 8MHz	500	–	600	ns
Address Setup Time	t_{RAE}	f_{CK} = 8MHz	35	–	–	ns
Address Hold Time	t_{ROA}	f_{CK} = 8MHz	50	–	–	ns
Data Setup Time	t_{RRS}	f_{CK} = 8MHz	300	–	–	ns
Data Hold Time	t_{RRH}	f_{CK} = 8MHz	0	–	–	ns

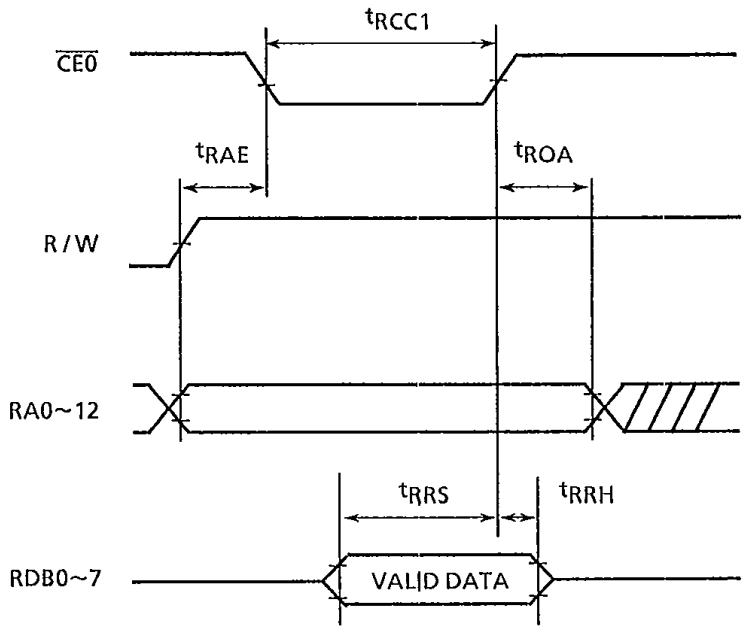


Fig. 6.5 Reading cycle timing diagram on TC8865F-01 external memory interface

(4) External Memory I/F Writing Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{CE}$ Pulse Width	t_{RCC2}	f_{CK} = 8MHz	500	–	600	ns
R/W→$\overline{CE}$ Delay Time	t_{REW}	f_{CK} = 8MHz	0	–	–	ns
R/W Pulse Width	t_{RWW}	f_{CK} = 8MHz	200	–	–	ns
R/W→$\overline{CE}$ Delay Time	t_{RWE}	f_{CK} = 8MHz	0	–	–	ns
Address Setup Time	t_{RAW}	f_{CK} = 8MHz	180	–	–	ns
Address Hold Time	t_{RWA}	f_{CK} = 8MHz	100	–	–	ns
Data Setup Time	t_{RDW}	f_{CK} = 8MHz	0	–	–	ns
Data Hold Time	t_{RWD}	f_{CK} = 8MHz	1000	–	–	ns

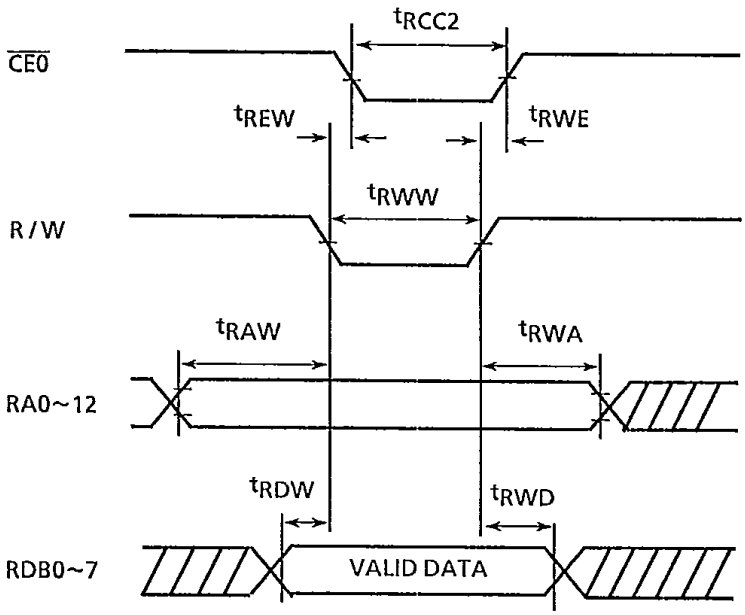


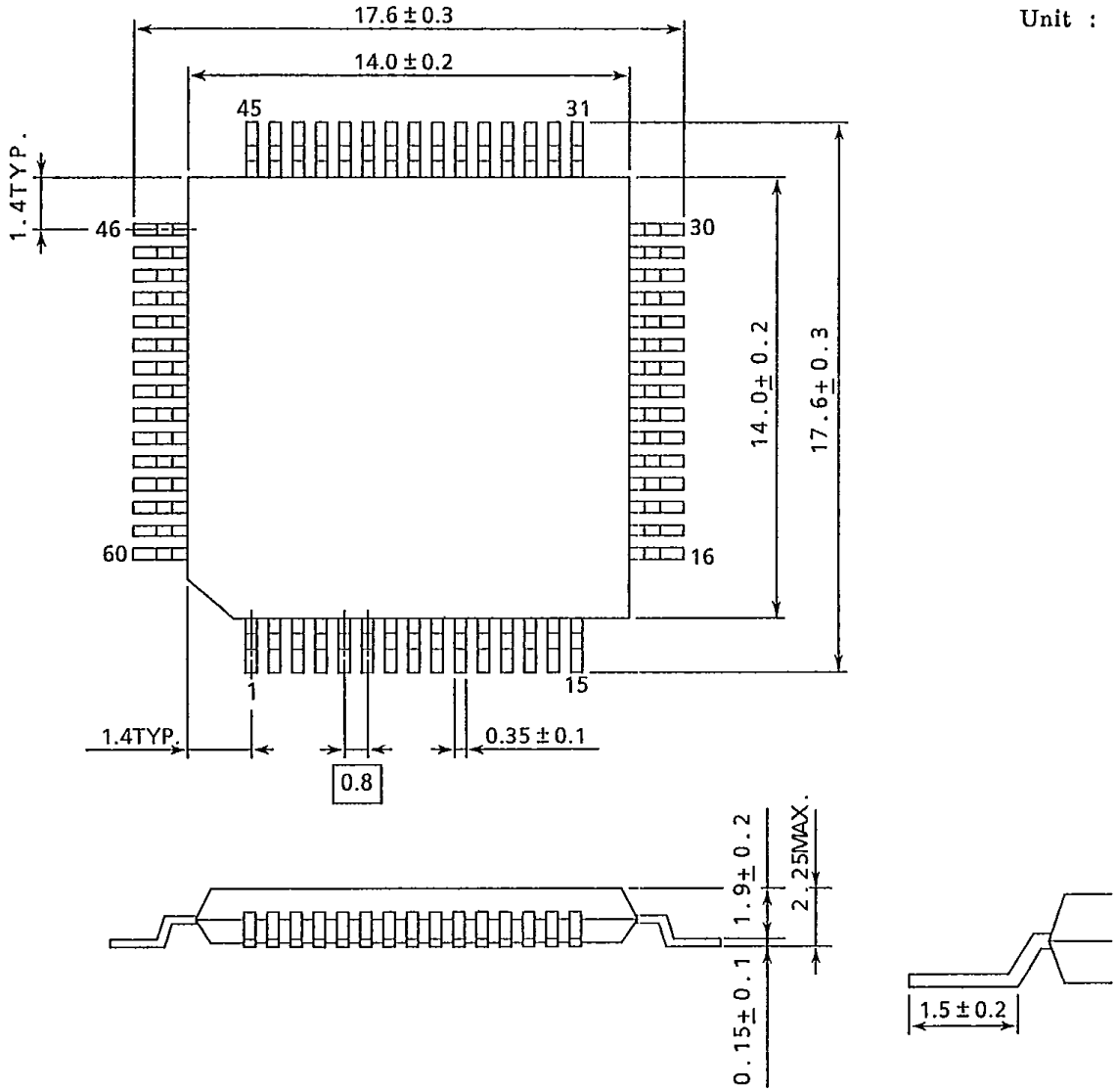
Fig. 6.6 Writing cycle timing diagram on TC8865F-01 external memory interface

7. OUTLINE DRAWING

7.1 TC8861F

60-pin Mini-Flat Package (QFP60-P-1414A)

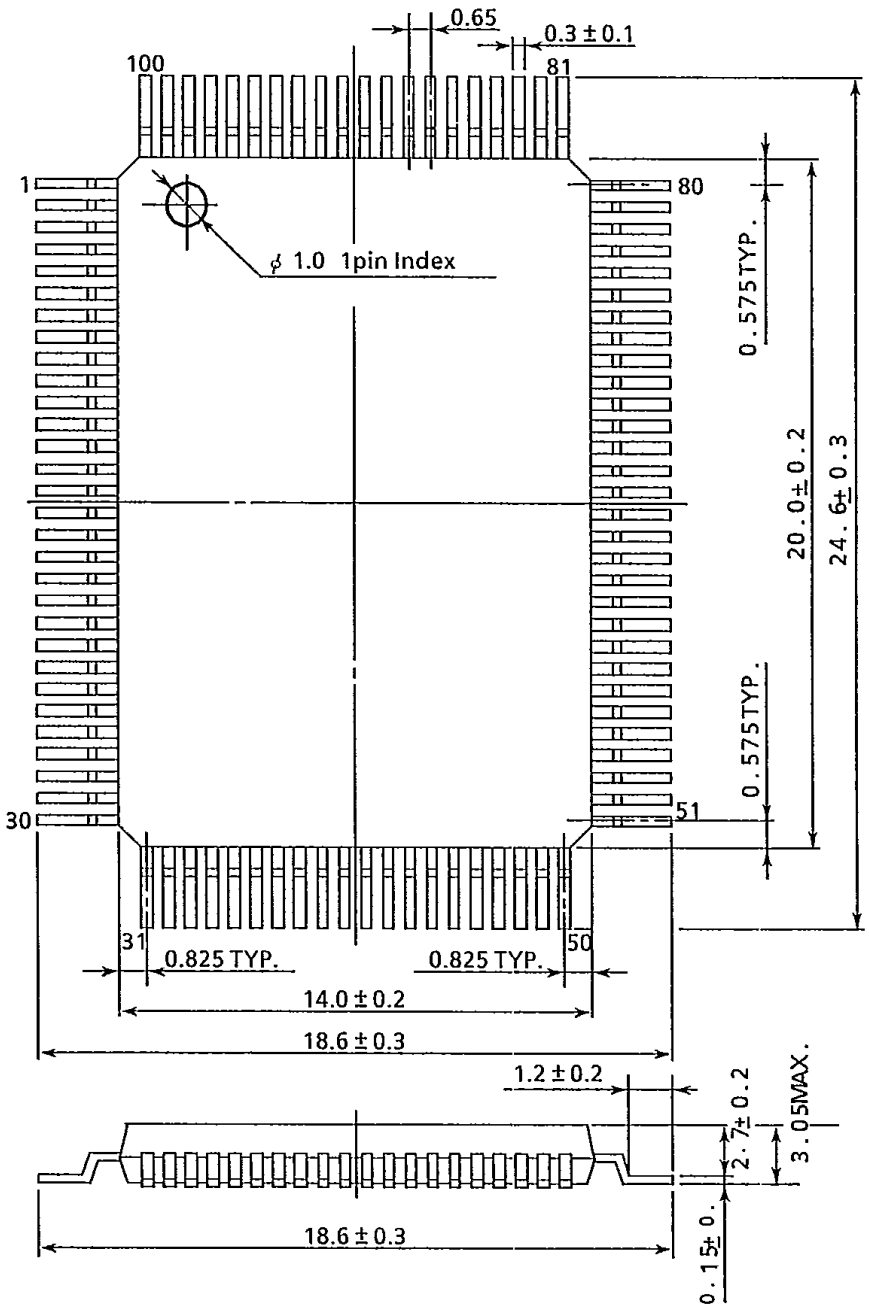
Unit : mm



7.2 TC8865F-01

100-pin Flat Package (QFP100-P-1420)

Unit : mm



8. APPLICATION CIRCUIT

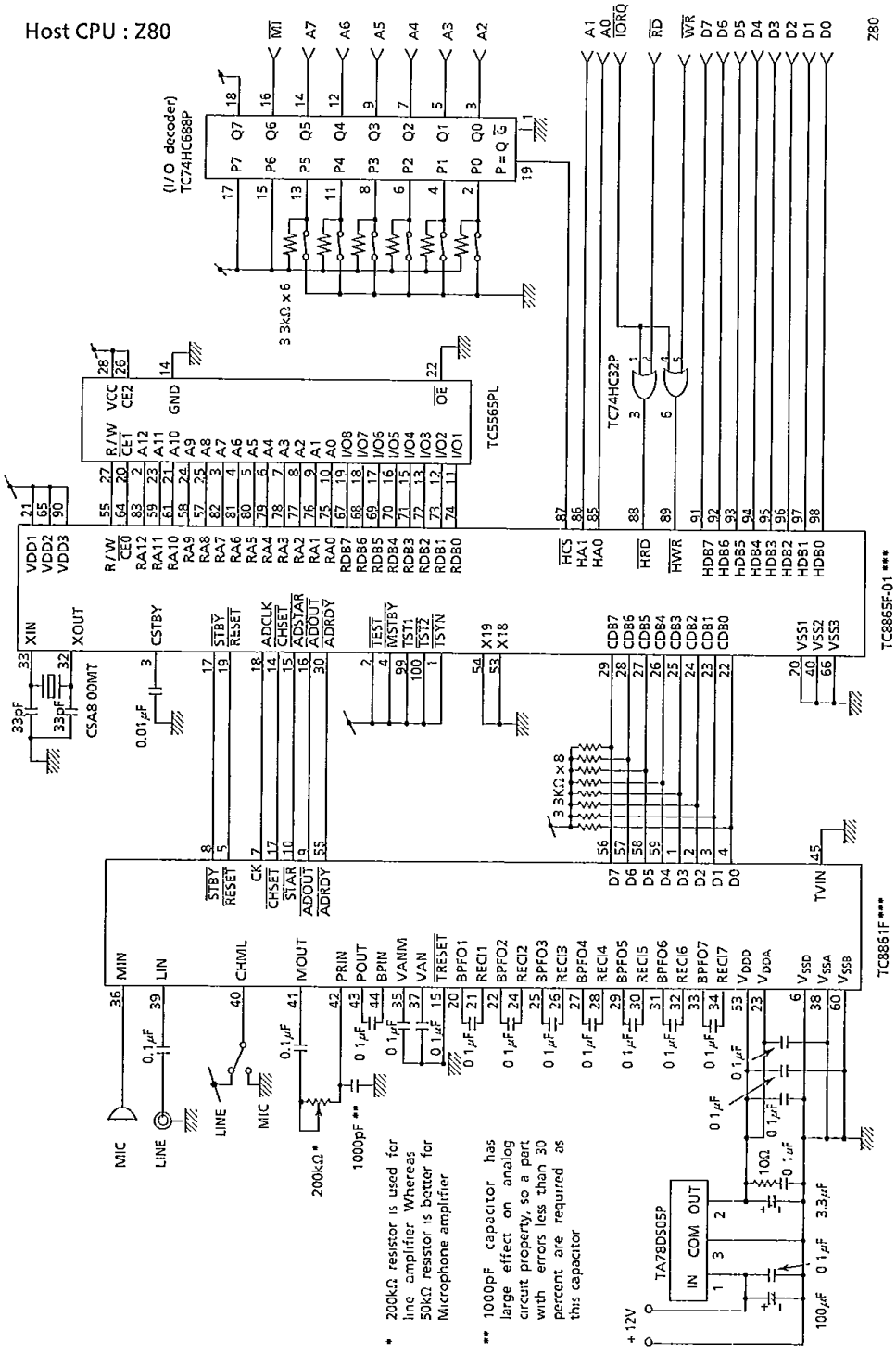


Fig. 8.1 Application Circuitry Example

467-A