1. Introduction

The speaker dependent isolated word recognition device set consists of TC8861F, TC8864F-00 and 64kbit static RAM. The device set contains the whole circuits and functions necessary to recognize voices, so it is easily employed in a wide range of applications. The device set operates with commands given by a host computer.

1.1 Features of Recognition Device Set

(1) Reference pattern generation* with Differential Filter Method**. Three utterances per word required.

(2) Pattern matching with Multiple Similarity Method***.

(3) Configuration: TC8861F, TC8864F-00 and 64kbit static RAM.

(4) Recognition rate: 95%
(Vocabulary: 50 most frequent Japanese sir names
Test Speakers: 8 Japanese (males, females))

(5) Vocabulary numbers: Maximum 50.

(6) Response time: 0.3~0.5 seconds.
(Defined as the time length from the utterance end point to the time point of result return to the host computer.)

(7) Input voice time length allowed: 0.12~1.6 seconds.

(8) Reference pattern bank setting: Every reference pattern can be, if necessary, allocated to one of 8 banks so that the device set executes pattern matching with vocabularies in the designated bank.

(9) Rejection:
On registration: If three utterances for a word shows characteristic differences among them, the device set rejects these three utterances and then requires another three for the same word again.
On recognition: If a voice to be recognized presents low similarity to all the vocabularies registered, the device set rejects input voice and requests another input voice.

(10) Directly connectable to a voice input microphone.

(11) Power saving mode available.

(12) +5 single power supply: (Caution: The separate second power suppy is recommended to be employed to TC8861F in order to improve the recognition rate.)

* Reference patterns must be readily generated on 64k bit static RAM through registration process requiring users to store vocabularies by their own voices. These patterns are examined to choose the most possible vocabulary candidate when voice to be recognized enters the device set.

** The method uniquely developed by Toshiba.

*** The method jointly developed by the Agency of Industrial Science & Technology of MITI in Japanese Government, and Toshiba. The device set adopts the Patent "Multiple Similarity Method" (Japanese Patent No.739890) under license of the Japanese Industrial Technology Association. Details are to be referred to references (1), (2).

References

(1) Y.Takebayashi, et al., "Telephone Speech Recognition Using a Hybrid Method", IEEE 7th International Conference on Pattern Recognition Proc., pp.1232-1235, 1984.

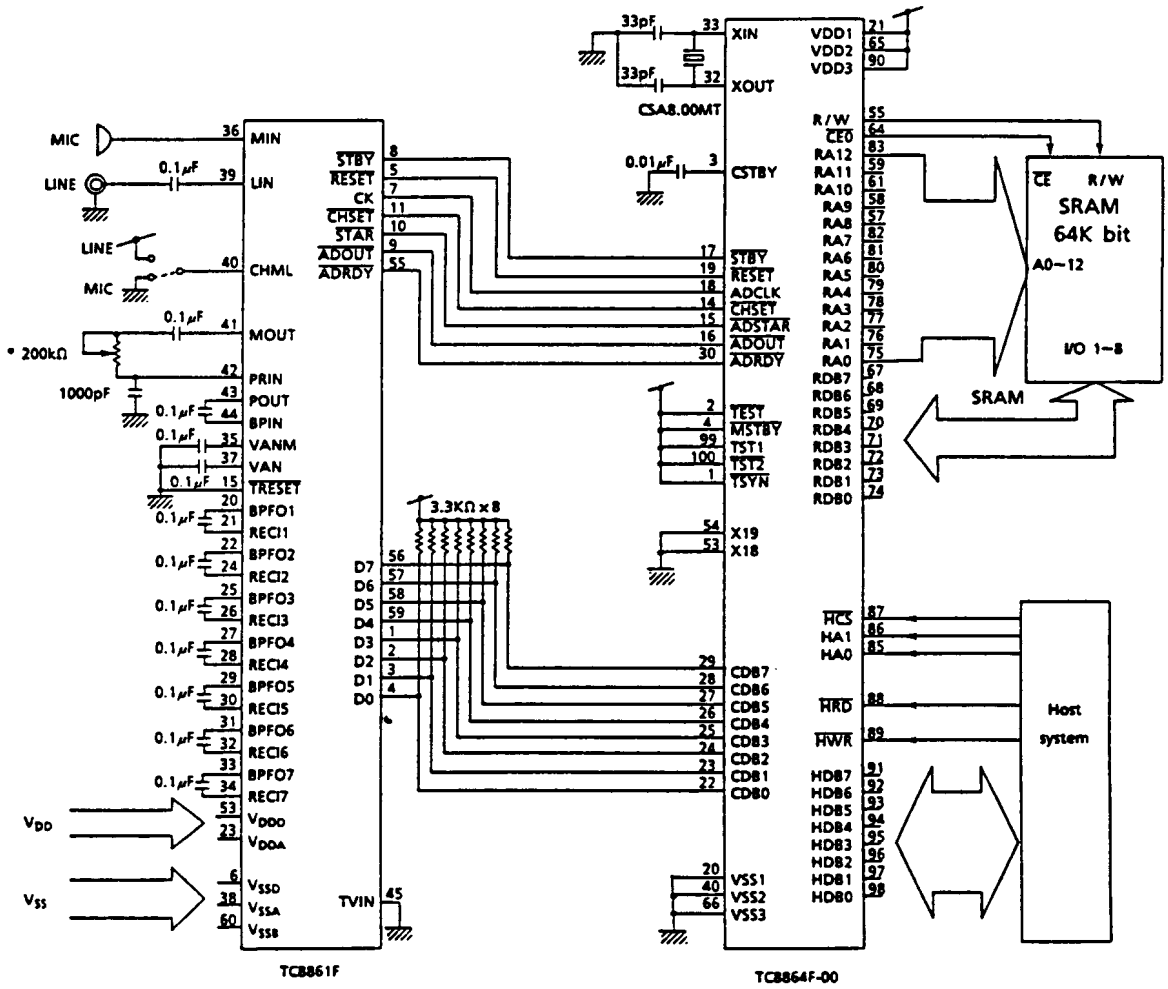
(2) H.Sekiguchi, et al., "A Three-Chip LSI System for Speaker Independent Isolated Word Recognition by Multiple Similarity Method", IEEE ICCE Dig. of Tech. Papers pp.240-241, 1987.

2. Hardware on Device Set

The purpose of this chapter is to outline the device set hardware. The device set configuration is mentioned in 2.1 and also block diagrams are shown in 2.2. Each dvice on the set is briefly described in 2.3 from the functional viewpoint.

2.1 Device Set Configuration

The recognition device set is comprised of 3 chips. They are TC8861F analog processor, TC8864F-00 digital processor and 64kbit CMOS static RAM.



* A 50kΩ or 200kΩ resister is recommended for microphone amplifier or Line amplifier respectively.

Fig. 2.1 Device Set Configuration

2.2 Device Set Block Diagram

Fig. 2.2 shows the device set block diagram.

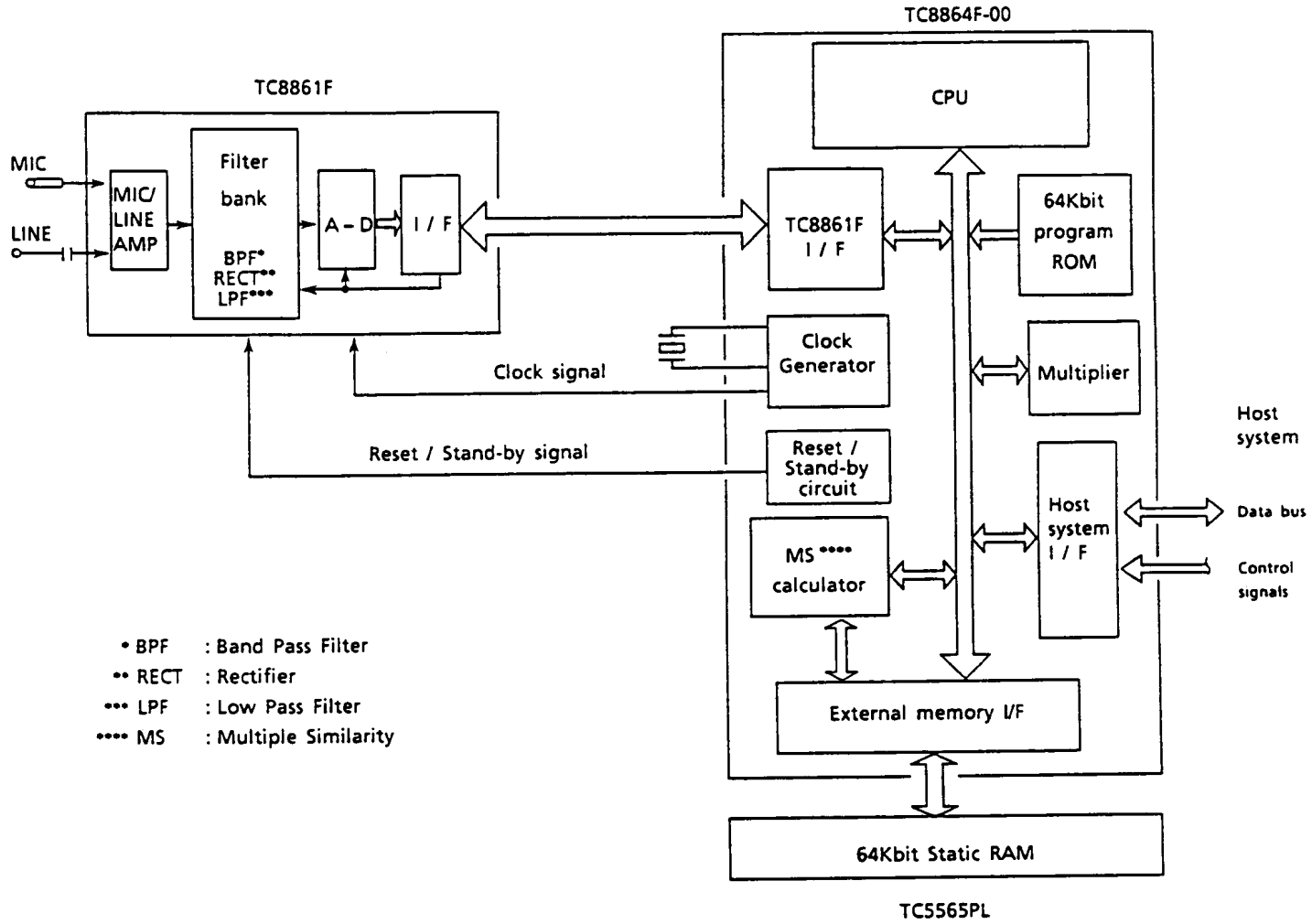


Fig. 2.2 Device Set Block Diagram

2.3 Explanation of Block Diagram

Features on each device are roughly described here. More details for each device are mentioned in Chapter 6.

2.3.1 TC8861F Analog Processor

(1) MIC/LINE AMP
Two types of amplifiers respectively for a microphone input or for an audio line input. A microphone can connect with MIC AMP directly.

(2) Filter bank
Built-in 7 channel band-pass filters.

(3) A - D
Built-in analog-to-digital (A to D) converter with 10bit resolution for acoustic analysis of voice signals.

(4) I/F
Interface with TC8864F-00.

2.3.2 TC8864F-00 Digital Processor

(1) CPU
Built-in central processing unit (CPU) with system architecture compatible with TMPZ84C00A.

(2) TC8861F I/F
Interface with TC8861F.

(3) 64K bit program ROM
This ROM contains the speaker dependent word recognition program codes.

(4) Multiplier
Multiplier speeds up registration process, used by CPU.

(5) MS calculator
This block calculates the similarity between the input voice data and reference patterns for each words.

(6) External memory I/F
Interface for a external RAM.

(7) Host system I/F
Interface for a host system.

(8) Reset/Stand-by circuit
This block makes system reset and stand-by signal.

(9) Clock Generator
Built-in oscillation circuit for ceramic resonator. This block makes 8MHz system clock.

2.3.3 64Kbit Static RAM

This memory stores scratch-pad data and reference patterns.

3. Device Set Functional Organization

The device set provides 12 functions as described in Fig. 3.1. These functions are embedded in 3 LSI hardware and software program on the TC8864F-00 on-chip Mask ROM *.

All the functions are executed by commands given by a host computer. Therefore the device set always needs a host computer. Practical description about command operations are given in Chapter 4 and Chapter 5 in terms of both hardware aspects and software aspects, respectively.

The two most important functions among twelve are reference pattern registration and recognition. 3.1 and 3.2 describe these two functions. 3.3 shows the system inner state transfer chart to overview the device set functional organization.

* Toshiba holds the copy right for the programs embedded in the Mask ROM.

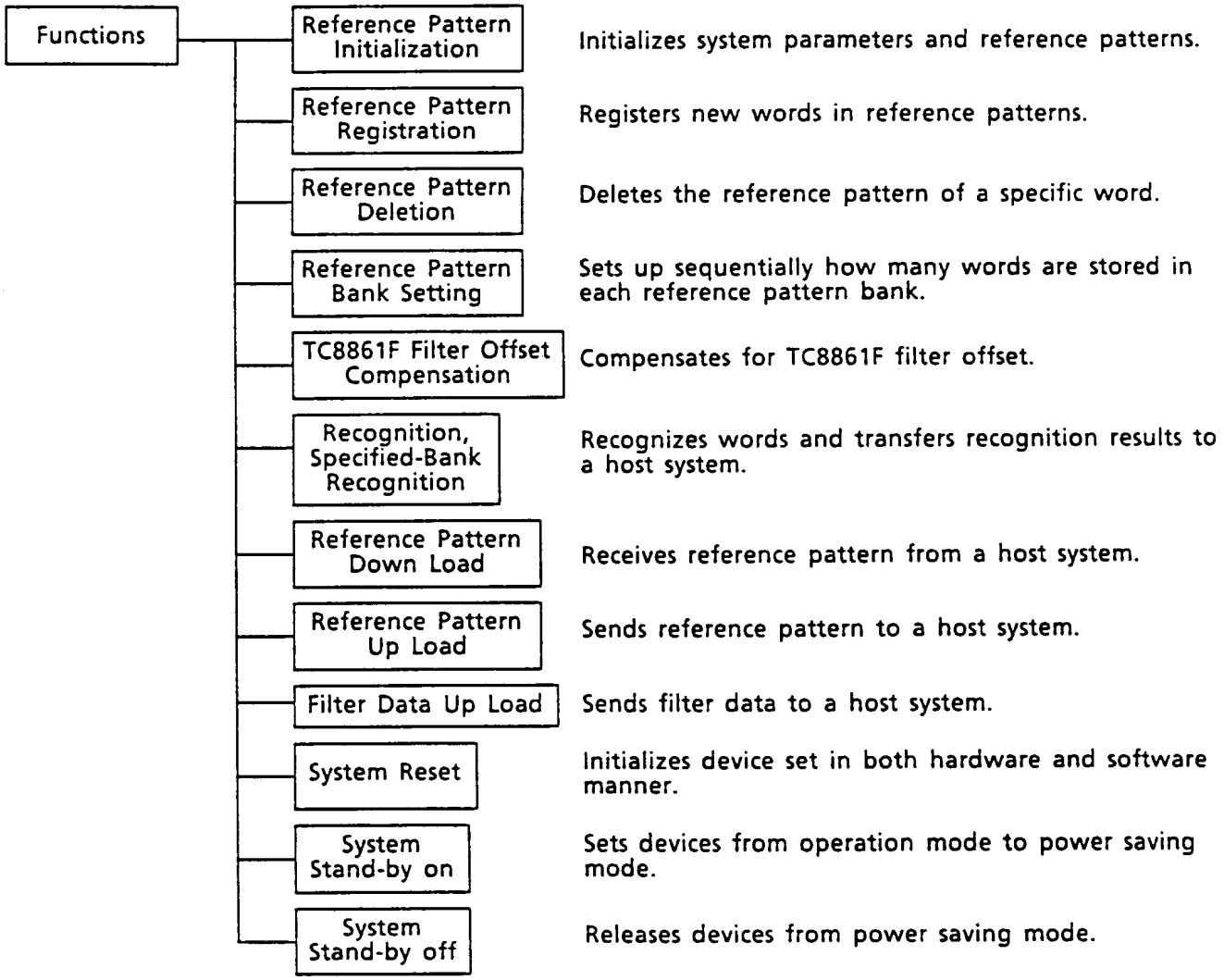


Fig. 3.1 Functional Organization of Device Set

3.1 Reference Pattern Registration

Reference patterns for vocabularies to be recognized must be stored in external static RAM before recognition. To store reference patterns is called registration. A reference pattern for a word is made by analyzing three utterances. The sequence of reference pattern production is itemized below and is illustrated in Fig. 3.2.

(1) TC8861F receives three utterances per word to analyze them and to digitize the analyzed analog signals with A to D.

(2) CPU detects word boundaries with A to D output signals. Then it prepares a reference pattern.

(3) The prepared reference pattern is, through external memory I/F, transferred to and is stored in external static RAM.

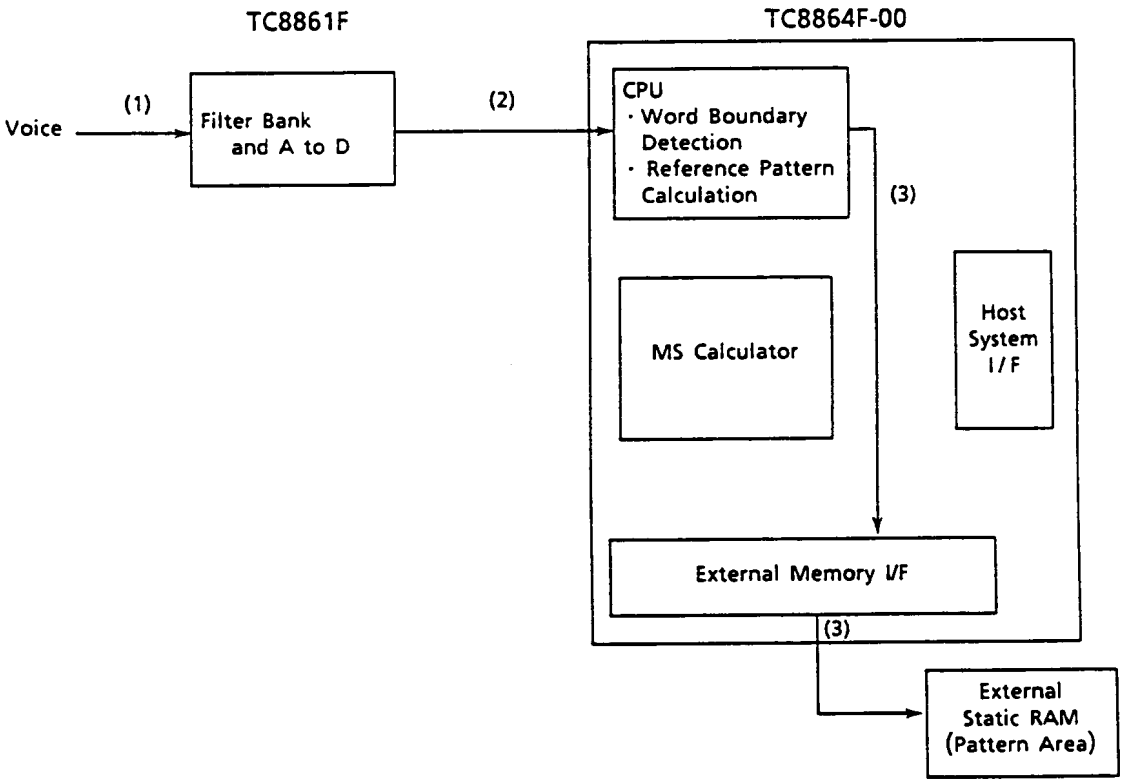


Fig. 3.2 Data Flow in Reference Pattern Registration

3.2 Recognition

The device set recognizes voices in a way that it compares input voice features with vocabulary reference patterns beforehand stored in an external static RAM. The recognition results indicating most possible word candidates for input words are transferred to a host computer. The functional process is itemized below and is charted in Fig. 3.3.

(1) TC8861F receives a voice to be recognized, analyzes acoustically, and digitizes the analyzed analog signals with A to D.

(2) CPU detects word boundary of A to D output signals.
Then the detected signals are transmitted to a data RAM in the MS calculator.

(3) The similarity of the detected signals to all reference patterns stored in external static RAM is examined.

(4) All similarity scores with the whole vocabularies are transferred to CPU.

(5) CPU arranges the scores in reverse-numerical order. And the top three scores and their word numbers are sent to the host system I/F on TC8864F-00.

(6) The top three scores and their word numbers are transferred to a host system.

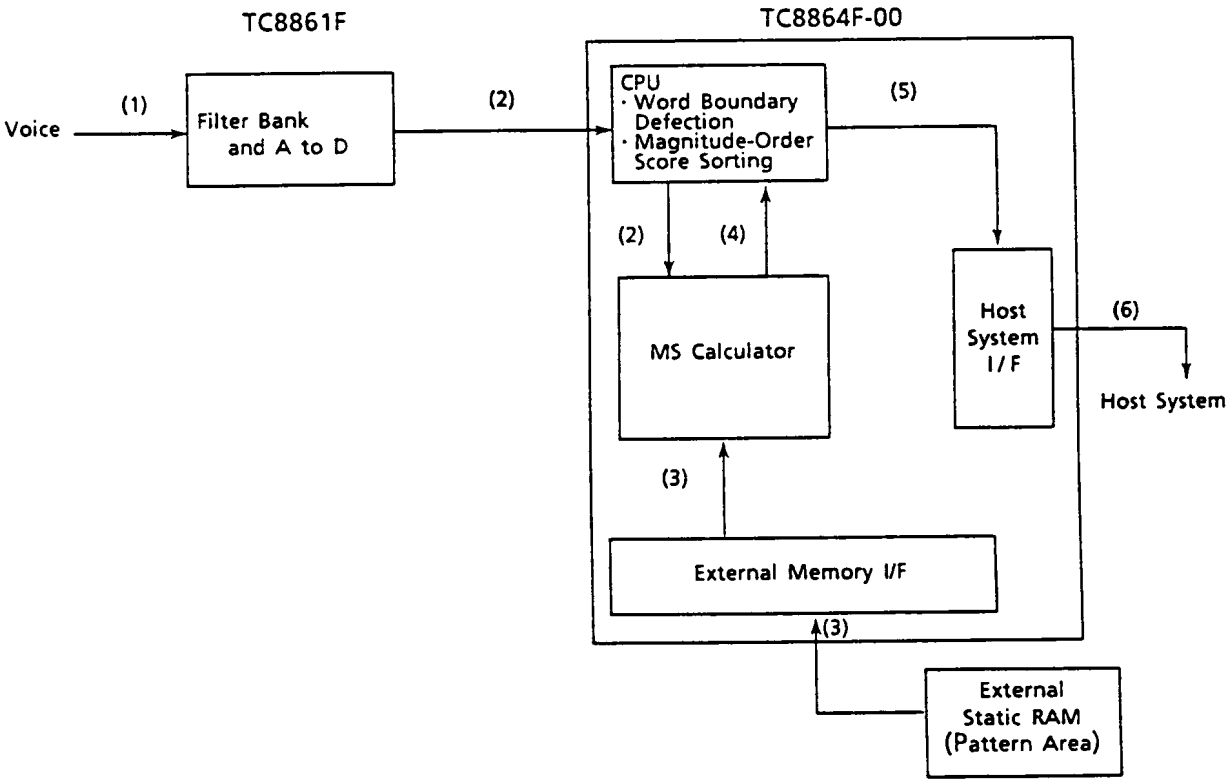
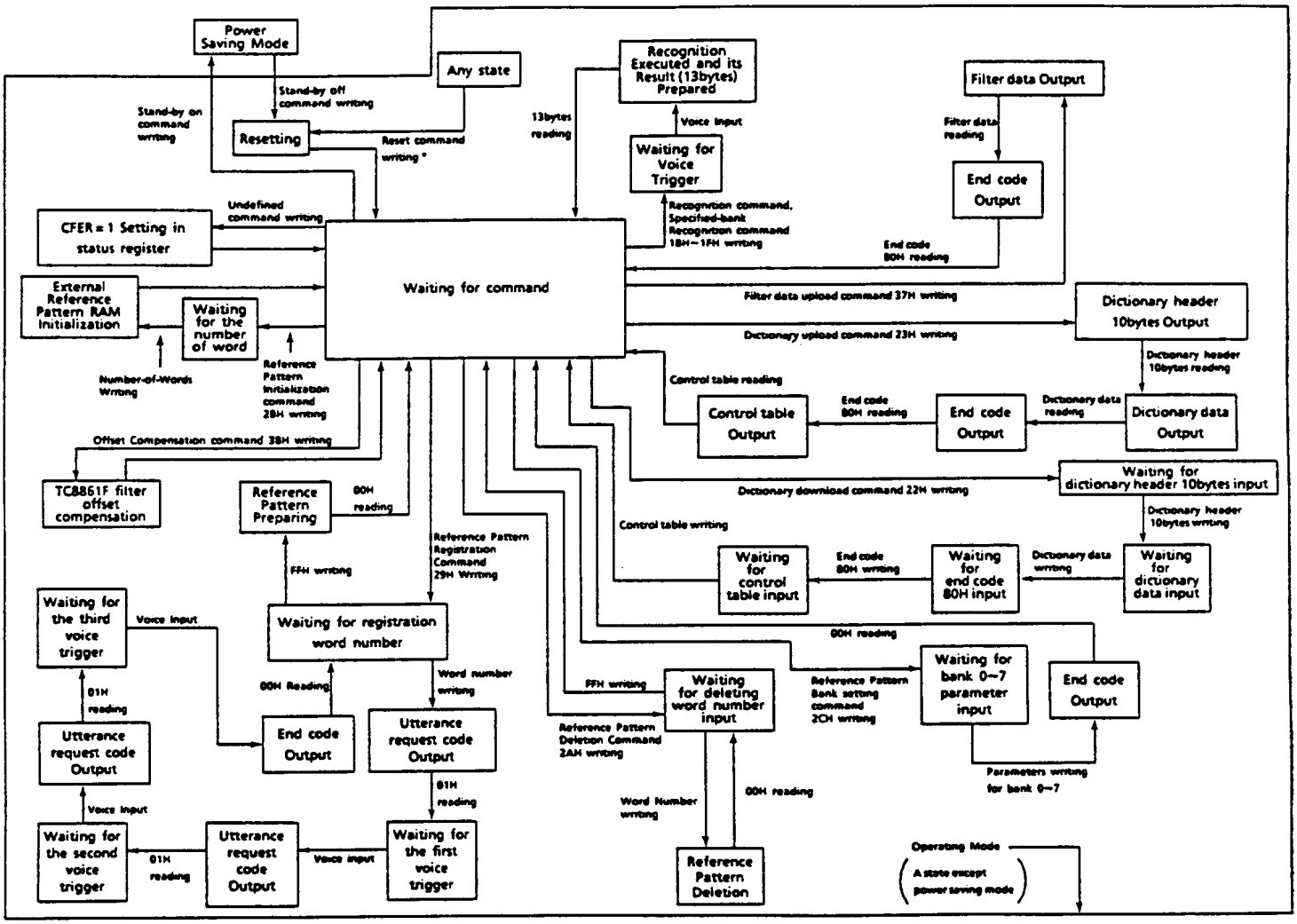


Fig. 3.3 Data Flow in Recognition

3.3 System Inner State Transfer Chart

The device set changes its inner state by host system command/data writing, host system data reading and voice input through MIN/LIN terminals on TC8861F. The inner state transfer chart is depicted in Fig. 3.4. Here "writing" means command/data transfer from a host system to the device set and "reading" indicates data transfer from the device set to a host system.



* Writing the reset command is allowed any time except when reference patterns are being generated. More detail information about the reset command is mentioned at 5.3.16.

Fig. 3.4 System Inner State Transfer Chart

3.4 Recognition Rate

3.4.1 Definition of Recognition Rate

Recognition rate varies with a vocabulary, a voice quality and a recognition rate calculation method. Though many calculation method for unbiased recognition rate have been proposed, there is no standard formula for recognition rate. In this manual, recognition rate is calculated by following definition.

Expression:

$$\text{Recognition rate} = \frac{N - E}{N}$$

Where: N means all test voice count. N = 2 (times per words) × m (words).

E means incorrect result count.

Evaluation method:

(1) The voice is recorded to an audio tape 5 times for each word.

(2) The tape is played back, and 3 utterances of each word are sent to the device set and are analyzed for the reference pattern. Here the audio signal line is fed into LIN terminal of TC8861F.

(3) Remaining 2 utterances per word in the audio tape are used for the test data to calculate recognition rate.

Condition:

Reject flag, Too long flag and Too low flag are ignored, and recognition rate is calculated by the correct/incorrect answer counts.

3.4.2 To Get Optimal Performance

To achieve optimal performance of the device set, it is recommended to follow several notes and advices mentioned below.

Notes about a vocabulary:

(1) This system can deal with an isolated word recognition, but it can hardly recognize connected words and sentences which are spoken continuously.

(2) A vocabulary must be made of 2 through 5 syllabled words. A word with one syllable or over six syllables decreases system performance. Especially the alphabet is similar to each other, leading to low performance.

Notes about an utterance:

(1) On registration, at least three utterances are needed and each utterance must be same as much as possible. Different utterances will be rejected.

(2) On recognition, an utterance should be same as registered voice as possible.

(3) The dynamic range of input voice signal is 10 through 15 dB for maintaining high performance.

(4) Two factors to decide the level of input voice signal exist, one is the speaker's voice volume and the other is the distance from the speaker's mouth to a microphone. The recommended distance between the mouth and the microphone is roughly 5 through 15 cm according to voice level.

(5) A microphone must observe following conditions:

Frequency characteristics:	Flat gain from 200Hz to 7KHz. Gain deviation is within ±2.5dB.
Directivity:	single directional.

Limitations about an environment noise:

The recognition system can be used in the office environment (noise level with at most 50dBA). Performance in more noisy environment degrades.

Limitation of candidates:

In the case that only a part of the words in reference patterns are previously known as targets, reference pattern bank setting command and specified-bank recognition command are recommended. The unnecessary words for recognition are removed and better performance is achieved.

Removing offset by TC8861F filter offset compensation command:

Each TC8861F has a different offset. Moreover, the offset relates to supply voltage and temperature of atmosphere. The offset causes wrong recognition result because the offset disturbs correct frequency analysis. TC8861F offset compensation circuit can remove the offset by TC8861F offset compensation command. Offset compensation is automatically executed by system reset command, system stand-by off command, and power on.

4. Host System Interface

4.1 Introduction to Interface Hardware

A host system operates the recognition device set with both commands and data transferred through the host system interface circuit on TC8864F-00. The circuit reads or writes 8-bit parallel data bus like a general purpose 8bit parallel interface TMP82C55AP-5. TC8864F-00 terminals for the operations are HDB0~7, $\overline{HCS}$, $\overline{HRD}$, $\overline{HWR}$, HA0~1. Functional description for the terminals are given in Table 4.1.

Table 4.1 Host Interface Terminals and their Functions

Terminal Names	Number of Terminals	Input/ Output	Description
HDB0~7	8	3 state Input/ Output	8 bit 3-state bidirectional data bus. Used for transferring commands, data and status between host system and device set.
$\overline{HCS}$	1	Input	Chip select input. At "L" level, data transfer with host system is enabled. At "H" level, all signals given by host system are ignored.
$\overline{HRD}$	1	Input	Read strobe signal. At "L" level, HDB0~7 is put in the output mode so that host system may read data on HDB0~7. (at $\overline{HCS}$ = HA1 = "L")
$\overline{HWR}$	1	Input	Write strobe signal. At rising edge, command or data are written from HDB0~7 into a specific register. (at $\overline{HCS}$ = HA0 = "L")
HA1, HA0	2	Input	Addresses selecting command/data register, status register or reset/stand-by register. Generally connect to lower 2bits of address bus of host system.

4.2 Interface Hardware Configuration and its Timing

TC8864F-00 host interface circuit hardware block diagram is illustrated in Fig. 4.1. The circuit contains three registers, command/data register (8bit), status register (8bit) and reset/stand-by register (1bit). Host system's reading/writing operations with these registers run the device set. The registers are distinguished among themselves by two address terminals (HA0, HA1). The command/data register can be read/written and the status register is dedicated to reading only. The reset/stand-by register is dedicated to writing only.

Table 4.2 shows the terminal setting to realize the above-mentioned functions. Switching timings in reading or writing operations are illustrated in Fig. 4.2 and Fig. 4.3.

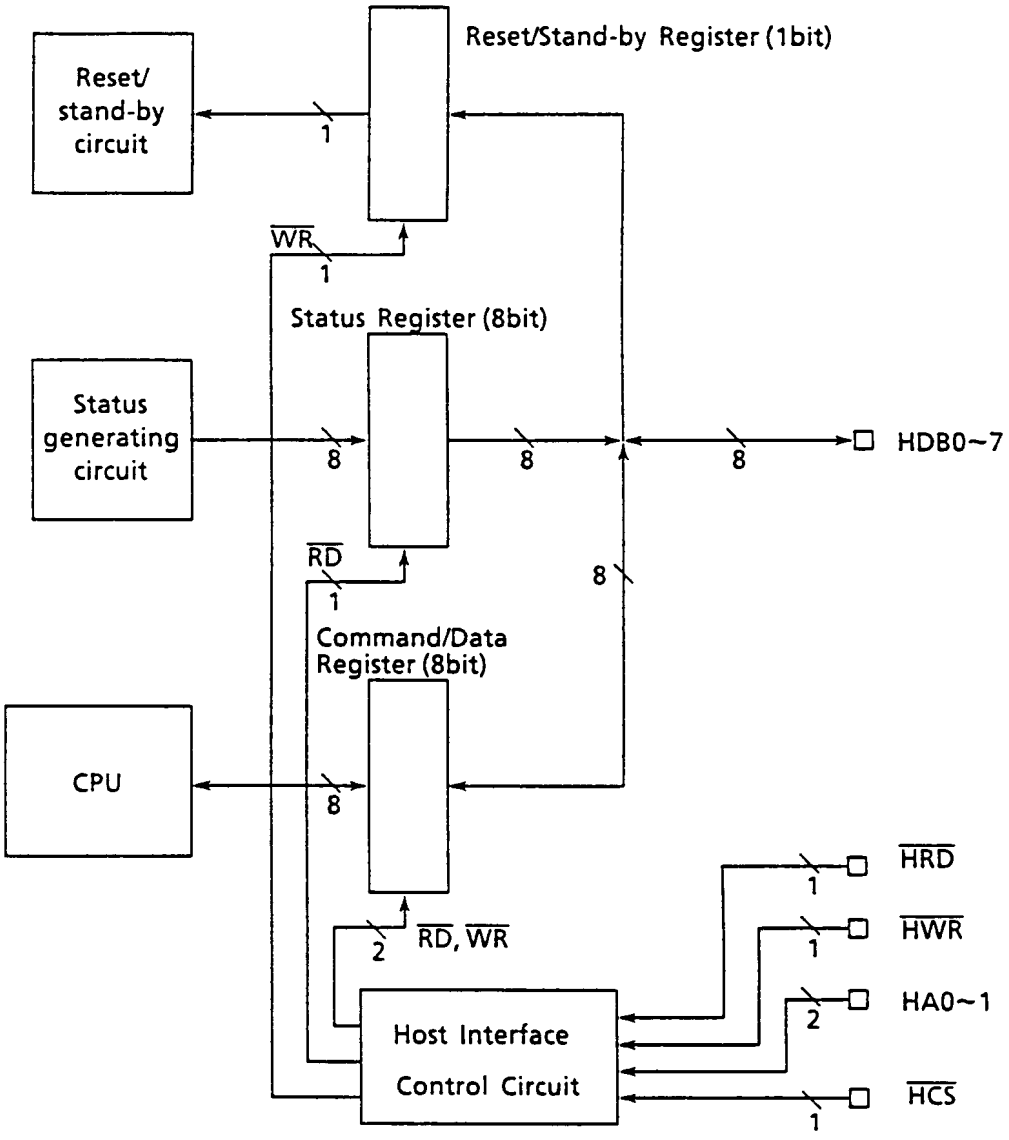


Fig. 4.1 Host Interface Circuit Block Diagram

Table 4.2 Terminal Setting for Functions

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Functions
0	0	0	0	1	Data Reading.
0	0	0	1	0	Command/Data Writing.
0	1	0	0	1	Status Reading.
1	0	0	1	0	Reset/Stand-by Command Writing.
×	×	0	1	1	Device Set remains unchanged.
×	×	1	×	×	Device Set remains unchanged.
0	1	0	1	0	Device Set remains unchanged.
1	0	0	0	1	Device Set remains unchanged.
1	1	0	0	1	Device Set remains unchanged.
1	1	0	1	0	Device Set remains unchanged.
×	×	0	0	0	Not Allowed.

0 : "L" level, 1 : "H" level, × : Don't care

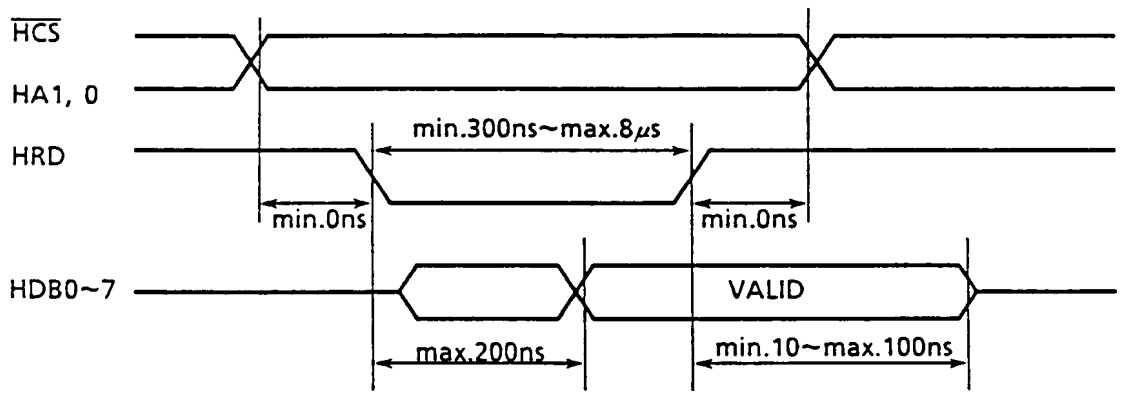


Fig. 4.2 Host Interface Reading Cycle Timing

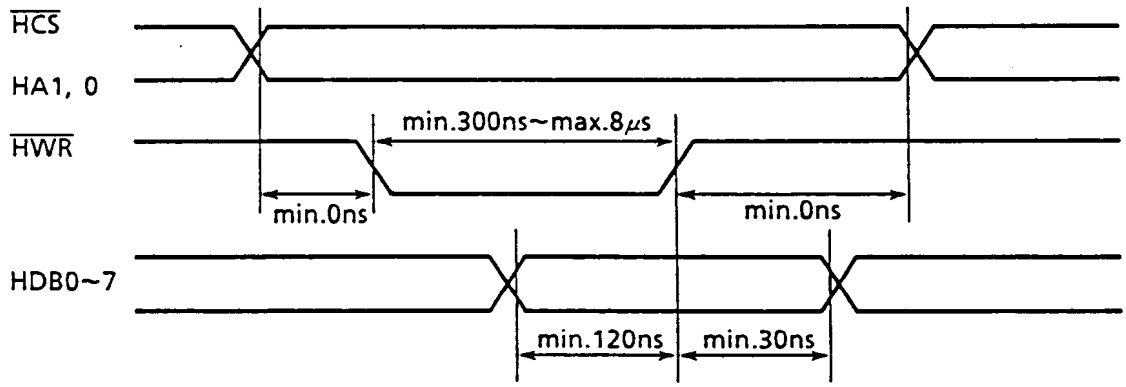


Fig. 4.3 Host Interface Writing Cycle Timing

4.3 How to Use Command/Data Register

Command/data register with 8bit data is used for "command"/"data" writing operation and data reading operation. Here "command code" is defined as 8bit code given into this register by a host computer on waiting state for the next command. On the other hand, "data" are defined as 8bit data transferred through the register while the device set is executing commands. Examples of "data" are "word number" given by a host system and "control code" output to a host system in registration command execution.

Table 4.3 shows a command list to with the command/data register. Operating details and their usages are referred to 5.3 Command Description.

Table 4.3 Commands with Command/Data Register

Command	HDB0~7	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$
Reference Pattern Initialization	28H	0	0	0	1	0
Reference Pattern Registration	29H					
Reference Pattern Deletion	2AH					
Reference Pattern Bank Setting	2CH					
TC8861F Filter Offset Compensation	38H					
Recognition	18H*					
Reference Pattern Down Load	22H					
Reference Pattern Up Load	23H					
Filter Data Up Load	37H					

* 18H is a bank 0 recognition command. 19H is for bank 1. The same way holds for other banks. Namely 1AH is for bank 2 and 1FH is for bank 7. In case bank setting is not preset beforehand, only 18H executes recognition operation.

4.4 Hand Shake with Command/Data Register

Communication between the host system and the device set with the command/data register employs "hand shake" protocol. This protocol uses two status signals HRRDY (Host Read ReaDY) and HWRDY (Host Write ReaDY), offered as flag bits on the status register.

HRRDY = "1" indicates that the device set is ready to send some data to the host system. HWRDY = "1" means that the device set is waiting for command code and data to come from the host system. Note that the two status signals will not be "1" simultaneously.

Host system operational sequence is as follows:

(1) When commands/data are written into the device set,
   ① Check whether HWRDY "1".
   ② Go to ① when HWRDY is "0" (when the device set is not ready to receive command/data from the host system).
   ③ Write command code or data into the device set when HWRDY is "1" (when the device set is waiting for command code or data). The finish of writing operation automatically leads to HWRDY = "0". (The device set is released from the command/data waiting state.) Exit.

(2) When data are read out from the device set,
   ① Check whether HRRDY = "1".
   ② Return to ① when HRRDY is "0".
   ③ Read data from the device set when HRRDY is "1" (when the device set is ready to output date to the host system). Reading operation automatically leads to HRRDY = "0". (The device set is released from the sending-data ready state.) Exit.

Fig. 4.4 illustrates the "hand shake" protocol timing chart.

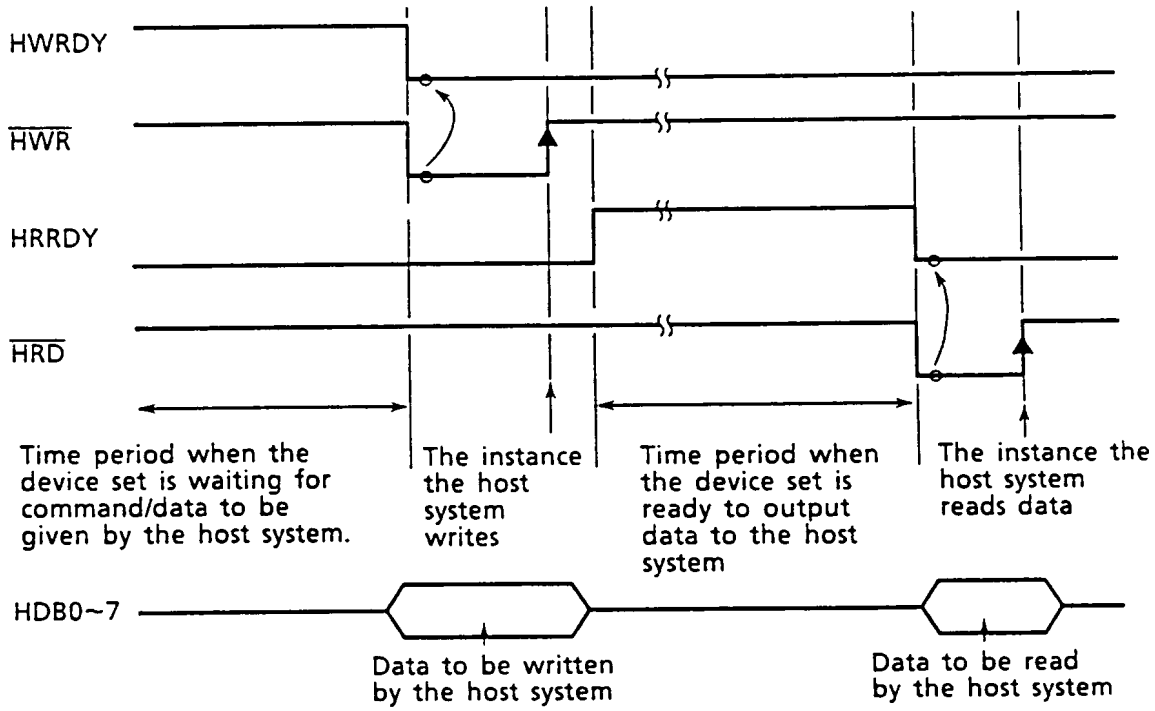
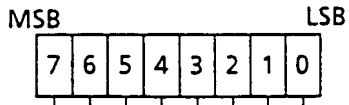


Fig. 4.4 "Hand Shake" Timing Chart

4.5 How to Use Status Register

Status register with 8bit flags indicating the device set state is allowed only to be read. Reading operation doesn't require the "hand shake" protocol described in 4.4. Instead reading is permitted in any instance. Each bit flag meaning is explained in the following figure.



HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$
0	1	0	0	1

1 = H Level, 0 = L Level

- HWRDY — HWRDY "1" indicates that command/data register is ready to receive data given by a host system.
- HRRDY — HRRDY "1" indicates that command/data register contains data to be read by a host system.
- STBY — STBY "1" means the device set is in power saving mode.
- RESET — RESET "1" means the device set in reset period with no data transfer allowed.
- TMGER — TMGER becomes "1" when writing operation to command/data register is executed during reset period. Note that the writing operation is dealt invalid. The consecutive writing operation to command/data register releases TMGER from "1" with its original function executed.
- CFER — CFER becomes "1" within 300μs when undefined command or recognition command with no reference pattern registered is executed.
- TRANS — TRANS is "1" while reference pattern up load, reference pattern down load or filter data up load command is being executed.
- RECOG — RECOG is "1" while registration or recognition command is being executed.

Fig. 4.5 Flag Meanings of Status Register

4.6 How to Use Reset/Stand-by Register

Reset/stand-by register with a 1bit writing-only flip-flop offers three kinds of functions determined by combination of the current device set state (power saving mode or operating mode) and 1bit datum, 0 or 1, to be written.

Writing with the least significant bit (LSB) of "0" (ex. 00H) to the reset/stand-by register in the operating mode results in reset command execution, which initializes the device set in hardware way and then returns it back to a waiting state for host system commands. Also writing with LSB of "1" (ex. 01H, FFH) in the operating mode leads to the power saving mode in the device set; which ceases all operations. Writing with LSB of "0" in the power saving mode releases the device set from the power saving mode to the operating mode.

Table 4.4 describes terminal settings and functions. Note that writing to the reset/stand-by register do not require the "hand shake" protocol described in 4.4, and is allowed to be executed any time.

Table 4.4 Reset/stand-by Register Function

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	HDB0 (LSB)	Description	The Device Set State on Writing
1	0	0	1	0	0	Reset the device set	Operating Mode
1	0	0	1	0	1	Place the device set in power saving mode	Operating Mode
1	0	0	1	0	0	Release the device set from power saving mode	Power Saving Mode

1 = H Level, 0 = L Level

5. Host System Command

The device set always operates with commands given by a host system. This chapter overviews how to write programs on a host system for the device set management. 5.1 describes commands acceptable to the device set and how the device executes these commands. 5.2 shows an example of host system operation as an introduction. 5.3 handles detail explanations to use commands. 5.4 depicts all data formats employed in the device set.

5.1 Command Process in Device Set

5.1.1 Command List

All commands available are listed in Table 5.1. These commands are 8bit data written into the device set by a host system. The commands are divided into two categories, one employing command/data register and the other using reset/stand-by register.

Table 5.1 Command List (1 = "H"level, 0 = "L"level)

Command Name	Command Code (HDB0~7)	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Notes
Reference Pattern Initialization	28H	0	0	0	1	0	Command/data Register used
Reference Pattern Registration	29H	0	0	0	1	0	
Reference Pattern Deletion	2AH	0	0	0	1	0	
Reference Pattern Bank Setting	2CH	0	0	0	1	0	
TC8861F Filter Offset Compensation	38H	0	0	0	1	0	
Recognition	18H*	0	0	0	1	0	
Reference Pattern Down load	22H	0	0	0	1	0	
Reference Pattern Up load	23H	0	0	0	1	0	
Filter data Up load	37H	0	0	0	1	0	
Reset	HDB0 = 0	1	0	0	1	0	Reset/stand-by Register used
Stand-by On	HDB0 = 1	1	0	0	1	0	
Stand-by Off	HDB0 = 0	1	0	0	1	0	

* Recognition commands other than 18H are valid as described in the following table in case reference pattern bank is created beforehand.

Bank 0 Recognition	18H	HA1 = HA0 = $\overline{HCS}$ = $\overline{HWR}$ = 0 $\overline{HRD}$ = 1
Bank 1 Recognition	19H	
Bank 2 Recognition	1AH	
Bank 3 Recognition	1BH	
Bank 4 Recognition	1CH	
Bank 5 Recognition	1DH	
Bank 6 Recognition	1EH	
Bank 7 Recognition	1FH	

5.1.2 Reference Pattern Initialization Command (28H)

Reference pattern initialization command initializes reference patterns and CPU scratch-pad memory so that it may enable the device set to be ready for initial registration. The reference pattern memory contents of the word number 1 through the designated word number are cleared to zero. This command should be executed at least once after power supply to the device set is turned on.

Process in the device set:

Start.
↓
CPU scratch-pad area in the external static RAM is initialized.
↓
Reference pattern area for the designated words is cleared to zero.
↓
command waiting.

5.1.3 Reference Pattern Registration Command (29H)

This command registers voice features on reference pattern RAM segments designated by word numbers. Usually three utterances per word are required to be input through analog input terminal on TC8861F. Reference pattern is generated by calculating these three utterances. In the case similarity among the spoken three is low, another three utterances for the word are required.

Process in the device set:

Start.
↓
Voice through analog input terminal on TC8861F is input.
Three utterances per word.
↓
Word boundary is detected.
↓
Validity of the input voice is checked.
↓
Reference pattern is prepared.
↓
Reference pattern is registered to external static RAM.
↓
command waiting.

5.1.4 Reference Pattern Deletion Command (2AH)

Reference pattern deletion command clears into zero reference pattern data of a specified word.

Process in the device set:

Start.
↓
Reference pattern data for the designated word is cleared to zero.
↓
command waiting.

5.1.5 Reference Pattern Bank Setting Command (2CH)

This command divides reference pattern RAMs into maximum 8 blocks, so called banks. Each bank contains any consecutive words in the memory space. This command is a complimentary function to the specified-bank recognition command, which recognizes input voice as one of words in a designated bank, when input voice is previously known as one of them.

Process in the device set:

Start.
↓
Validity of written bank setting parameters for each bank is examined.
↓
Bank setting parameters are registered to the specified area in scratch-pad area.
↓
command waiting.

5.1.6 TC8861F Filter Offset Compensation Command (38H)

This command compensates for TC8861F filter offset. Offset values vary by individual TC8861F or its assembly condition. Offset degrades frequency analysis accuracy on TC8861F and reduces recognition performance. To eliminate this harmful influence, TC8861F is equipped with offset compensation function.

Process in the device set:

Start
↓
Compensation for TC8861F filter offset is conducted.
↓
command waiting.

5.1.7 Recognition Command (18H), Specified-Bank Recognition Command (18H~1FH)

These commands perform recognition of input voice. When reference pattern banks are previously not set, only recognition command (18H) is effective. When they are set, specified-bank recognition command (18H~1FH) are valid. Specified-bank recognition is powerful to improve recognition performance by limiting the number of vocabulary referred to in pattern matching.

Process in the device set:

Start.
↓
Voice through analog input terminal on TC8861F is input.
↓
Word boundary is detected.
↓
Similarity scores between input voice and reference patterns are calculated.
↓
Similarity scores are arranged in reverse numerical order.
↓
Final recognition result is decided according to above similarity score order.
↓
Recognition result is transferred to host system.
↓
command waiting.

5.1.8 Reference Pattern Down Load Command (22H)

Reference pattern down load command receives the reference patterns from a host system and then stores them to the external static RAM. When reference patterns already exist in the external static RAM, contents of reference pattern are replaced with the new data from the host system. Reference pattern is transferred with the format explained in 5.4.4.

Process in the device set:

Start.
↓
Number of words is received by device set (1 byte) and stored to the reference pattern area.
↓
Header data (9 bytes) are received and stored to the scratch-pad area.
↓
Reference pattern data are transferred to device set until end of data code (80H) is met. They are all stored to the reference pattern area.
↓
Control table data (1 byte per word) are transferred and stored to the work area.
↓
command waiting.

5.1.9 Reference Pattern Up Load Command (23H)

Reference pattern up load command sends the reference patterns to a host system. Reference patterns are transferred with the format explained in 5.4.4.

Process in the device set:

Start.
↓
Number of words (1 byte) is sent to host system.
↓
Header data (9 bytes) are sent to host system.
↓
Reference pattern data and end of data code (80H) are sent.
↓
Control table data (1 byte per word) are sent.
↓
command waiting.

5.1.10 Filter data Up Load Command (37H)

This command sends the filter data to a host system. Because the filter data has variable length, the end of data (FFH) is always added as the last data. More detail information about filter data is illustrated in 5.4.5.

Process in the device set:

Start
↓
Filter data are sent.
↓
End of data code (FFH) is sent
↓
command waiting.

5.1.11 System Reset Command (Reset / Stand-by Register)

This command initializes the device set in hardware manner. The data in the external static RAM keeps its contents after this command. But in some cases, the device can't keep the contents of the external static RAM. Refer to 5.3.16 Notes on system Reset Command Usage for more details.

Process in the device set:

Start.
↓
CPU starts from address zero in the program memory.
↓
Filter offset in TC8861F is compensated for.
↓
Command waiting.

5.1.12 System Stand-by On Command (Reset / Stand-by Register)

The device set has the power saving function. In the power saving mode, internal system clock is stopped and system power consumption becomes less than 10μA. This state is called stand-by mode. The data in the scratch-pad area and reference patterns keep their contents even in the stand-by mode. To release from stand-by mode, system stand-by off command should be executed.

Process in the device set:

Start.
↓
To stand-by mode (system clock is stopped).

5.1.13 System Stand-by Off Command (Reset / Stand-by Register)

This command releases the device set from stand-by mode to normal mode. In normal mode internal system clock operates normally.

Process in the device set:

Start.
↓
System clock starts.
↓
CPU starts from address zero in the program memory.
↓
Filter offset in TC8861F is Compensated for.
↓
Command waiting.

5.2 Host System Operation Flow Chart Example

Here described is a flow chart example to operate the device set in the following sequence:

(1) Reference pattern initial registration.

(2) Recognition.

(3) Reference pattern deletion.

These three activities are essential to any recognition device. Fig. 5.1 illustrates the flow chart. More details in each operation in Fig. 5.1 are referred to 5.3.

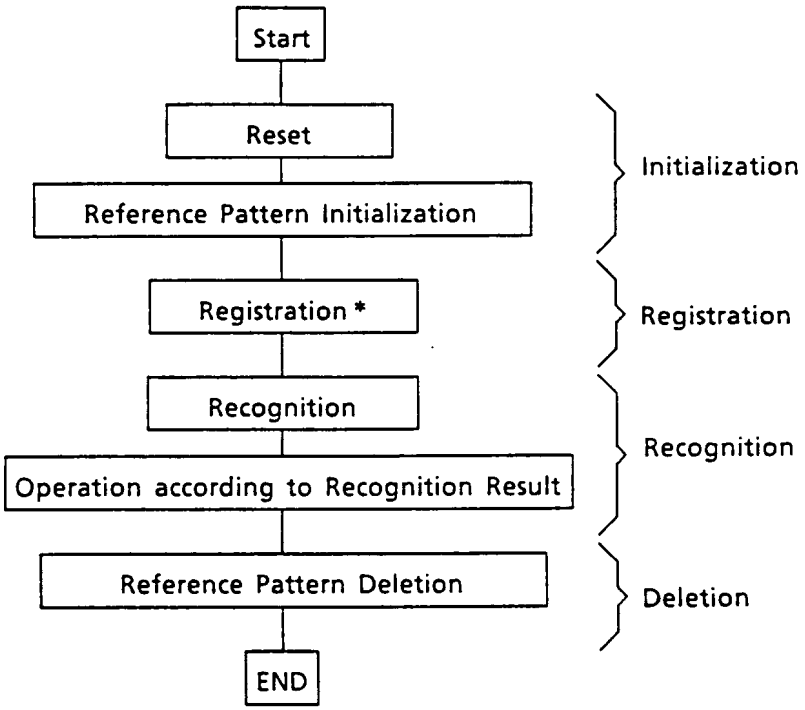


Fig. 5.1 Host System Operation Flow Chart Example

* More than 3 utterance per word may be required in some cases.
See details in 5.3.2 Reference Pattern Registration Command.

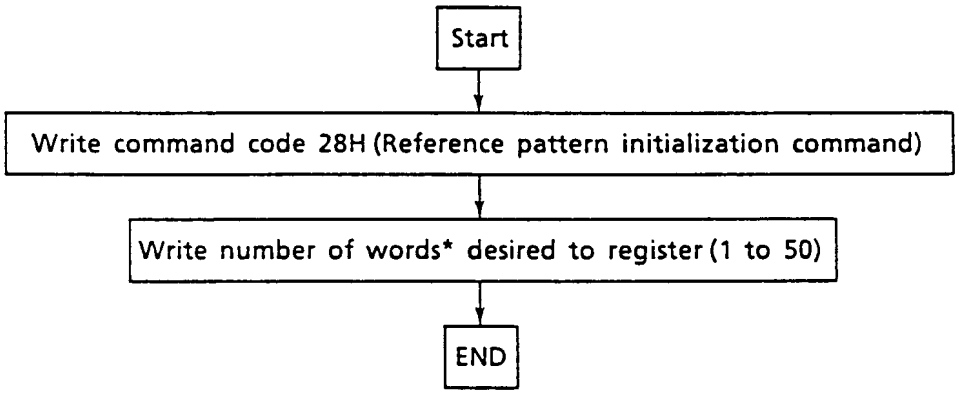
5.3 Command Description

This section describes a host system operational flow chart and a timing diagram for each command.

5.3.1 Reference Pattern Initialization Command (28H)

Reference pattern initialization command initializes reference patterns and CPU scratch-pad memory so that it may enable the device set to be ready for initial registration. System parameters stored in the scratch-pad RAM are initialized. For example, reference pattern bank setting done so far becomes of no effect and only bank 0 recognition command (18H) is effective from then. Reference patterns on external RAMs are initialized to zero from word number 1 to the word number designated by the host system. This command should be executed at least once after power supply to the device set is turned on. The Fig. 5.2 illustrates the host system operational flow chart for the command. Note that the number of words desired to register in the chart is natural number less than or equal to 50.

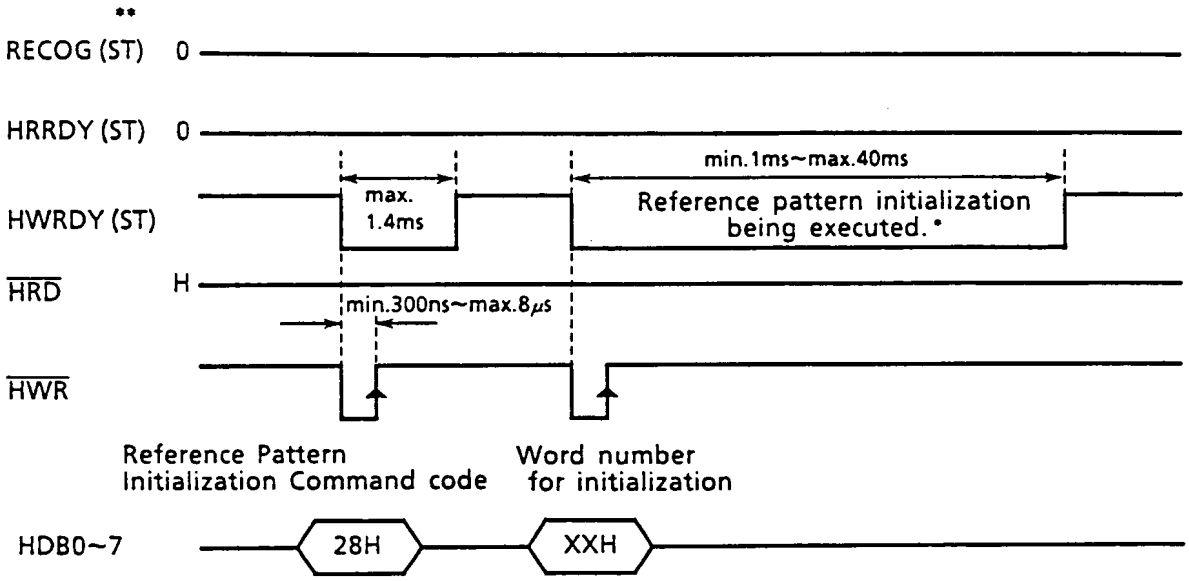
(1) Flow chart



* Since the device set does not examine the validity of the value written as the number of words, the host system program must check it. Otherwise the operation can not be assured.

Fig. 5.2 Reference Pattern Initialization Command Flow Chart

(2) Timing chart



* Avoid writing system reset command while refernce pattern is being intialized. Normal operation can not be guaranteed from then if system reset command is executed within this period of time.

** ST means status in status resister. Status logic on the timing chart is shown by "0" or "1", and the device terminal signal is shown by "L" or "H".

Fig. 5.3 Reference Pattern Initialization Command Timing Chart

5.3.2 Reference Pattern Registration Command (29H)

This command registers voice features on reference pattern RAM segments designated by word numbers. It allows multiple of words to be registration in a single execution. Fig. 5.4 shows the flow chart for a host system. After registration command (29H) is written to command/data register, the device set asks for a word number to be registered. When the word number is written, usually three utterances per word are required to be input through analog input terminal on TC8861F. In some cases where similarity among the spoken three is low, another three utterances for the word is required. Writing "FFH" as a word number starts arithmetic operations to create reference patterns and then output a registration end code (a kind of control code) at their completion. Reading the code leads the device set to the state waiting for another command. The arithmetic operations for more number of words stored require more processing time. Typical processing time is 9 seconds for 30 words, and 16 seconds for 50 words.

(1) Flow chart

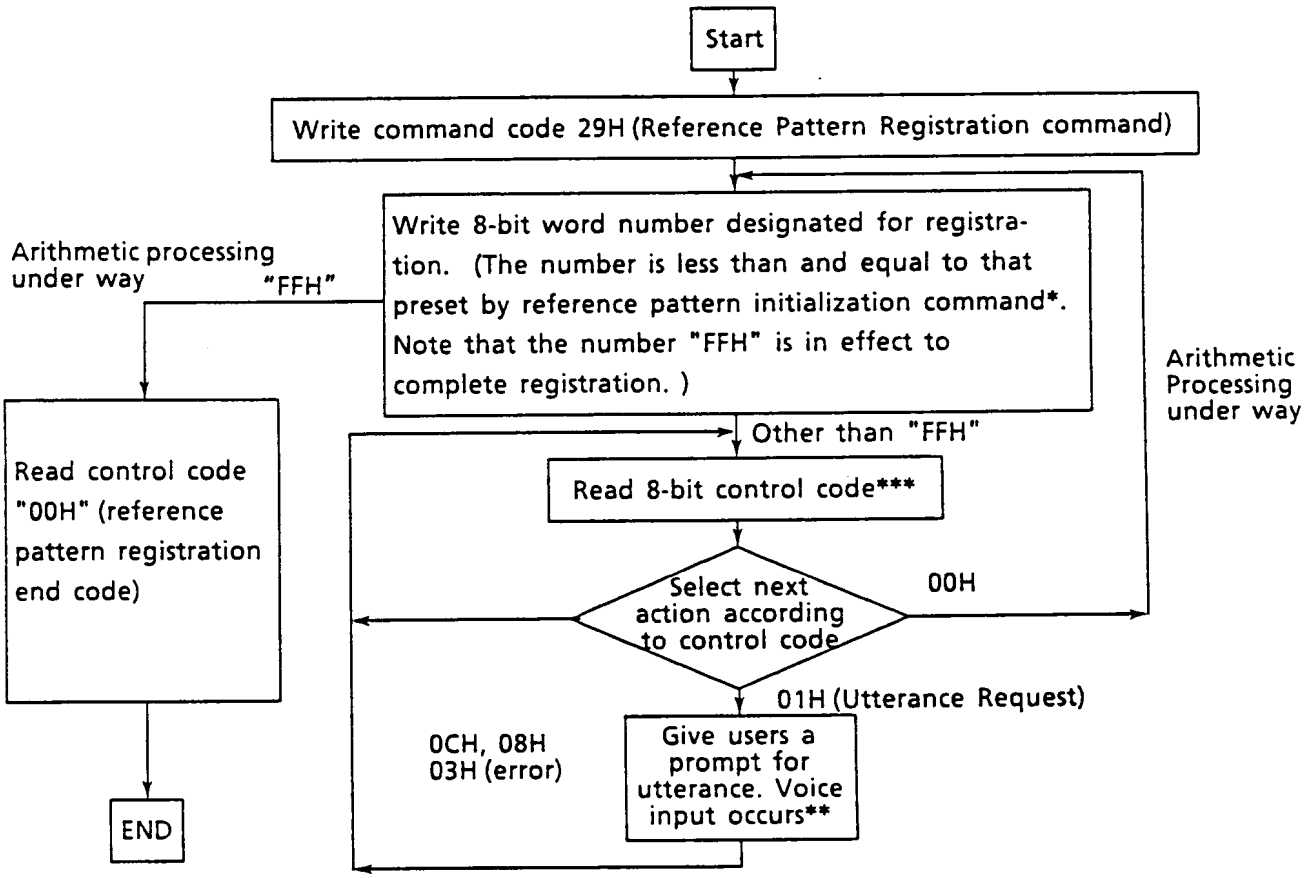


Fig. 5.4 Reference Pattern Registration Command Flow Chart

* Since the device set does not examine the validity of value written as a word number, a host system should guarantee it. Wrong value input will lead to malfunction.

** Three utterances per word are principally required. However more than three utterances are required in the case where similarity among the three is low.

*** Meanings of control codes are referred to 5.4.3 Control Code List.

(2) Timing chart

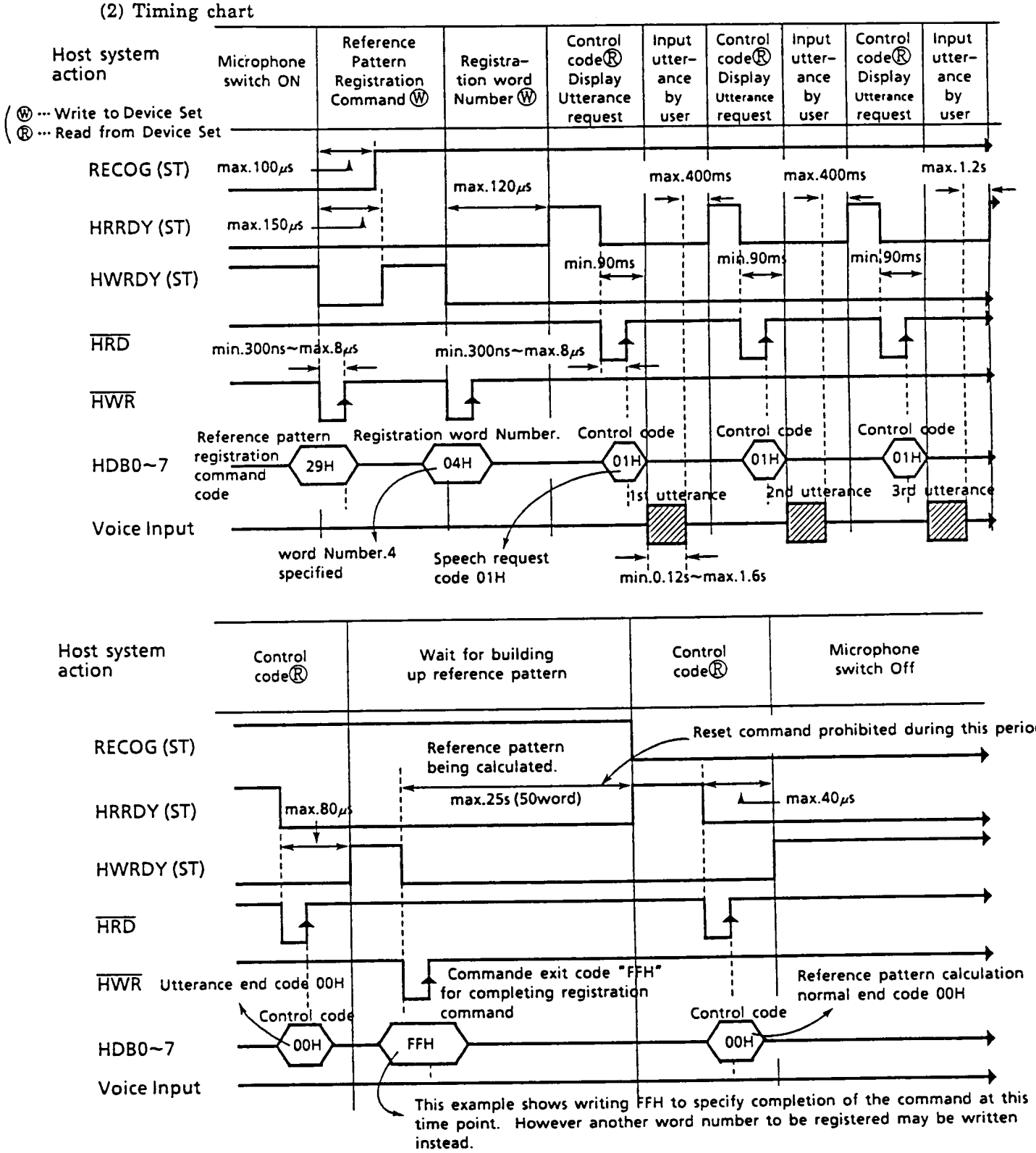


Fig 5.5 Reference Pattern Registration Command Timing Chart (In the case of three times utterance for word

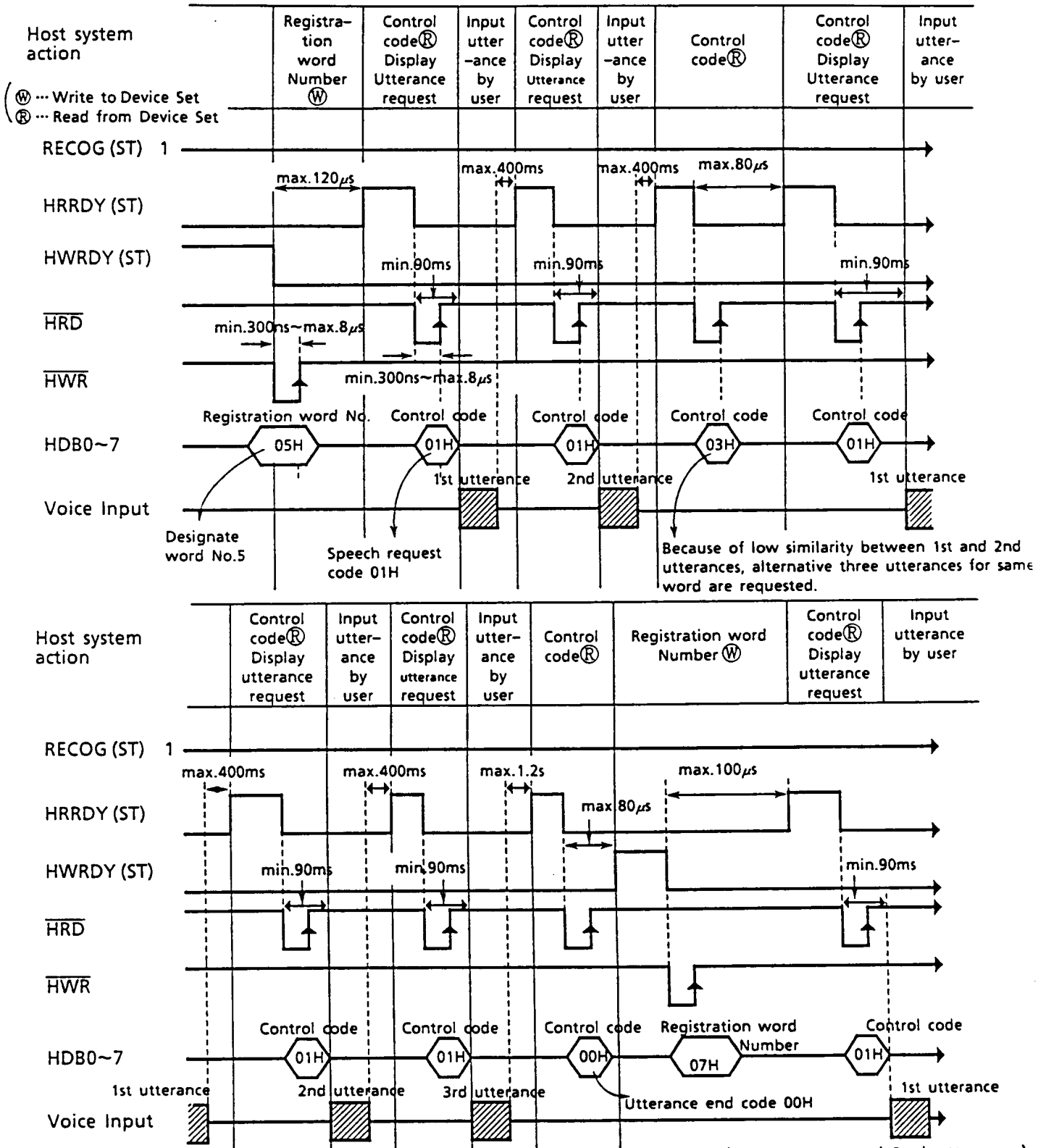


Fig 5.6 Reference Pattern Registration Command Timing Chart (The case of low similarity between 1st and 2nd utterance)

(3) Coutions in Using Reference Pattern Registration.

A host system is required to observe cautions described below when it uses reference pattern registration command. Refer to Fig. 5.5 and Fig. 5.6 for thorough understanding.

- ○ Microphone must be on and ready to transmit voice signal to TC8861F by the time the host system writes word number to be registered. When multiple of words are to be registered sequentially in a single registration command, the microphone may not be turned off word by word. Instead, it is allowed to be kept on all the time when RECOG status flag in the status register takes 1.
- ○ After word number is written, the control code must be read out both to confirm the utterance request code 01H and to give users a prompt for utterance within 90ms from the time point when $\overline{\text{HRD}}$ terminal changes from H to L.
- ○ However, a speaker is prohibited to give utterance in this 90ms time period. The reason is that the device set monitors environmental noise level to determine a threshold for discrimination of voice signal from background noise. This monitor is done immediately before the device set is ready to receive input voice signal. Thus the period is called environmental noise level monitoring period. So microphone must be on to receive background noise then. Also note that every utterance request is accompanied by the monitoring period.
- ○ Nevertheless, a prompt to urge utterance can still be given to speakers within the period. It is because response time of human being is not less than 100ms. Therefore there is no risk that a speaker actually gives utterance in that period even if the speaker recognizes a prompt and utters immediately.
- ○ A prompt given far behind the period may cause the device set to mistake meaningless voice signal for targeted utterance. So a prompt is strongly recommended to be given within the period.
- ○ Once an utterance is given, the device set analyzes the utterance acoustic signal and sets HRRDY status flag to 1 at its completion. The control code is then read out to check whether the given utterance is normally accepted. The control codes 00H or 01H indicates normal completion of voice input activity but the others mean abnormal completion. 00H indicates that three utterances for a word have been successfully given, whereas 01H shows that more utterances for the word are to be given next. Other codes than 00H and 01H urge the host system to read out another control code successively. Then the device set retries a prompt again for the first utterance of the word.

5.3.3 Reference Pattern Deletion Command (2AH)

Reference Pattern Deletion command clears reference pattern data of a specified word into zero. Word numbers and their reference patterns of words other than the specified remains unchanged.

(1) Flow Chart

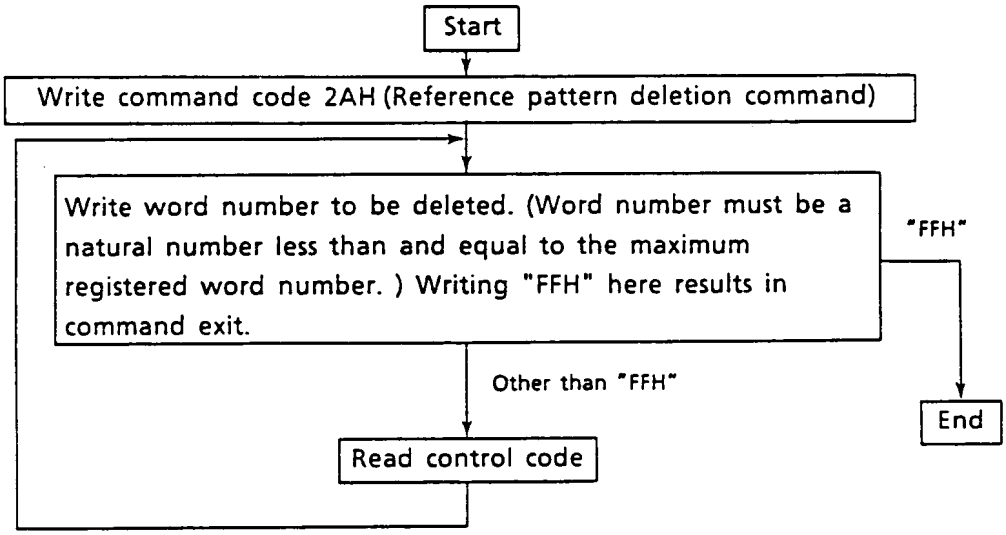
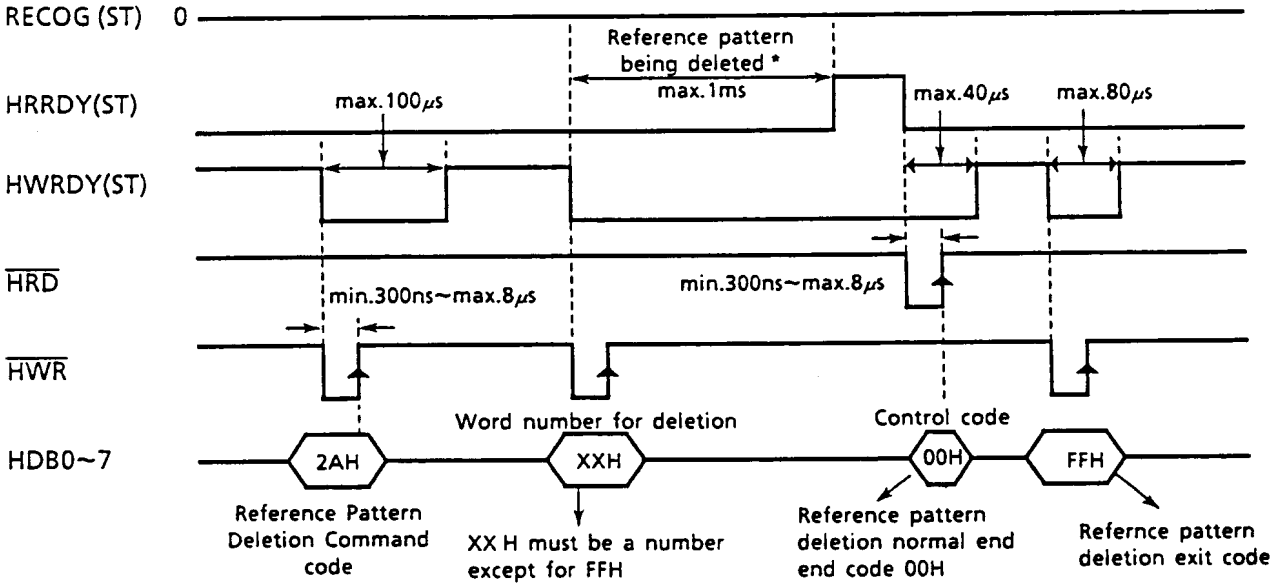


Fig. 5.7 Reference Pattern Deletion Command Flow Chart

(2) Timing Chart



* In deletion process reset command is prohibited from being executed. Reset execution in the period causes malfunction of the device set.

Fig. 5.8 Reference Pattern Deletion Command Timing Chart

5.3.4 Reference Pattern Bank Setting Command (2CH)

This command specifies how many consecutive words are included in 8 different banks. It must be executed at least once before specified-bank recognition commands (19H~1FH). The command may be written any times, but the newest setting is valid.

Reference pattern bank setting command and specified-bank recognition command is a complementary pair for functions with banks. Bank setting command assigns 8 groups of consecutive word numbers to 8 banks. Specified-bank recognition command uses those bank numbers in order to compare input voice with words in designated banks when input voice is previously known as one of them.

The device set uses up to 8 banks. Every bank must be set in terms of the number of consecutive words in the bank setting command even if only some of 8 are used. For instance, when only 3 banks are used, the other 5 must also be set to "0" as the number of words respectively. On the other hand specified-bank recognition command execution for a bank with no word specified leads the device set, without any recognition activity, to waiting-command state with CFER bit "1" in status register.

If the total sum of the 8 numbers of words for 8 banks exceeds 50, the device set returns a control code (a return code) other than "00H". Here the current bank setting is of no effect, and the previous bank setting is preserved.

If the total sum exceeds the maximum registered word number, specified-bank recognition copes with words of up to the maximum registered word number.

On the contrary, if the total sum comes less than the maximum registered, recognition commands deals with only words included by 8 banks.

(1) Flow Chart

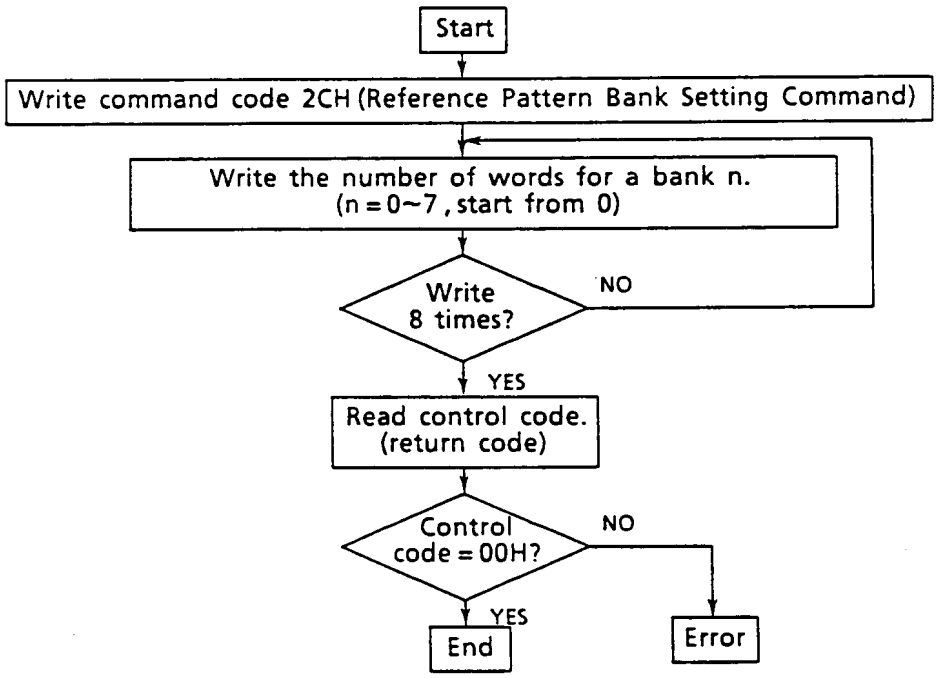


Fig. 5.9 Reference Pattern Bank Setting Command Flow Chart

(2) Timing Chart

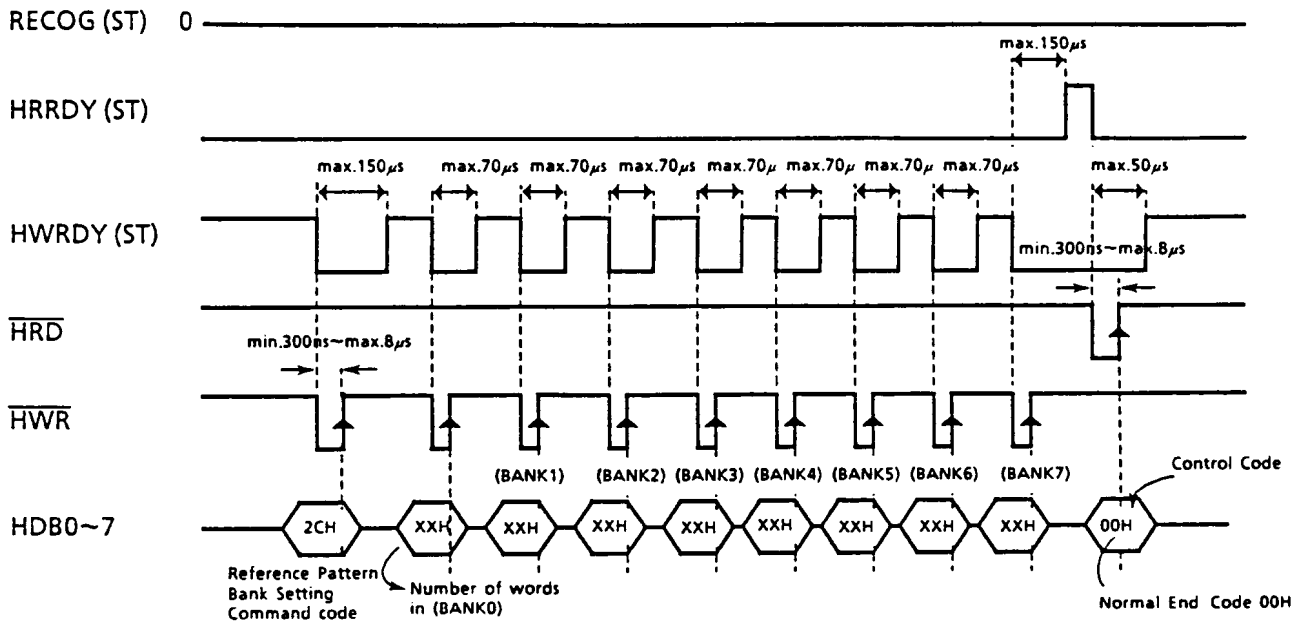


Fig 5.10 Reference Pattern Bank Setting Command Timing Chart

5.3.5 TC8861F Filter Offset Compensation Command (38H)

The command compensates for TC8861F filter offset.

Offset values vary by individual TC8861F or its assembly condition. Offset degrades frequency analysis accuracy of TC8861F and then reduces recognition performance. To eliminate this harmful influence, TC8861F is equipped with offset compensation function. The command executes the function on TC8861F. This function is automatically executed every time the reset command or stand-by on command is operated or when power supply is turned on. However users are recommended to execute this command explicitly at about 5 minute interval in case the device set is operated continuously for more than 5 minutes without any interruption by either the reset command or the stand-by on command.

(1) Flow Chart

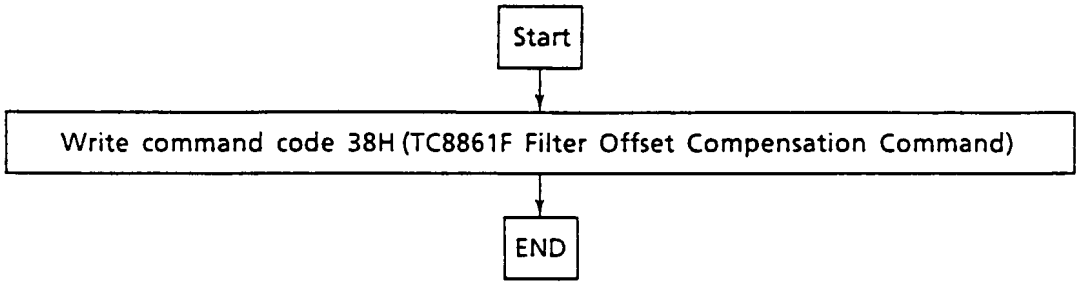


Fig. 5.11 TC8861F Filter Offset Compensation Command Flow Chart

(2) Timing Chart

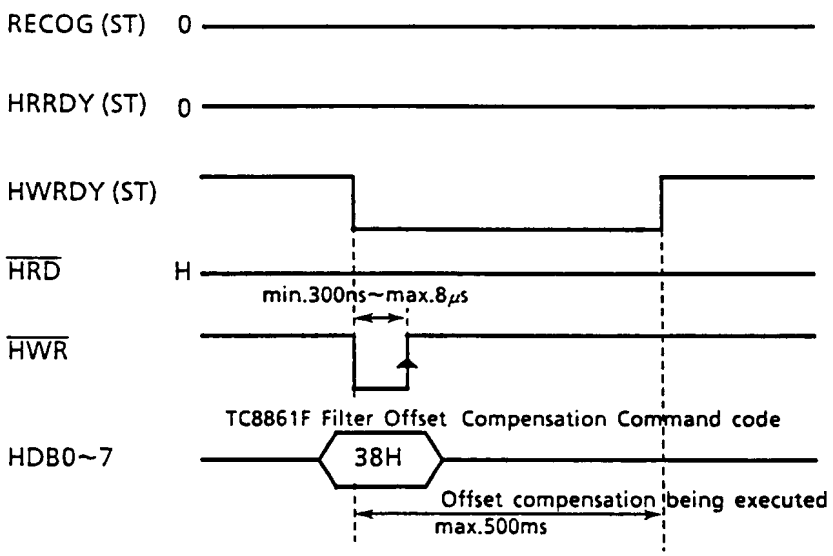


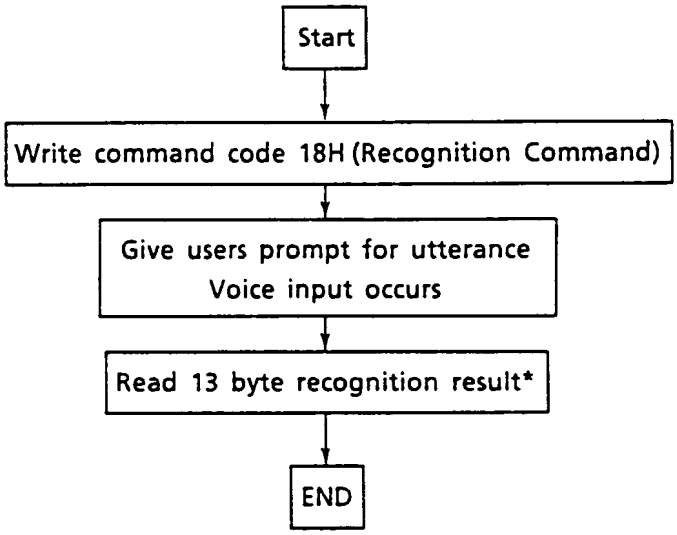
Fig 5.12 TC8861F Filter Offset Compensation Command Timing Chart

5.3.6 Recognition Command (18H)

The command performs recognition of input voice on vocabulary reference patterns registered by reference pattern registration command. As a result 13byte data returns back to a host system.

If the reference patterns don't exist (the case happens if any registration has not been executed after reference pattern initialization), the recognition command does not proceed any longer and results in command waiting state with status register CFER bit "1".

(1) Flow Chart



* Refer to 5.4.1 Recognition Result Data Format

Fig. 5.13 Recognition Command Flow Chart

Following points must be strictly observed in the procedure until start time point of voice input after writing recognition command. At least 90ms must be needed until starting time point of voice input after RECOG status changes to "1". Refer Fig. 5.14 for understanding. In this period, the device system determines parameters for discriminating voice signal from environment noise signal by monitoring environment noise signal from a microphone. Therefore a microphone should be operated in this period and a host system forbids users to enter voice to the device set. On the other hand, this 90ms period is suitable for giving users a prompt to start utterance. Even if the prompt is acknowledged by users in the 90ms period, the user's utterance period doesn't overlap forbidden period because human's reaction time is over 100ms.

(2) Timing Chart

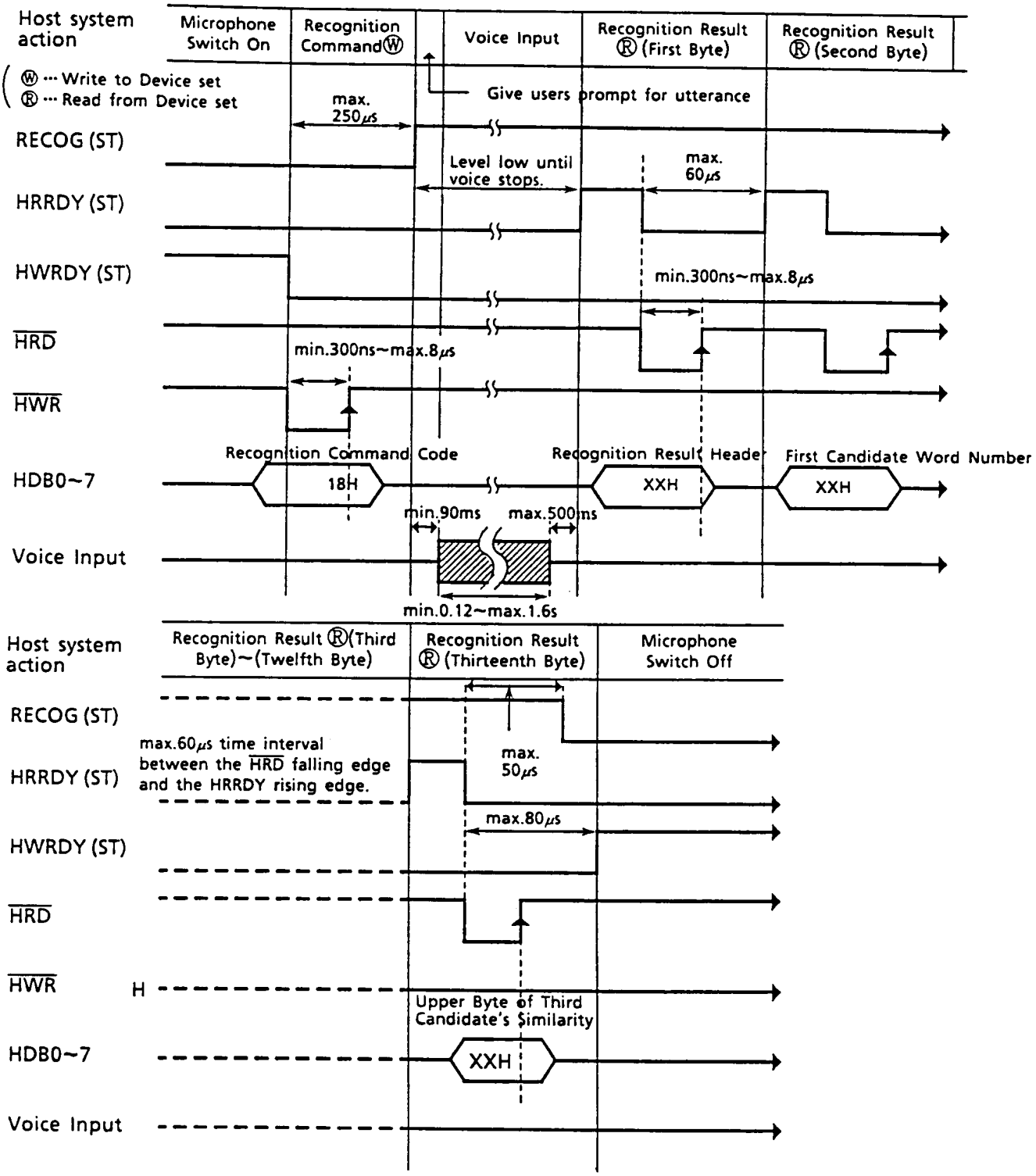


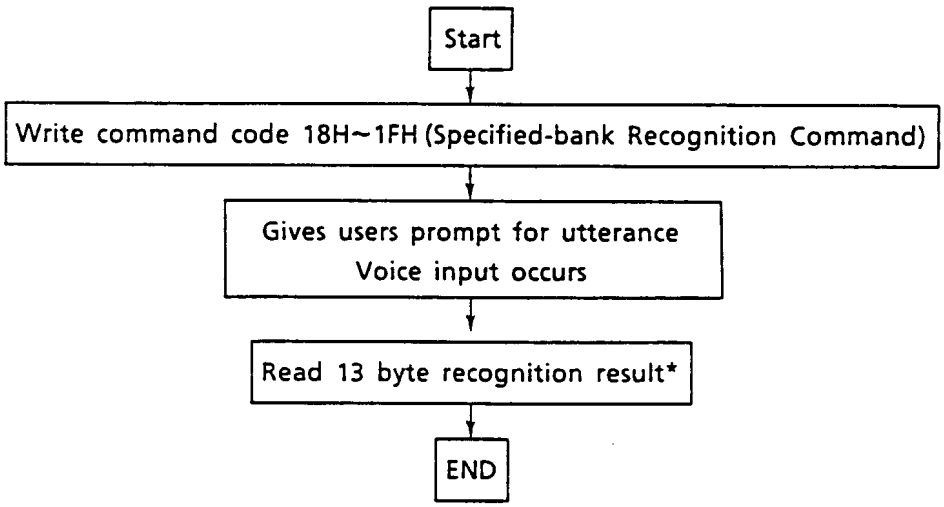
Fig 5.14 Recognition Command Timing Chart

5.3.7 Specified-Bank Recognition Command (18H~1FH)

The device set is provided with the recognition function which employs only a portion of the whole reference patterns as a pattern matching object. That function is called specified-bank recognition command. The command is complementary to reference pattern bank setting command. The former command requires a portion of reference patterns to be defined beforehand as a bank by the latter command. Up to 8 banks can be set and they are numbered from 0 through 7. The former command executes recognition with segment of reference patterns specified by bank number. Command code for bank 0 is 18H, that for bank 1 is 19H, that for bank 2 is 1AH, and that for bank 7 is 1FH.

If bank setting has not be performed after reference pattern initialization command, all reference patterns registered are treated as involved in bank 0. In this case only recognition command 18H is valid and other specified-bank recognition command 19H~1FH are of no effect.

(1) Flow Chart



* Refer to 5.4.1 Recognition Result Data Format

Fig. 5.15 Specified-Bank Recognition Command Flow Chart

Following points must be strictly observed in the procedure between the command writing and voice input. Fig. 5.16 will be helpful in understanding. A host system must organize the procedure in such a way that voice input occurs at least 90ms later than the time point when RECOG status flag turns from 0 to 1. The device set monitors environmental noise level during that period so as to determine parameters for voice detection. Therefore a microphone must be on, and moreover, utterance must be prohibited during the whole period. On the other hand, a prompt for utterance is given to users most suitably in that time period. Even though users recognize the prompt and try to utter immediately, there is no risk that actual utterance is given in the period. It is because response time of human being is not less than 100ms.

(2) Timing Chart

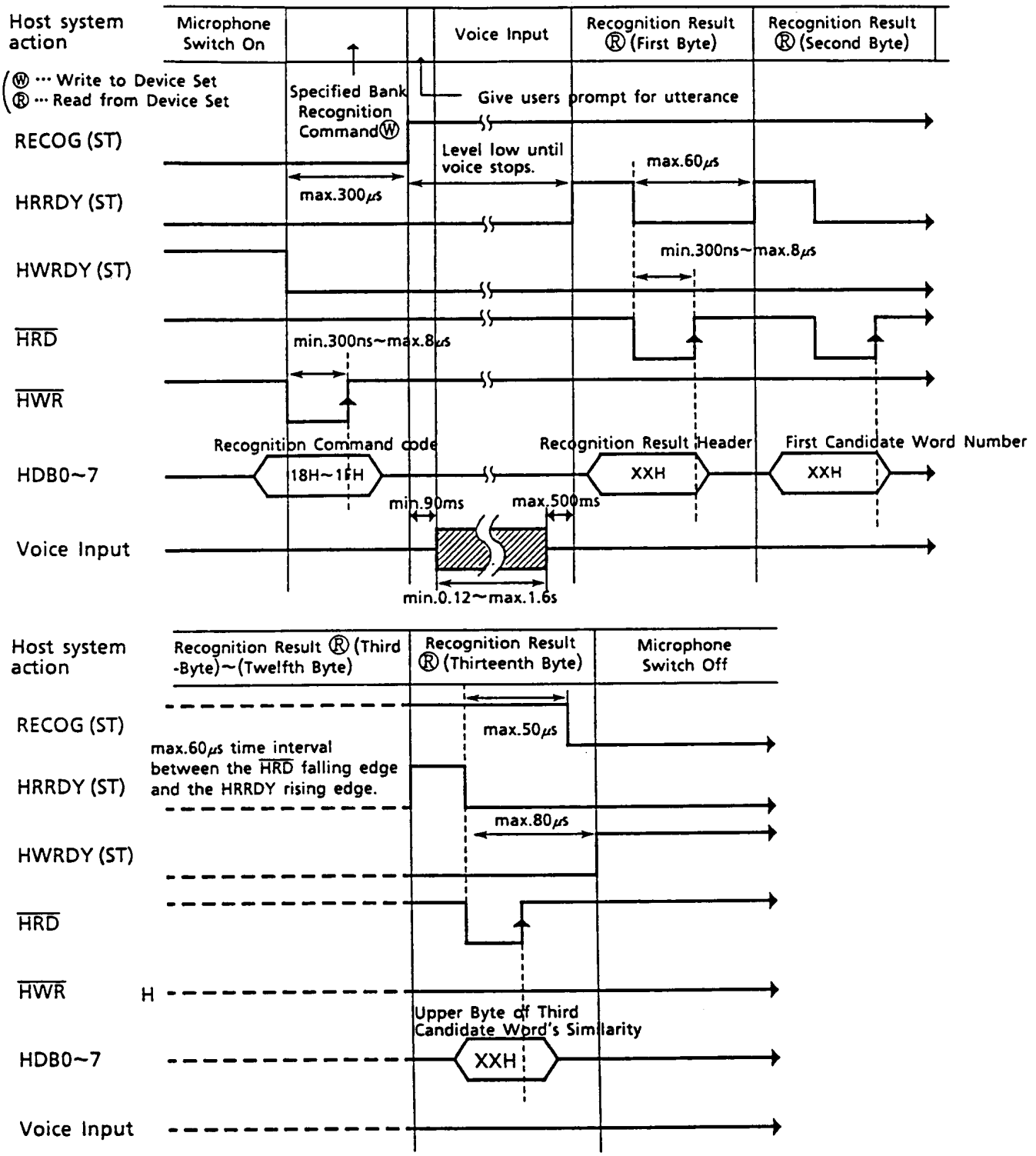


Fig 5.16 Specified-Bank Recognition Command Timing Chart

5.3.8 Reference Pattern Down Load Command (22H)

A host system can get reference patterns by reference pattern up load command. When other reference patterns already exist in external static RAM, this reference pattern down load command replaces the already existent reference patterns with other patterns transferred from the host system. A reference pattern is transferred in the format described in 5.4.4.

(1) Flow Chart

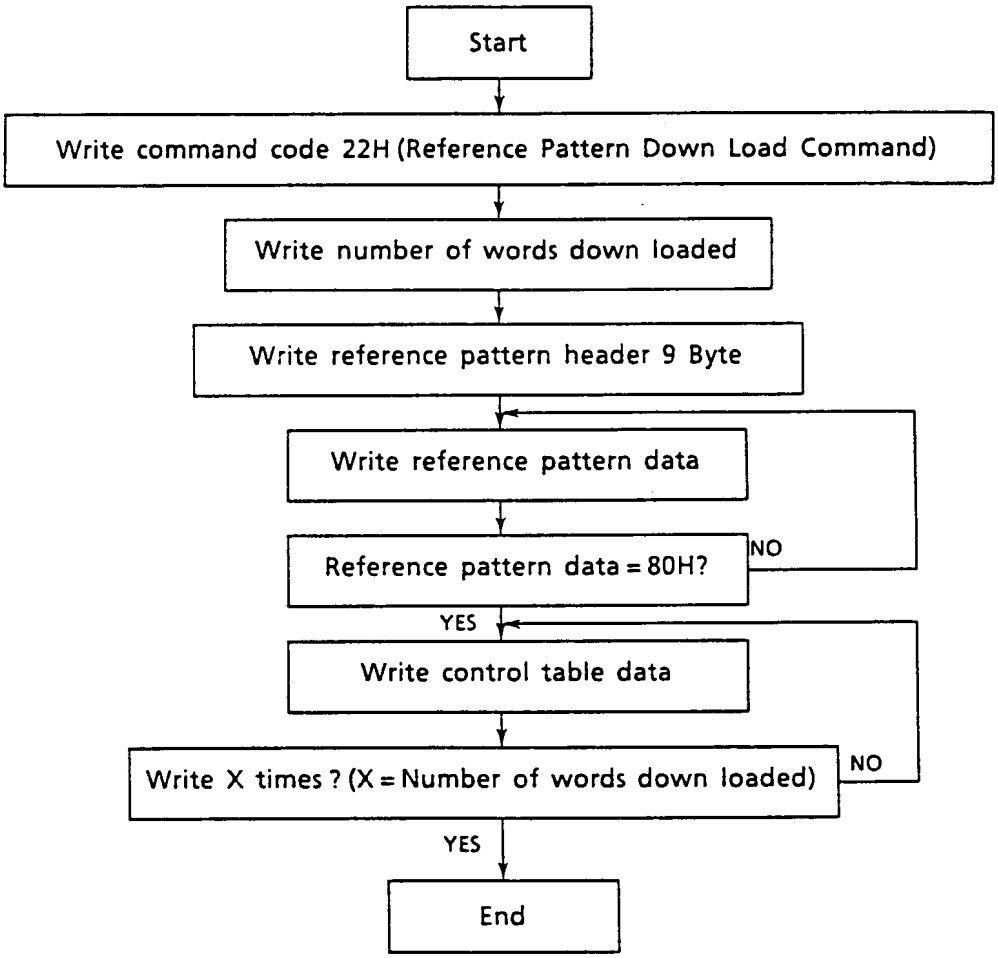


Fig 5.17 Reference Pattern Down Load Command Flow Chart

(2) Timing Chart

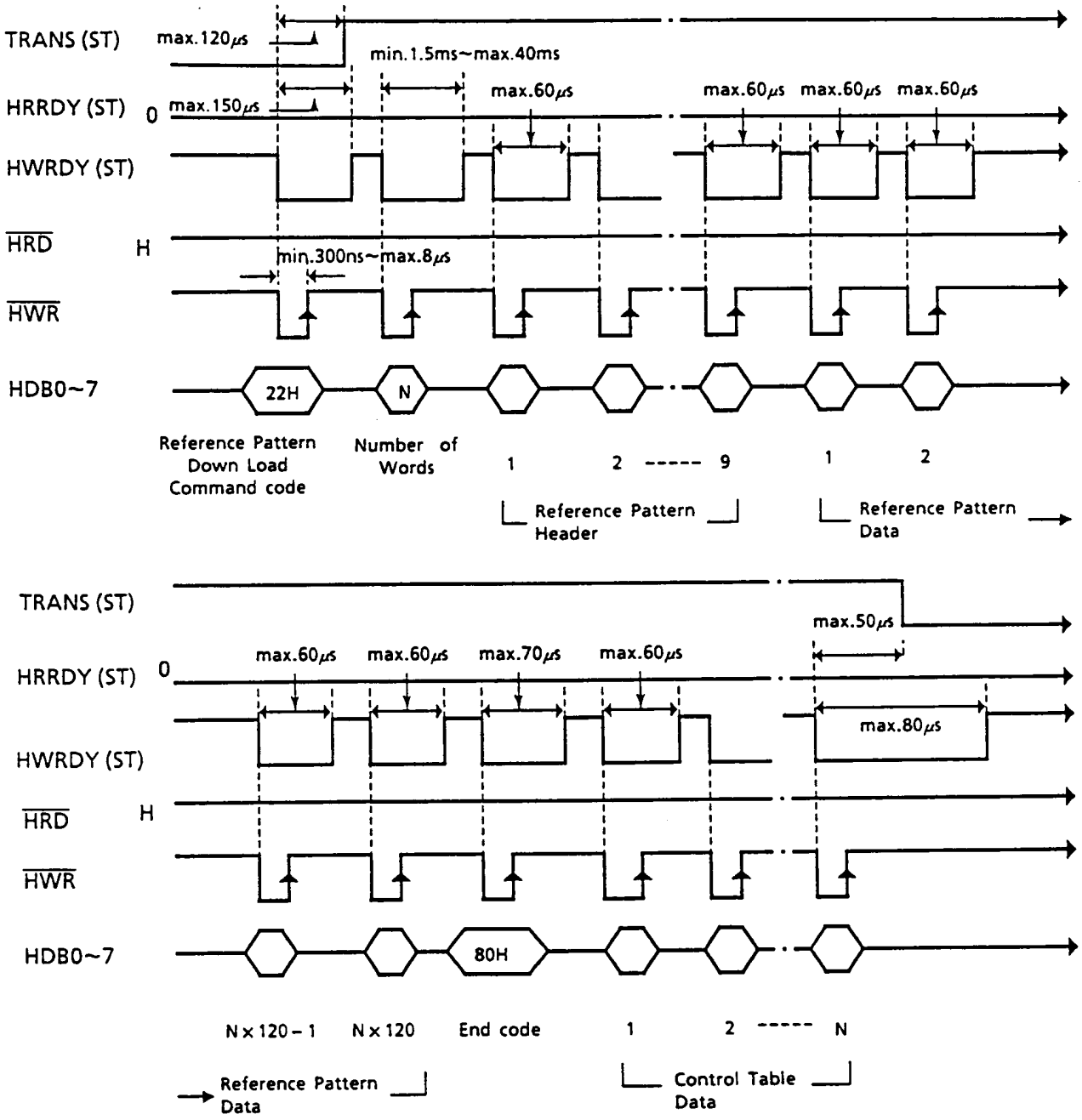


Fig 5.18 Reference Pattern Down Load Command Timing Chart

5.3.9 Reference Pattern Up Load Command (23H)

This command transfers reference patterns to a host system. When reference patterns don't exist in external static RAM, this command leads the device set to command waiting state without any processing.

(1) Flow Chart

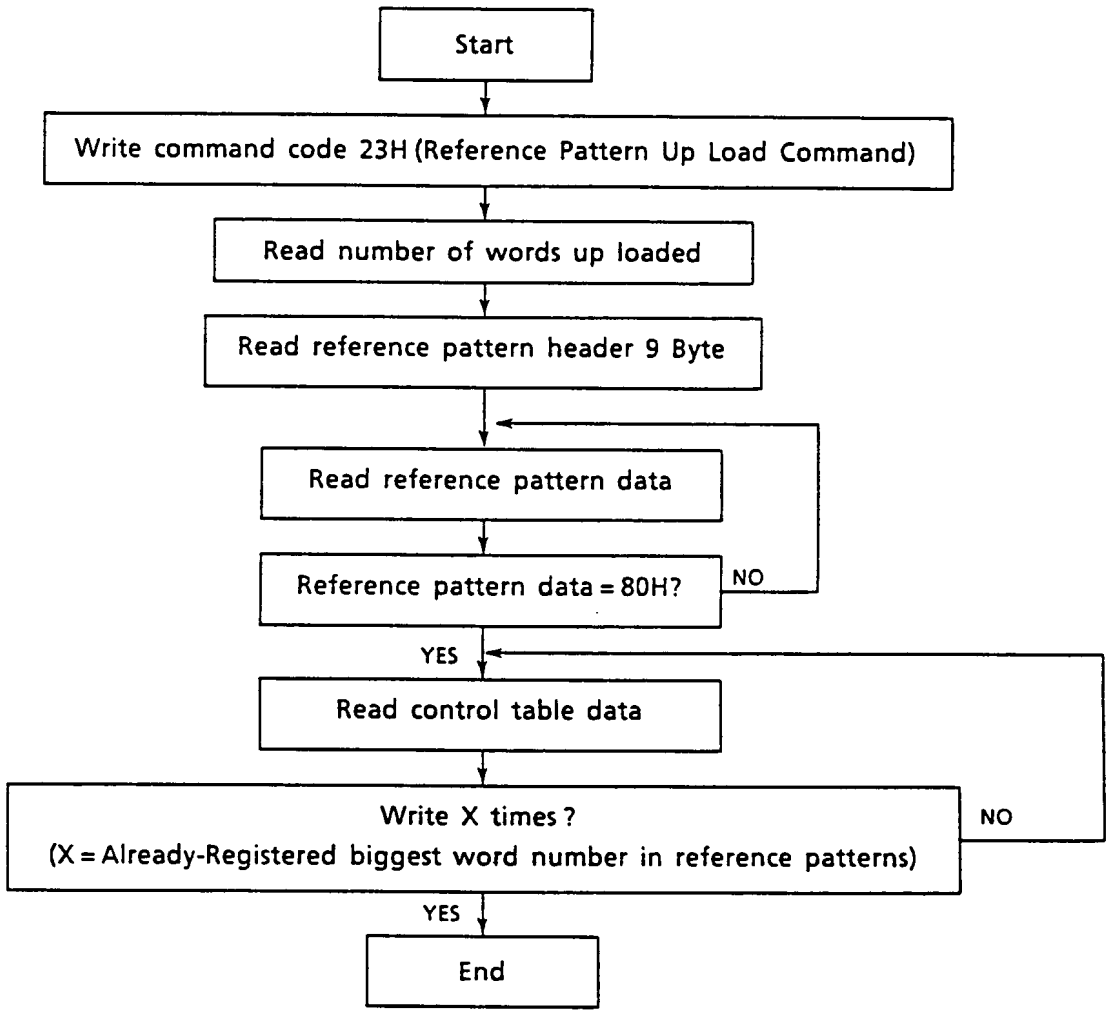


Fig 5.19 Reference Pattern Up Load Command Flow Chart

(2) Timing Chart

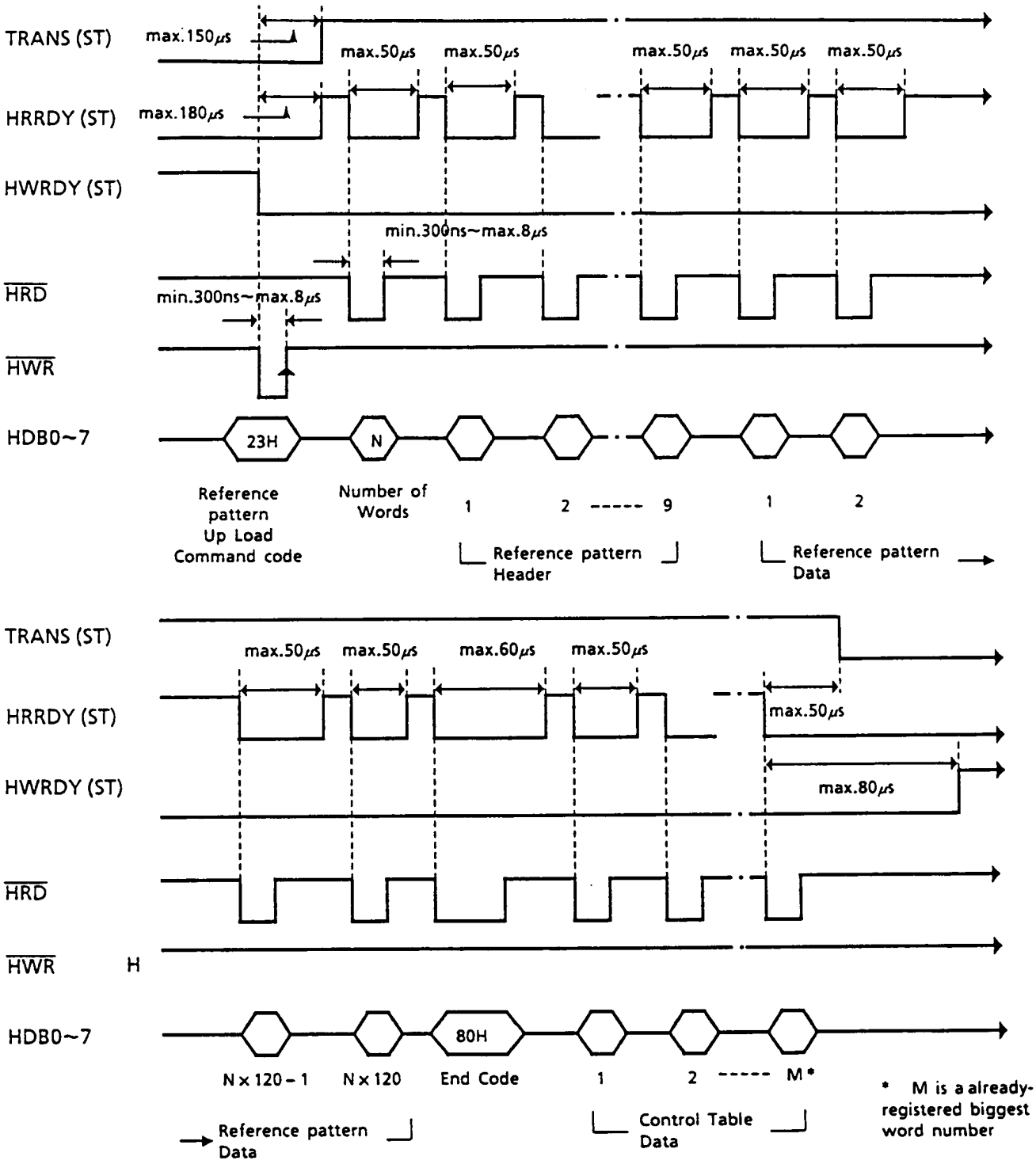


Fig 5.20 Reference Pattern Up Load Command Timing Chart

5.3.10 Filter Data Up Load Command (37H)

This command sends filter data to a host system. The filter data are created by recognition command just before executed. The filter data are of variable length with end code FFH. The filter data format is described in 5.4.5.

(1) Flow Chart

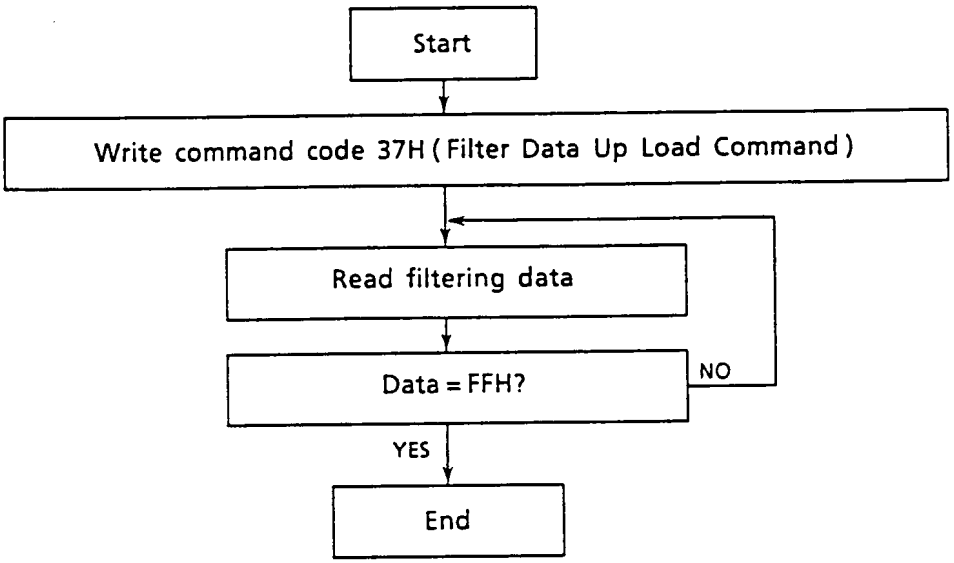


Fig 5.21 Filter Data Up Load Command Flow Chart

(2) Timing Chart

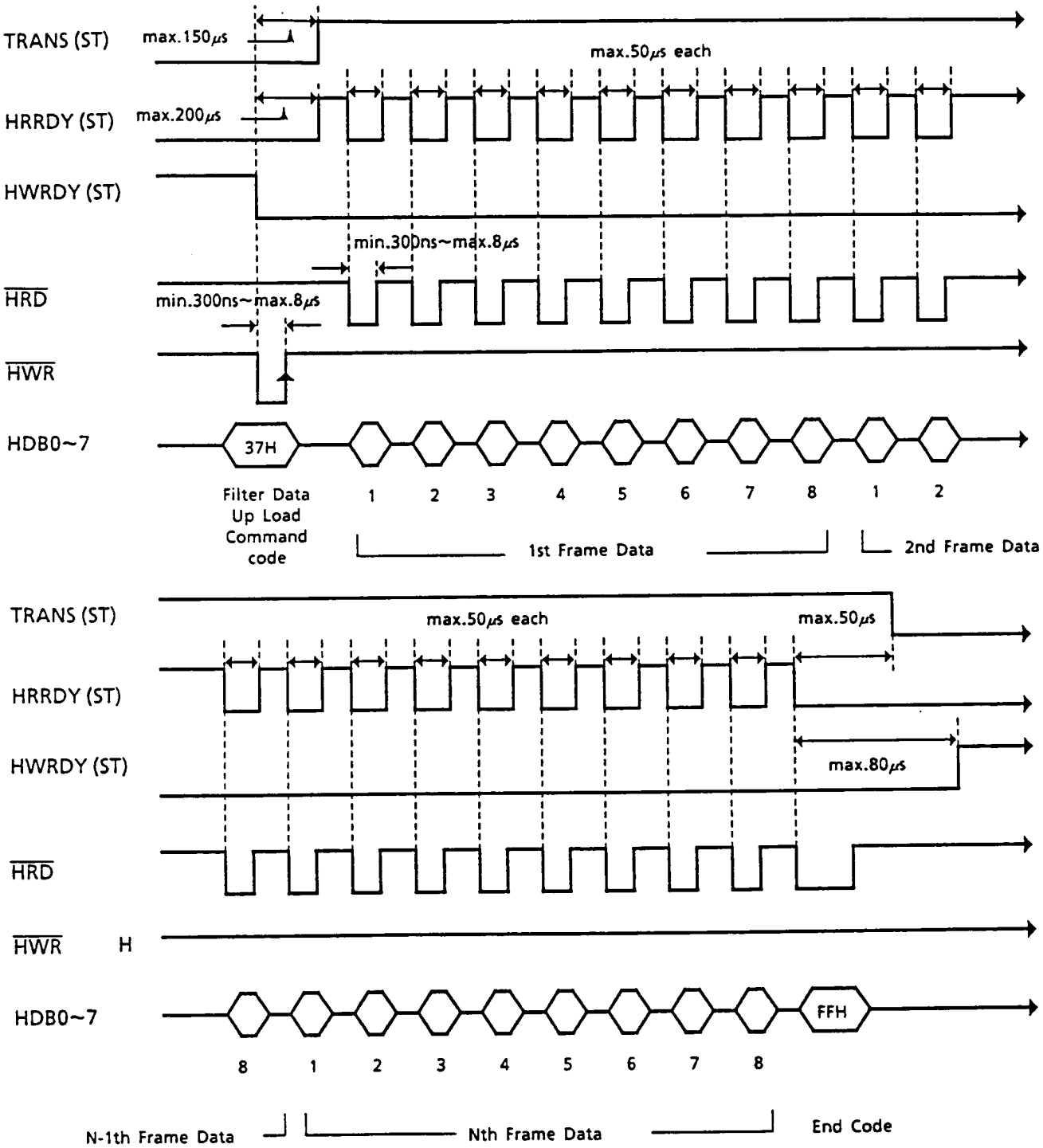


Fig 5.22 Filter Data Up Load Command Timing Chart

5.3.11 System Reset Command, System Stand-by Off Command

Reset command is used to release the device set from hung up state to normal operation state. It is also used as a stand-by off command to release the power saving mode when the device is in the mode. In both cases it initializes the device set, but the device set saves all previous data in its scratch-pad RAM and its reference pattern RAM. Actual actions are as follows. The command

- Initializes all registers on each device.
- Clears all flags on each device.
- Resets program counter (PC) on TC8864F-00 to 000H and then starts program from PC=000H.
- Compensates for TC8861F filter offset.
- Leads the device set to command waiting state.

During these reset command action, status register flag RESET keeps "1". So a host system operates as described below.

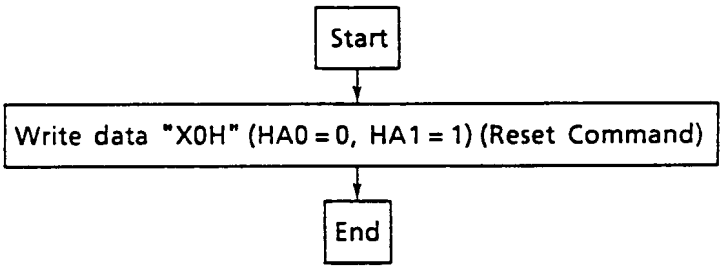


Fig. 5.23 Reset Command Flow Chart

5.3.12 System Stand-by On Command (Reset/Stand-by Register)

Stand-by On command leads the device set to power saving mode, where TC8861F, TC8864F-00 hold their system clock to realize total device set power supply current less than 10μA. The command allows the device set to preserve their system parameters on both internal RAMs and external reference pattern RAMs. The mode can be detected by status register flags STBY="1" and RESET="1". Note that RESET flag is also 1 in the power saving mode. Stand-by off command releases the device set from power saving mode.

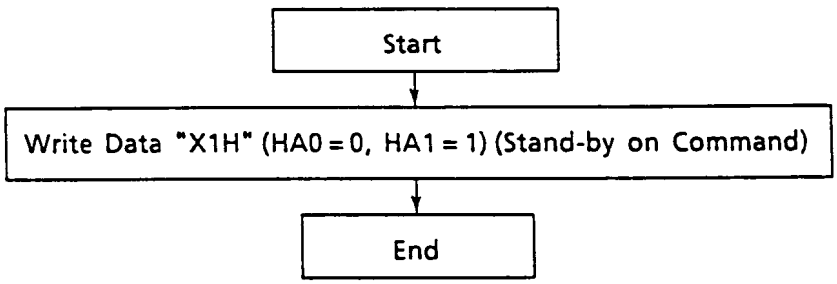


Fig 5.24 Stand-by on Command Flow Chart

5.3.13 Reset Timing

Fig.5.25 shows reset command timing.

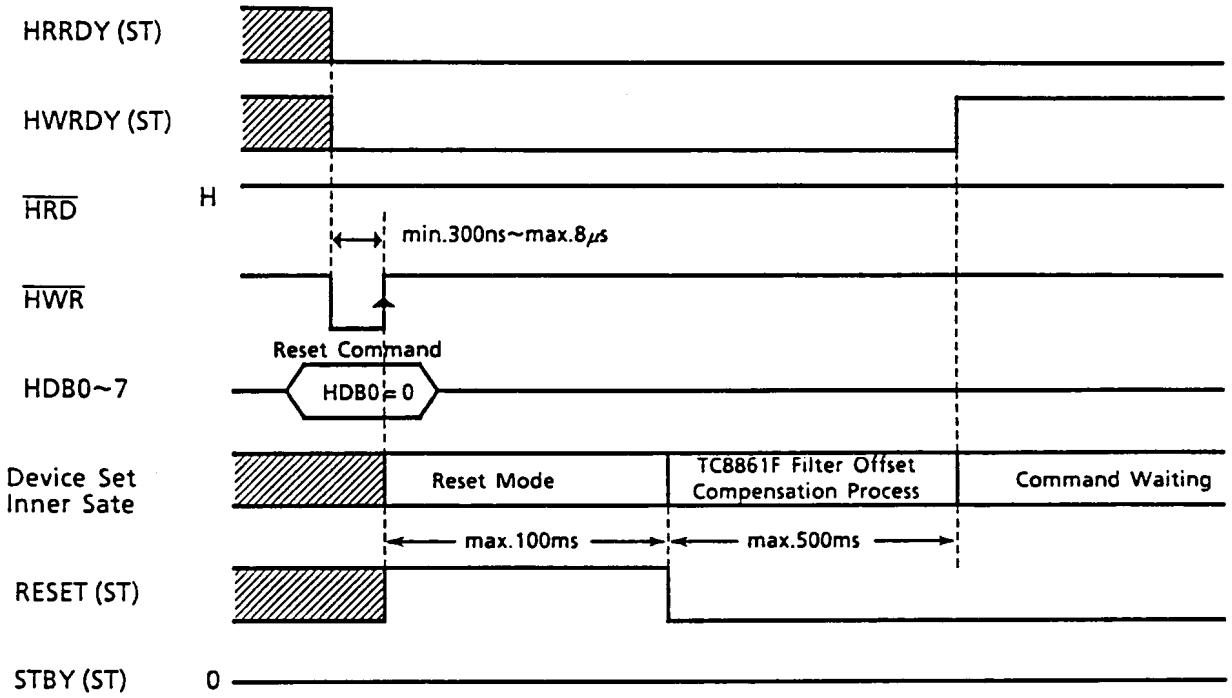


Fig 5.25 Reset Timing Chart (HA1 = 1, HA0 = 0, $\overline{HCS}$ = 0)

5.3.14 Stand-by On/Off Timing

Fig.5.26 shows stand-by on / off command timing.

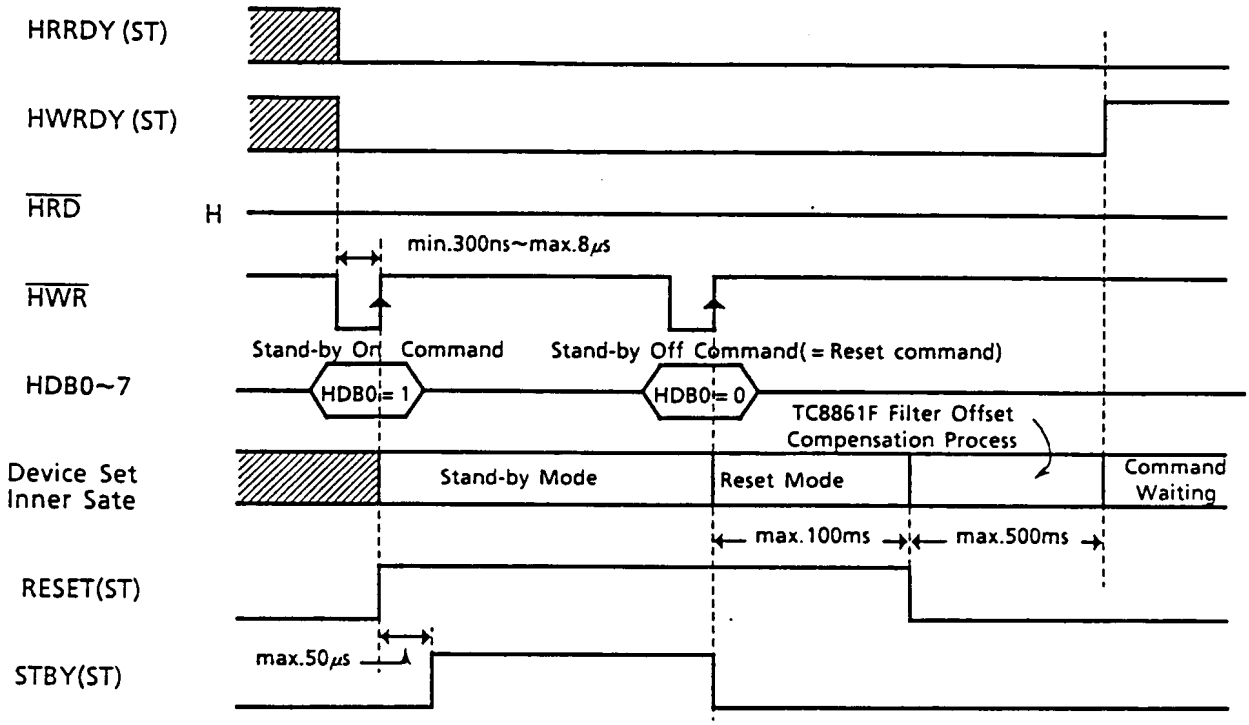


Fig 5.26 Stand-by On/Off Timing Chart (HA1 = 1, HA0 = 0, $\overline{HCS}$ = 0)

5.3.15 System Transition Timing When Power Supply Turns On

Fig.5.27 shows some terminal timing when power supply turns on. Even though device set becomes reset mode in the transition period, reset command must be executed once for complete system initialization.

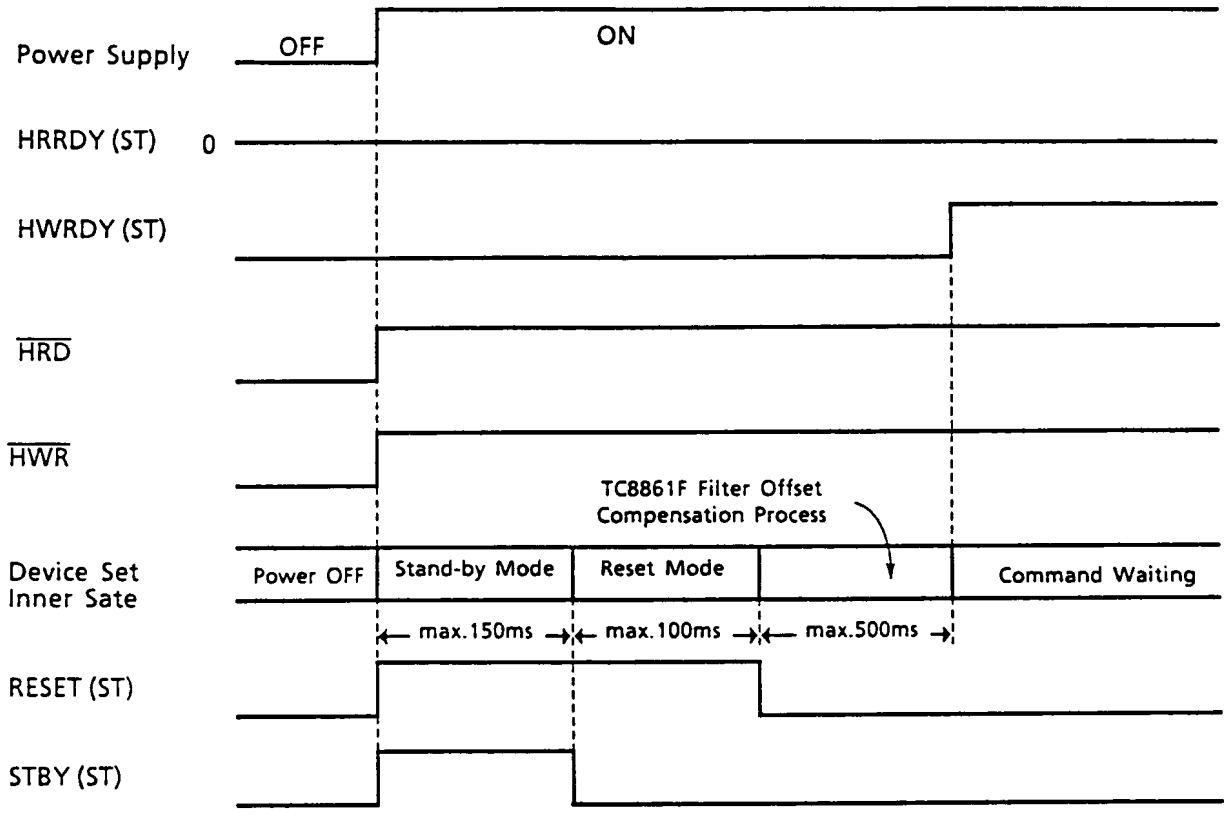


Fig 5.27 System Transition Timing Chart When Power Supply Turns On

5.3.16 Notes on system Reset command Usage.

With a few exceptions stated below, a host system can operates reset command any time even when the device set performs a certain process. The process interrupted by reset command still allows following commands to operate with previous device-set operation history alive, because the reset command can preserves essential system parameters of scratch-pad RAM and reference pattern RAM safely.

This data preservation capability provided by the reset command offers convenience to handle the device set in various applications. Several examples include cases where a host system intends to;

(1) Quit voice input waiting state in recognition command or reference pattern registration command forcefully when the voice will not come in.

(2) Quit infinite loops of recognition command, if it happens.

(3) Stop processes on their way driven by wrong commands.

(4) Recover from hung-up state in host computer program development.

Two exceptions are the time period for actual arithmetic calculation in reference pattern registration command, and the whole time period in reference pattern deletion command.

As for reference pattern registration command, execution of reset command must be prohibited in the time period between writing FFH and reading control code (end code)(See Fig. 5.4). There actual arithmetic calculation for reference patterns is performed from three utterances per word and the reference patterns are transmitted to external SRAM. If it is nevertheless executed in the prohibited period, none of reference patterns are guaranteed.

However, as long as the reset command is executed in periods other than the prohibited even during reference pattern registration, reference patterns being developed as well as those already prepared can be restored completely. The following paragraph explains sequences to restore patterns.

If reset command enters before "FFH" is input as a word number, sets of three utterances per word just already spoken are still alive in the scratch-pad memory. But the problem is that reference patterns for the words are not completed yet because actual arithmetic calculation is suspended due to reset operation. To complete them, the second registration command must be executed on command waiting state immediately after the reset command execution. On the first prompt for word number entry in the second registration command, writing "FFH" must be operated to execute actual arithmetic calculation with those utterances spoken in the first registration command.

As for reference pattern deletion command, reference pattern segment data specified with a word number by the command is not guaranteed when reset command is executed on its half way.

5.4 Data Format

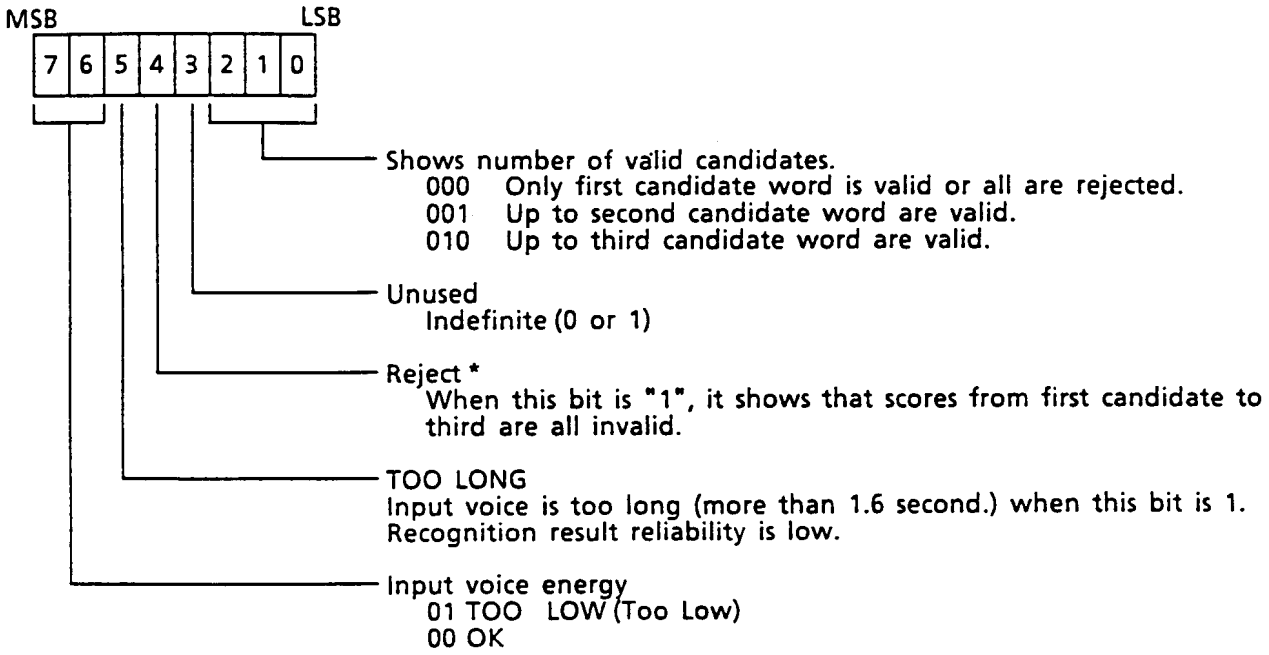
5.4.1 Recognition Result Data Format

Recognition Result Header (Refer to description in the next page)	
First Candidate Word Number	
Second Candidate Word Number	
Third Candidate Word Number	
First-Candidate Word Similarity Score	(Lower Byte)
First-Candidate Word Similarity Score	(Middle Byte)
First-Candidate Word Similarity Score	(Upper Byte)
Second-Candidate Word Similarity Score	(Lower Byte)
Second-Candidate Word Similarity Score	(Middle Byte)
Second-Candidate Word Similarity Score	(Upper Byte)
Third-Candidate Word Similarity Score	(Lower Byte)
Third-Candidate Word Similarity Score	(Middle Byte)
Third-Candidate Word Similarity Score	(Upper Byte)

13 Bytes Data

Fig. 5.28 Recognition Result Data Format

5.4.2 Recognition Result Header Format



* Reject Flag "1" indicates reliability of recognition result is low.

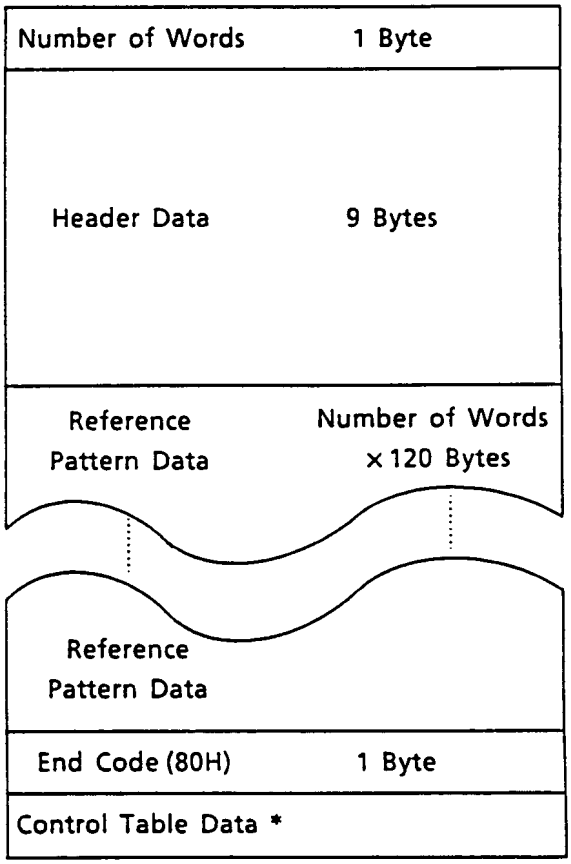
Fig. 5.29 Recognition Result Header Format

5.4.3 Control Code List

Table 5.2 Control Code List

Value	Meaning
00H	Input voice is normal.
01H	Utterance of word is requested.
03H	Second or third utterance has much difference with first word in registration mode, thus correct reference pattern of the word can not be made.
08H	Input voice is too long (more than 1.6 second.)
0CH	Input voice is too low in energy.

5.4.4 Structure of Reference Pattern



* Data langth corresponds to already-registered biggest word number (bytes) in reference pattern upload command. On the other hand it corresponds to number of words (bytes) located in the first byte of the reference pattern format in reference pattern download command.

Fig. 5.30 Reference Pattern Format

5.4.5 Filter Data Format

Fig. 5.31 shows filter data format.

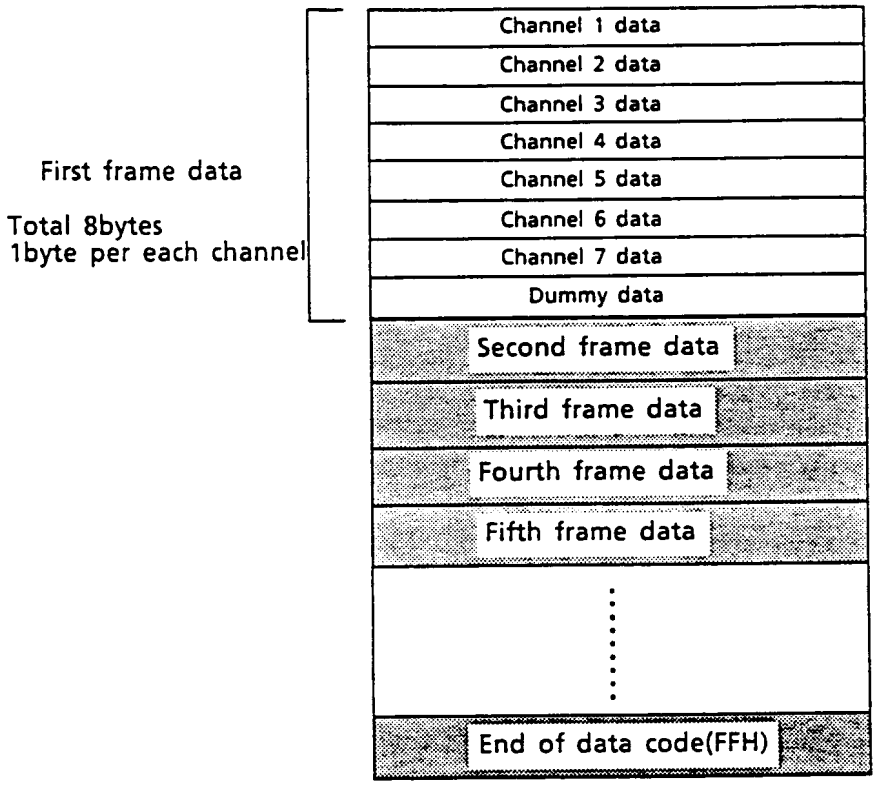


Fig. 5.31 Filter data format

6. Detail Description on Each Device

6.1 TC8861F (Acoustic Processing Analog Device)

6.1.1 Functional Description and Block Diagram

The device performs acoustic processing for analog voice input signal to prepare acoustic feature extraction parameters. The block diagram is presented in Fig. 6.1 and signal processing flow is described in following paragraph.

Analog voice signal fed through either MIN terminal or LIN terminal is amplified first in either a microphone amplifier (Gain=26dB) or a line amplifier (Gain=15dB) and then is amplified again in a preamplifier. The preamplifier gain can vary by a variable resistor (RVI) from 0 dB (RVI=450kΩ) to 20 dB (RVI=0kΩ). The amplified signal is then fed to high pass filter (HPF) to emphasize high frequency component in consonant. Next, the signal is input into 7 channel filter bank for frequency analysis. Each filter bank channel consists of a supplementary low pass filter (LPF), a band pass filter (BPF), a rectifier and a smoothing low pass filter. The supplementary LPF and the BPF extracts a portion of signals lying in pass-band of frequency range between f_L and f_H shown in Fig. 6.1 BPF block.

Then the rectifier rectifies the BPFed signal in an absolute manner and the smoothing LPF (cut frequency=50Hz) smooths the rectified signal. Therefore the output from the smoothing LPF represents averaged amplitude time series of waveform in pass-band frequency region uniquely determined for each filter channel.

Single analog-to-digital converter (A to D) digitizes 7 outputs of smoothing LPFs from a multiplexer one by one. The A to D digitizes each channel every 20ms. The input-output digitizing characteristic in the A to D shows non-linearity with 8bit compressed output. The analog input signal full range for the A to D is approximately 2 (V).

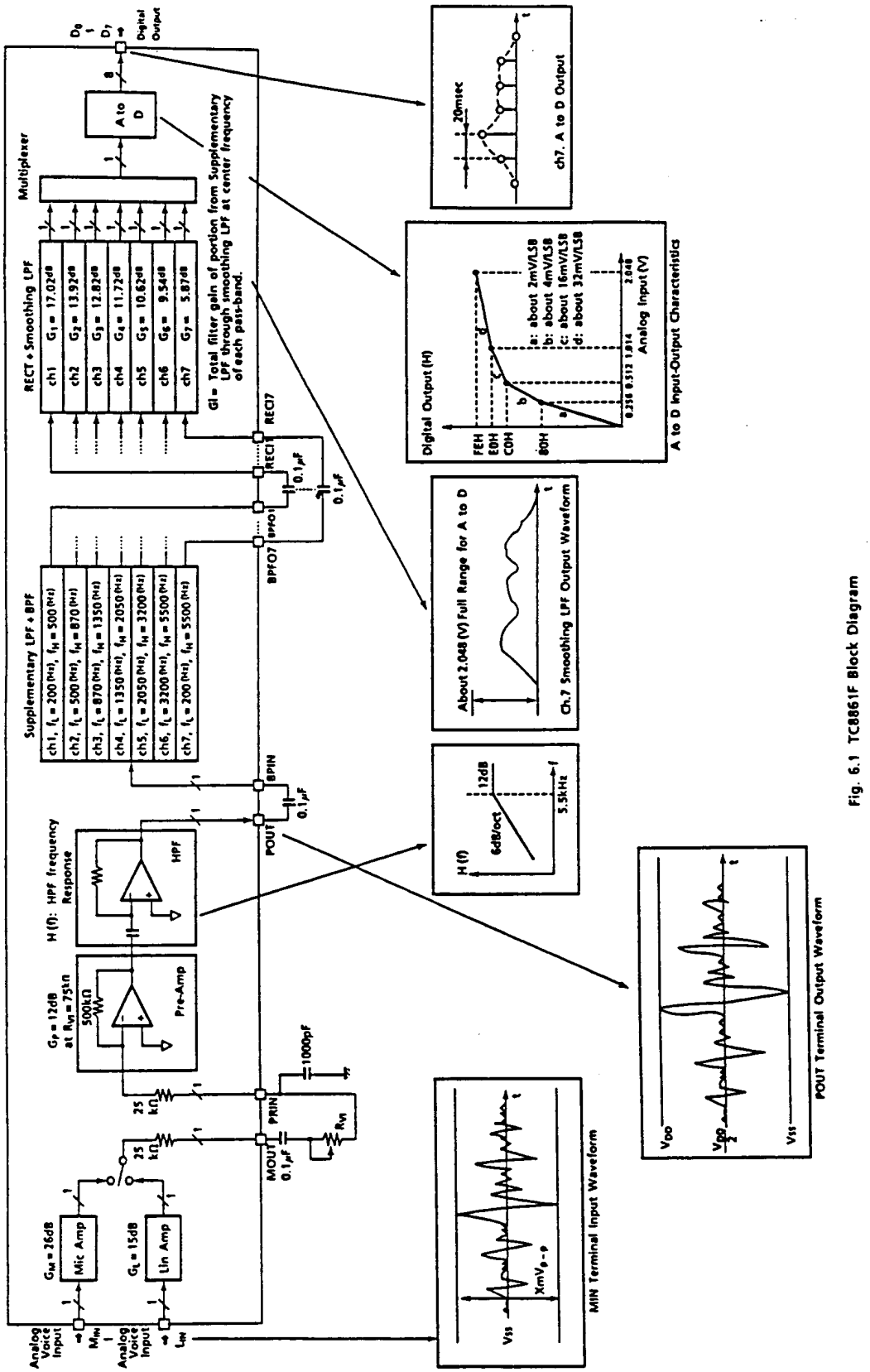


Fig. 6.1 TC8861F Block Diagram

6.1.2 TC8861F Pin Assignments

MFP 60 PIN

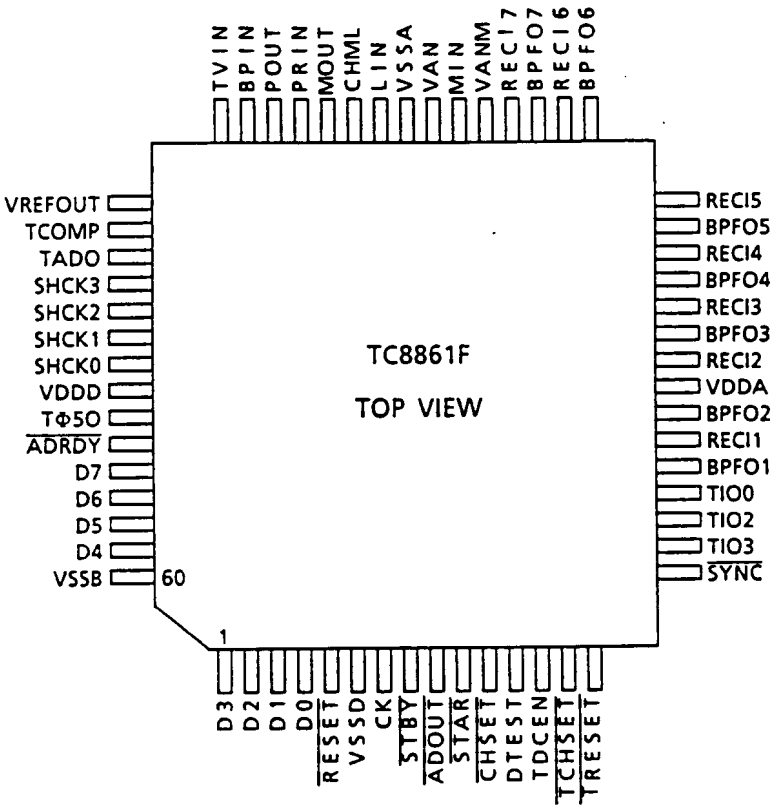


Fig. 6.2 TC8861F Pin Assignment Diagram

6.1.3 TC8861F Signal Description

(1) D0 ~ D7 (Data bus) [Input/Output]
8-bit bidirectional data bus. To be connected to the inner bus of the recognition system. These terminals are used by TC8864F-00 to write data into TC8861F and read data from TC8861F.

(2) $\overline{\text{CHSET}}$ (CHannel SET strobe) [Input]
When L to H rising signal is input to this terminal, D0-D7 data (To select multiplexer input filter channel) is written in the internal register of TC8861F. This terminal is connected to the $\overline{\text{CHSET}}$ terminal of TC8864F-00.

(3) $\overline{\text{ADOUT}}$ (A to D read OUT strobe) [Input]
When L level signal is input to this terminal, D0-D7 become the output mode and data (A to D output data) of the output register on TC8861F is output on D0-D7. This terminal is to be connected to the $\overline{\text{ADOUT}}$ terminal of TC8864F-00.

(4) $\overline{\text{STAR}}$ (a to d STARt signal) [Input]
A to D conversion start signal for A to D converter to be connected to the $\overline{\text{ADSTAR}}$ terminal of TC8864F-00.

(5) CK (ClocK) [Input]
Clock input terminal. By being connected to the ADCLK terminal of TC8864F-00, system clock (Typ. 2MHz) is supplied from TC8864F-00.

(6) $\overline{\text{RESET}}$ (system RESET) [Input]
Reset input terminal. To be connected to the $\overline{\text{RESET}}$ terminal of TC8864F-00. When L level signal is input to this terminal, TC8861F is reset.

(7) $\overline{\text{STBY}}$ (STand-BY) [Input]
Stand-by input terminal. To be connected to the $\overline{\text{STBY}}$ terminal of TC8864F-00. When L level signal is input to this terminal, TC8861F is put in the stand-by mode. At this time, however, the $\overline{\text{RESET}}$ terminal must have been set at L level in advance.

(8) $\overline{\text{ADRDY}}$ (A to D ReaDY) [Output]
This terminal is H level when the A to D converter is in the conversion operation and is L level after end of the conversion. This terminal is to be connected to the $\overline{\text{ADRDY}}$ terminal of TC8864F-00.

(9) MIN (Microphone INput) [Input]
Microphone signal input terminal. A microphone can be directly connected. When the CHML terminal is at L level, this terminal is valid. The microphone signal's ground level must be equal to Vss (ground) level of the LSI.

(10) LIN (Line INput) [Input]
Line input terminal. Voice signal is input to this terminal through the coupling capacitor. When the CHML terminal is at H level, this terminal is valid.

(11) CHML (CHange input terminal between Min and Lin) [Input]
Control signal to select whether a signal to be processed by TC8861F is input signal from the MIN terminal or that from the LIN terminal.

(12) MOUT (Min/lin amplifier OUTput) [Output]
Output terminal of the MIN or LIN input amplifier selected by the CHML terminal. To be connected to the PRIN terminal through a capacitor and a variable resistor.

(13) PRIN (PReamplifier INput) [Input]
Preamplifier input terminal. Output signal from the MOUT terminal is input to this terminal. A capacitor 1000pF (deviation within ±30%) is to be placed between this terminal and Vss (ground) level in order to stabilize analog characteristics. Without the capacitor, TC8861F does not operate properly.

(14) POUT (Preamplifier OUTput) [Output]
Preamplifier output terminal. To be connected to the BPIN terminal through a capacitor.

(15) BPIN (Band-Pass-filter INput) [Input]
Band-pass filter input terminal. Output signal from the POUT terminal is input to this terminal.

(16) VAN (Voltage level of ANalog ground) [Output]
Ground level of analog signal on analog circuit except the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(17) VANM (Voltage level of ANalog ground for Mic amplifier) [Output]
Ground level of analog signal on the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(18) VREFOUT (Voltage level of REFerence OUTput for A to D) [Output]
Reference voltage monitor terminal for A to D converter.

(19) BPF01~BPF07 (Band-Pass-Filter Output) [Output]
Output terminals for 7 band-pass filters. These terminals are respectively to be connected to the rectifier input terminals (RECI1-7) correspondent to each channel.

(20) RECI1~RECI7 (RECtifier Input) [Input]
Input terminals of 7 rectifiers.

(21) TIO0, TIO2, TIO3 (Test Input/Output) [Input/Output]
Test input/output terminals. Nothing should be connected to this terminal.

(22) TVIN, $\overline{\text{TRESET}}$ [Input]
Test input terminals. $\overline{\text{TRESET}}$ terminal contains pull down resistor.
Set them at L level. (Connect to the system ground Vss.)

(23) $\overline{\text{SYNC}}$, $\overline{\text{TCHSET}}$, TDCEN, DTEST/TDCSET, TAD0 [Input]
Test input terminal with pull-up or pull-down resistor. Nothing should be connected to this terminal.

(24) TΦ50, TCOMP [Output]
Test output terminal. Nothing should be connected.

(25) SHCK0~SHCK3 (Sample & Hold ClocK) [Output]
Test output terminal. Nothing should be connected.

(26) VDDD, VDDA
VDDD is the TC8861F digital circuit power supply terminal. VDDA is the TC8861F analog circuit power supply terminal. Both should be connected to the plus side of the power supply.

(27) VSSD, VSSB, VSSA
Ground terminals. VSSD is the ground for TC8861F digital circuit, VSSB is the ground for TC8861F data bus buffer and VSSA is the ground for TC8861F analog circuit.

6.1.4 Method to Wire External Miscellaneous Parts

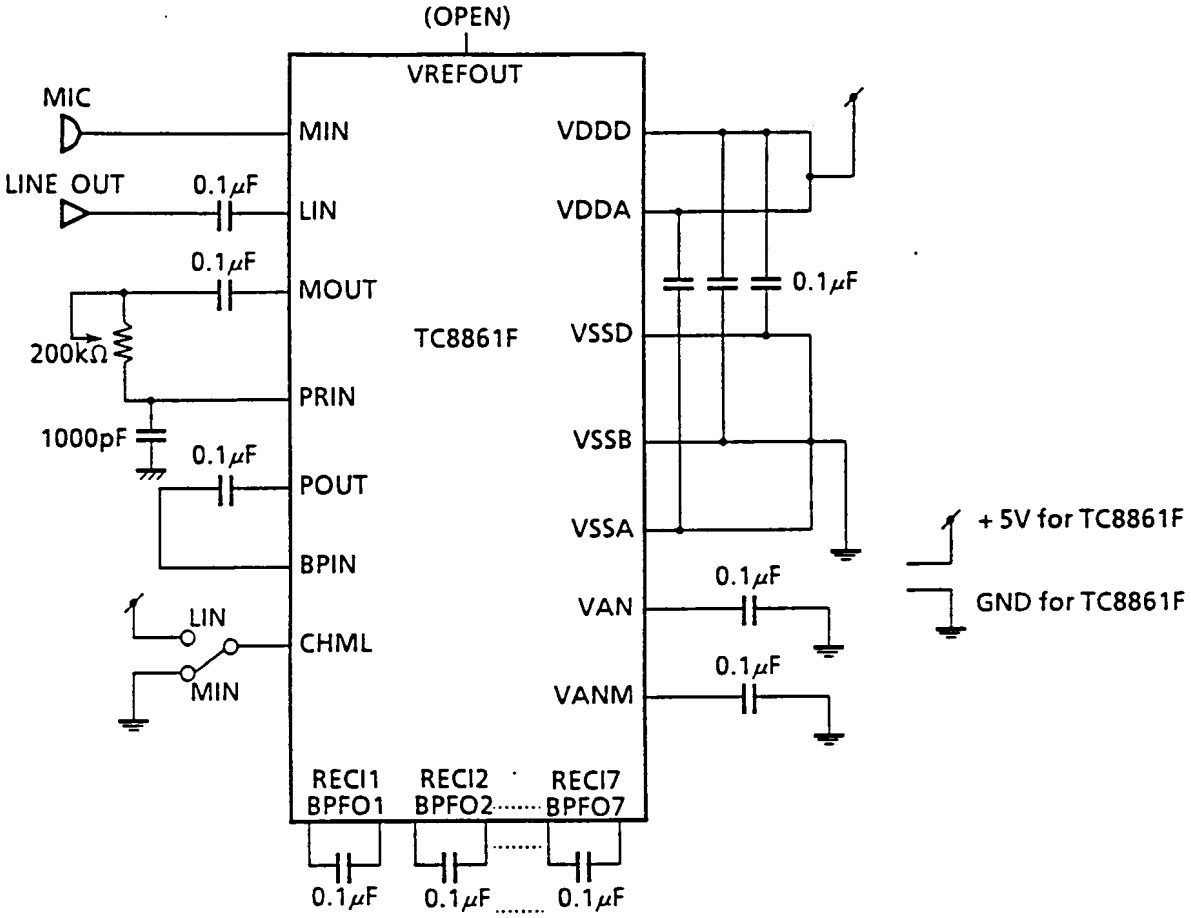


Fig. 6.3 Wiring Diagram

Because TC8861F is an analog device, special care must be taken of wiring external parts to maintain its analog characteristics. Following cautions must be carefully observed.

(1) Employ either MIN or LIN as an input terminal so that input voice may always pass through either microphone amplifier or line amplifier. The reason is that filter offset calibration offered by the device requires one of them to be passed through by input signal.
Otherwise the lack of calibration will lead to degradation in recognition accuracy.

(2) Position a bypass capacitor 0.1μF between power supply pins (VSS-VDD) as close to the pins as possible. Total 3 capacitors should be placed between VDDD-VSSD, VDDD-VSSB, and VDDA-VSSA.

(3) Position VAN and VANM level stabilization capacitors close to the pins.

(4) Use shield wires or pattern wires guard-ringed by GND against disturbing noise for MIN and LIN terminals. Also keep away PRIN, BPIN, RECIi (i=1~7), VAN, VANM, and VREFOUT terminals from digital high frequency signals.

(5) Place parts between MOUT and PRIN, POUT and BPIN, BPFOi and RECIi (i=1~7) as close to the pins as possible and connect them to the pins with short wires.
Warning! Place certainly a preamplifier stabilizing capacitor 1000pF within ±30% deviation between PRIN and VSSA as close to the pins as possible. Otherwise the device will not operate properly.

6.1.5 Method to Adjust Voice Level

Adjustment of voice level is important to maintain the high recognition performance. Two different stage adjustment are recommended.

(1) Variable Resistor (RVI) Setting: Adjustment by waveform amplitude on POUT.

Appropriate resistance setting on variable resistor (RVI) is usually once required after the device set is implemented in application product. RVI setting covers deviations in operational circumstance factors such as microphone sensitivity, distance between mouth and a microphone, and signal to Noise Ratio on MIN or LIN. Therefore it should not usually be done more than once after device set installation.

Concrete explanation about the setting is presented in the following: The criteria of appropriate setting is offered in such a way that maximum waveform amplitude of voice on POUT with analog GND 1/2 VDD (VDD: Supply power voltage) is equal or slightly more than full-range of GND-VDD. Although slight clipping of the signal on POUT due to a little louder voice do no harm, both too much clipping due to extremely loud voice and too little waveform due to too small voice reduces recognition performance.

An experiment with Japanese word "HAI", meaning "YES" in English, shows an equation about relationship between RVI value R (kΩ) and MIN or LIN maximum waveform amplitude X (mVp-p) or Y (mVp-p) producing full-range waveform on POUT as follows:

On MIN Terminal:

$$X\,(\mathrm{mVp\text{-}p}) = 70\,(\mathrm{mVp-p}) \times \frac{\frac{500\mathrm{k}\Omega}{75\mathrm{k}\Omega+50\mathrm{k}\Omega}}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}} = 70\,(\mathrm{mVp-p}) \times \frac{4}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}}$$

On LIN Terminal:

$$Y\,(\mathrm{mVp\text{-}p}) = 70\,(\mathrm{mVp-p}) \times \frac{4}{\frac{500\mathrm{k}\Omega}{R+50\mathrm{k}\Omega}} \times \frac{20\,(\mathrm{times})}{5.6\,(\mathrm{times})}$$

Table 6.1 indicates value relationships between R and X or between R and Y. Note that values indicated in the table are standard and will vary according to vocabulary.

Table 6.1 Relationship of values between R and X or between R and Y

R (kΩ)	X (mV_{p-p}) on MIN Terminal	Y (mV_{p-p}) on LIN Terminal
0	28	100
25	42	150
75	70	250
125	98	350
175	126	450
450	280	1000

Evaluation experience recommends around 15kΩ as R for condenser microphone.

(2) Input Voice Energy Flag in Recognition Result Header

Input voice energy flag mainly covers voice level deviation of individual utterance given by personal characteristics, like male or female. The flag is embedded in a 1byte recognition result header returned to a host system on recognition command execution. (See 5.4.2 Recognition Result Healer Format.) Upper 2bits of the header categorize the level of voice just recognized in two stages (too low, OK). Indication of this 2bit information to users helps better input voice level setting for next recognition.

6.1.6 Threshold for Word Boundary Detection

Word boundary detection threshold is used to determine valid voice signal period. Input signals with level exceeding the threshold, lasting over a certain period of time, is picked up as valid voice. The detection is followed by pattern matching activity.

The device set adaptively determines the threshold by monitoring background noise level when no voice exists, and changes the threshold level from '8H' (about 16mV) through '47H' (142mV) according to background noise. It sets lower threshold for lower background noise and higher threshold for higher background noise.

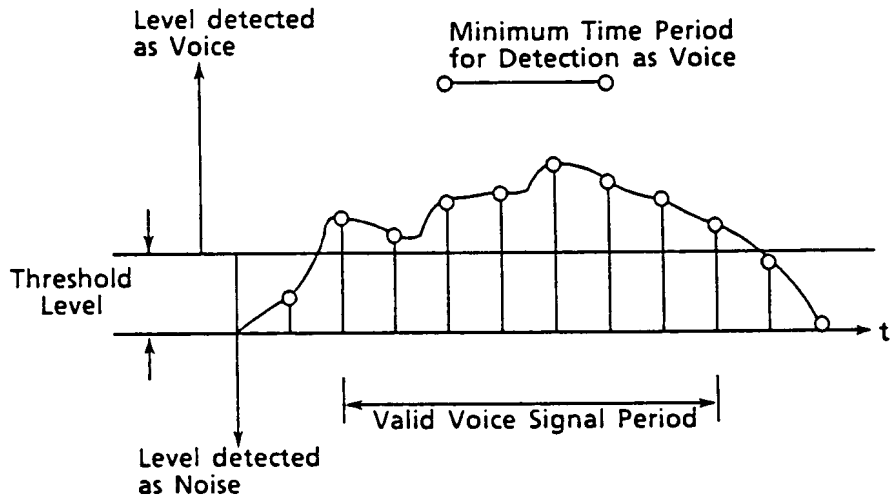


Fig. 6.4 Word Boundary Detection Scheme

6.1.7 Remarks on Power Supply

Since TC8861F is an LSI with the analog circuit built in, its analog characteristics may be adversely affected by the noise of a power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate a power supply to TC8861F from that to other LSI's (TC8864F-00, Host System and other LSI's). (2 power supplies)
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the other power supply GND to the power supply GND of TC8861F.
- The power supply for TC8861F should have as less ripple as possible and a series regulator power supply is recommended for the best condition. If a switching regulator power supply is used, it should be stabilized by a three-terminal regulator. An example of a circuit, when a power supply is composed of a combination of a switching regulator power supply and a three-terminal regulator, is shown below.

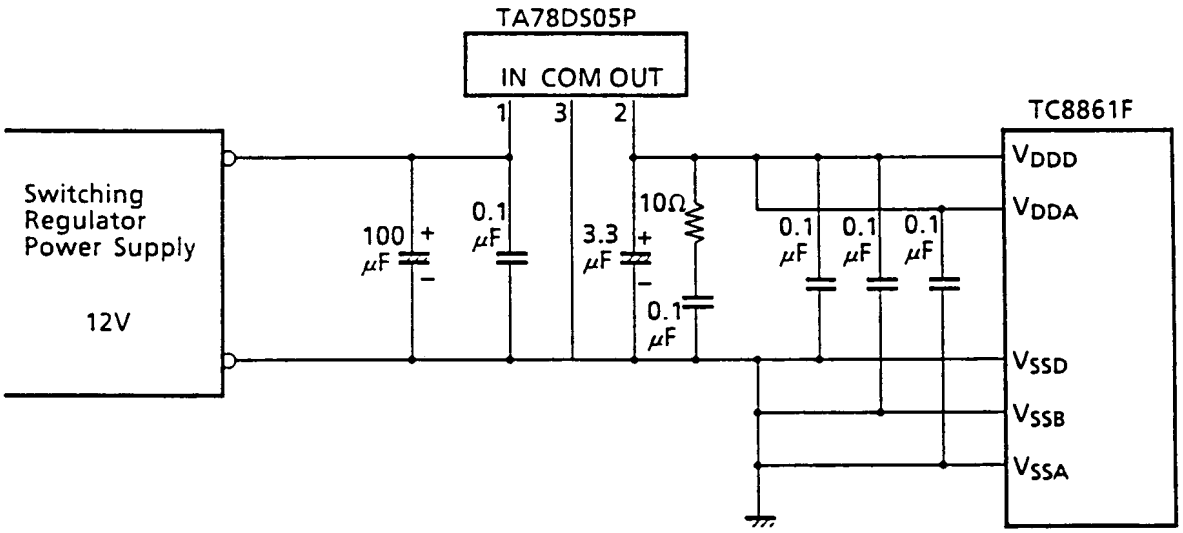


Fig. 6.5 Recommended Power Supply Circuit for TC8861F

6.1.8 TC8861F List of Pins

Table 6.2 List of Pins on TC8861F

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
D0	4	I/O, 3-State	System controller data bus	*Hz
D1	3	I/O, 3-State	System controller data bus	*Hz
D2	2	I/O, 3-State	System controller data bus	*Hz
D3	1	I/O, 3-State	System controller data bus	*Hz
D4	59	I/O, 3-State	System controller data bus	*Hz
D5	58	I/O, 3-State	System controller data bus	*Hz
D6	57	I/O, 3-State	System controller data bus	*Hz
D7	56	I/O, 3-State	System controller data bus	*Hz
$\overline{\text{CHSET}}$	11	Input	Control signal from TC8864F-00	-
$\overline{\text{ADOUT}}$	9	Input	Control signal from TC8864F-00	-
$\overline{\text{STAR}}$	10	Input	Control signal from TC8864F-00	-
CK	7	Input	Clock input	-
$\overline{\text{RESET}}$	5	Input	Reset input	-
$\overline{\text{STBY}}$	8	Input	Stand-by input	-
$\overline{\text{ADRDY}}$	55	Output	TC8861F A to D operational status	H
MIN	36	Input	Microphone input	-
LIN	39	Input	Line input	-
CHML	40	Input	Analog input change-over signal	-
MOUT	41	Output	Output of MIC Amplifier or LIN Amplifier	*Hz
PRIN	42	Input	Preamplifier input	-
POUT	43	Output	Preamplifier output	*Hz
BPIN	44	Input	Band-pass filter input	-
VAN	37	Output	Ground level of analog signal on analog circuit (except MIN amplifier, LIN amplifier and preamplifier)	L
VANM	35	Output	Ground level of analog signal on MIN amplifier, LIN amplifier and preamplifier	L
VREFOUT	46	Output	Reference voltage for A to D circuit	L
BPF01	20	Output	Band-pass filter 1 output	*Hz
RECI1	21	Input	Rectifier 1 input	-
BPF02	22	Output	Band-pass filter 2 output	*Hz
RECI2	24	Input	Rectifier 2 input	-
BPF03	25	Output	Band-pass filter 3 output	*Hz
RECI3	26	Input	Rectifier 3 input	-
BPF04	27	Output	Band-pass filter 4 output	*Hz
RECI4	28	Input	Rectifier 4 input	-
BPF05	29	Output	Band-pass filter 5 output	*Hz
RECI5	30	Input	Rectifier 5 input	-
BPF06	31	Output	Band-pass filter 6 output	*Hz
RECI6	32	Input	Rectifier 6 input	-
BPF07	33	Output	Band-pass filter 7 input	*Hz

* HZ=High impedance

(Continued)

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
RECI7	34	Input	Rectifier 7 input	-
TIO0	19	Input/Output	Test Terminal	*Hz
TIO2	18	Input/Output	Test Terminal	*Hz
TIO3	17	Input/Output	Test Terminal	*Hz
TVIN	45	Input	Test Terminal	-
$\overline{\text{SYNC}}$	16	Input	Test terminal: with a built-in pull-up resistor	-
$\overline{\text{TRESET}}$	15	Input	Test terminal: with a built-in pull-down resistor	-
$\overline{\text{TCHSET}}$	14	Input	Test terminal: with a built-in pull-up resistor	-
TDCEN	13	Input	Test terminal: with a built-in pull-down resistor	-
DTEST/ TDCSET	12	Input	Test terminal: with a built-in pull-down resistor	-
TADO	48	Input	Test terminal: with a built-in pull-down resistor	-
TΦ50	54	Output	Test terminal	L
TCOMP	47	Output	Test terminal	L
SHCK0	52	Output	Test terminal	L
SHCK1	51	Output	Test terminal	L
SHCK2	50	Output	Test terminal	L
SHCK3	49	Output	Test terminal	L
VDDD	53	–	Digital circuit power supply terminal	-
VDDA	23	–	Analog circuit power supply terminal	-
VSSD	6	–	Digital circuit ground terminal	-
VSSB	60	–	Data bus buffer ground terminal	-
VSSA	38	–	Analog circuit ground terminal	-

*HZ = High impedance

6.2 TC8864F-00

6.2.1 TC8864F-00 Pin Assignments

QFP 100 PIN

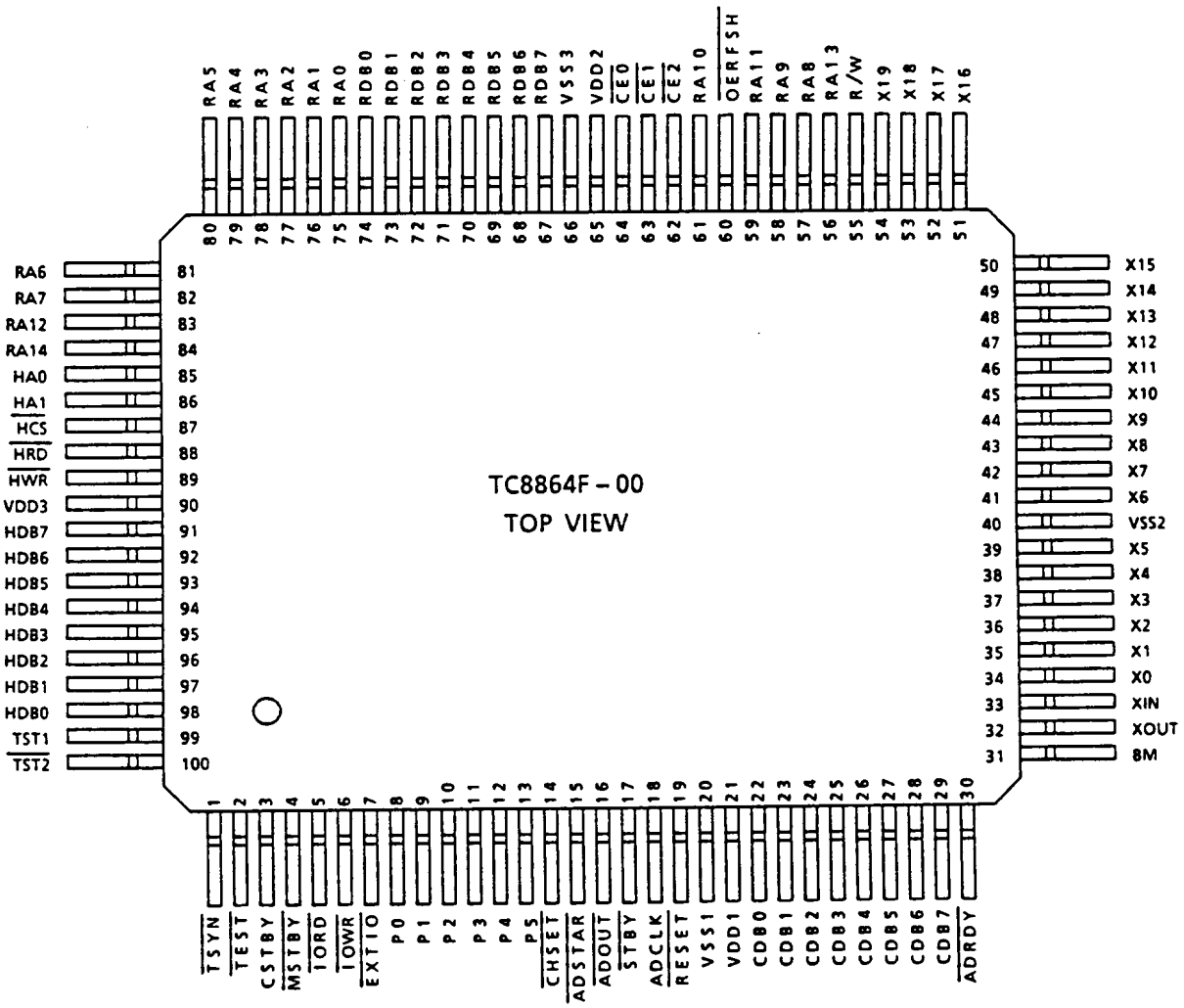


Fig. 6.6 TC8864F-00 Pin Assignment Diagram

6.2.2 TC8864F-00 Signal Descriptions

TC8861F I/F Signals

(1) CDB0~CDB7 (Cpu Data Bus) [Input/Output]
8-bit bidirectional data bus connected to the internal bus in the recognition system for address and data input/output. These terminals are to be connected to DB0-DB7 of TC8861F.

(2) ADCLK (A-D CLocK) [Output]
TC8861F clock output-terminal. 2MHz, duty 50% signal is output. This terminal is to be connected to the CK terminal of TC8861F.

(3) $\overline{\text{CHSET}}$ (CHannel SET strobe) [Output]
TC8861F channel set signal output-terminal. This terminal is to be connected to the $\overline{\text{CHSET}}$ terminal of TC8861F.

(4) $\overline{\text{ADOUT}}$ (A-D read OUT strobe) [Output]
TC8861F A to D output data read-out signal output-terminal. This terminal is to be connected to the $\overline{\text{ADOUT}}$ terminal of TC8861F.

(5) $\overline{\text{ADSTAR}}$ (A-D STARt signal) [Output]
TC8861F A to D conversion start signal output-terminal. To be connected to the $\overline{\text{STAR}}$ terminal of TC8861F.

(6) $\overline{\text{ADRDY}}$ (A-D ReaDY) [Input]
TC8861F A to D conversion end signal input-terminal. To be connected to the $\overline{\text{ADRDY}}$ terminal of TC8861F.

Host System I/F Signals

(7) HDB0~HDB7 (Host Data Bus) [Input/Output]
8-bit bidirectional data bus. These terminals are to be connected to the data bus of a host system and used for transferring all kinds of data such as commands, status and recognition result.

(8) HA0~HA1 (Host Port Address 0, 1) [Input]
These terminals are to be connected to the address output of a host system and used to specify the kind of data transferred through HDB0~7.

(9) $\overline{\text{HCS}}$ (Host Chip Select) [Input]
A low on this pin enables the TC8864F-00 host system I/F to be active and the $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals described below become valid.

(10) $\overline{\text{HRD}}$ (Host ReaD strobe) [Input]
When L level signal is input to this terminal at $\overline{\text{HCS}}$=L, the HDB0-HDB7 terminals are set to the output mode, and recognition result, status, etc. are output according to the signals of the HA0 and HA1 terminals. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals must not be put at L level at the same time.

(11) $\overline{\text{HWR}}$ (Host WRite strobe) [Input]

At the rising edge of this terminal at $\overline{\text{HCS}}$=L as described above, HDB0-HDB7 data are latched in TC8864F-00. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals should not be put at L level simultaneously.

Signals to Reset & Stand-by Circuits, Clock Oscillator, Test Circuits

(12) CSTBY (Capacitor for STand-BY) [Input]

This terminal is connected with a capacitor to the ground to produce the system start sequence control timing when the power supply becomes ON.

(13) $\overline{\text{MSTBY}}$ (Manual STand-BY) [Input]

Manual stand-by terminal. This terminal should be set at High level in normal operation.

(14) $\overline{\text{RESET}}$ [Output]

System reset signal output terminal. This terminal is to be connected to $\overline{\text{RESET}}$ terminal of TC8861F.

(15) $\overline{\text{STBY}}$ (STand-BY) [Output]

System stand-by signal output terminal. To be connected to $\overline{\text{STBY}}$ terminal of TC8861F.

(16) XIN, XOUT (Xtal-IN, OUT) [Input]

Ceramic resonator connecting terminals. An 8MHz ceramic resonator and capacitor are connected.

(17) $\overline{\text{TEST}}$, TST1, $\overline{\text{TST2}}$ [Input]

Test input terminal. These terminals should be set at High level in normal operation.

(18) $\overline{\text{TSYN}}$ [Input]

Test input terminal. This terminal should be set at High level in normal operation.

External memory I/F Signals

(19) RDB0~RDB7 (Reference memory Data Bus) [Input/Output]

8-bit bidirectional external memory data bus. These terminals are to be connected to the external memory data bus.

(20) RA0~RA14 (Reference memory Address) [Output]

The 15-bit external pattern memory address bus. These terminals are to be connected to the external memory address bus.

(21) $\overline{\text{CE0}}$ (Chip Enable 0) [Output]

This terminal is a chip select output available for CPU to accesses memory data addressed 4000H through 5FFFH. This terminal should be connected to a chip select terminal of 64K static RAM because program codes in TC8864F-00 are located within this address space.

(22) $\overline{\text{CE1}}$ (Chip Enable 1) [Output]

This terminal is a chip select output available for CPU to access memory data addressed 6000H through 7FFFH. $\overline{\text{CE1}}$ should not be connected to any signals.

(23) $\overline{CE2}$ (Chip Enable 2) [Output]

This terminal is a chip select output available for CPU to access memory data addressed 8000H through FFFFH. $\overline{CE2}$ should not be connected to any signals.

(24) R/W (Read/Write) [Output]

This terminal is to be connected to R/W terminal of 64Kbit static RAM.

(25) $\overline{OERFSH}$ (Output Enable/ReFreSH enable) [Output]

$\overline{OERFSH}$ should not be connected to any signals.

Internal general purpose interface signals

Following terminals are not supported by TC8864F-00 system.

(26) $\overline{IOWR}$ (I/O WRite strobe) [Output]

This terminal is enabled when CPU writes to a specified I/O port.

(27) $\overline{IORD}$ (I/O ReaD strobe) [Output]

This terminal is enabled when CPU reads from a specified I/O port.

(28) $\overline{EXTIO}$ (EXTernal I/O select) [Output]

This terminal is a chip select output using with $\overline{IOWR}$, $\overline{IORD}$ terminals.

(29) P0~5 (Port 0~5) [Input/Output]

P0 through P5 terminals are 6bit general purpose I/O ports, but not available in TC8864F-00 system. These terminals should not be connected any signals.

(30) 8M (8MHz clock output) [Output]

This terminal outputs 8MHz clock.

(31) X0~X17 [Output]

These terminals are test output terminals, and should not be connected any signals.

(32) X18,X19 [Input]

These terminals are test input terminals and should be connected to VSS terminal.

Power Supply Signals

(33) VDD1, VDD2, VDD3

The power supply terminals. All terminals are to be connected to the plus side of the power supply.

(34) VSS1, VSS2, VSS3

The ground terminals. All terminals are to be connected to the ground side of the power supply.

6.2.3 Method to Wire External Static RAM

TC8864F-00 is used with a 64K bit static RAM as external memory. Method of wiring external memory is displayed at fig. 6.7.

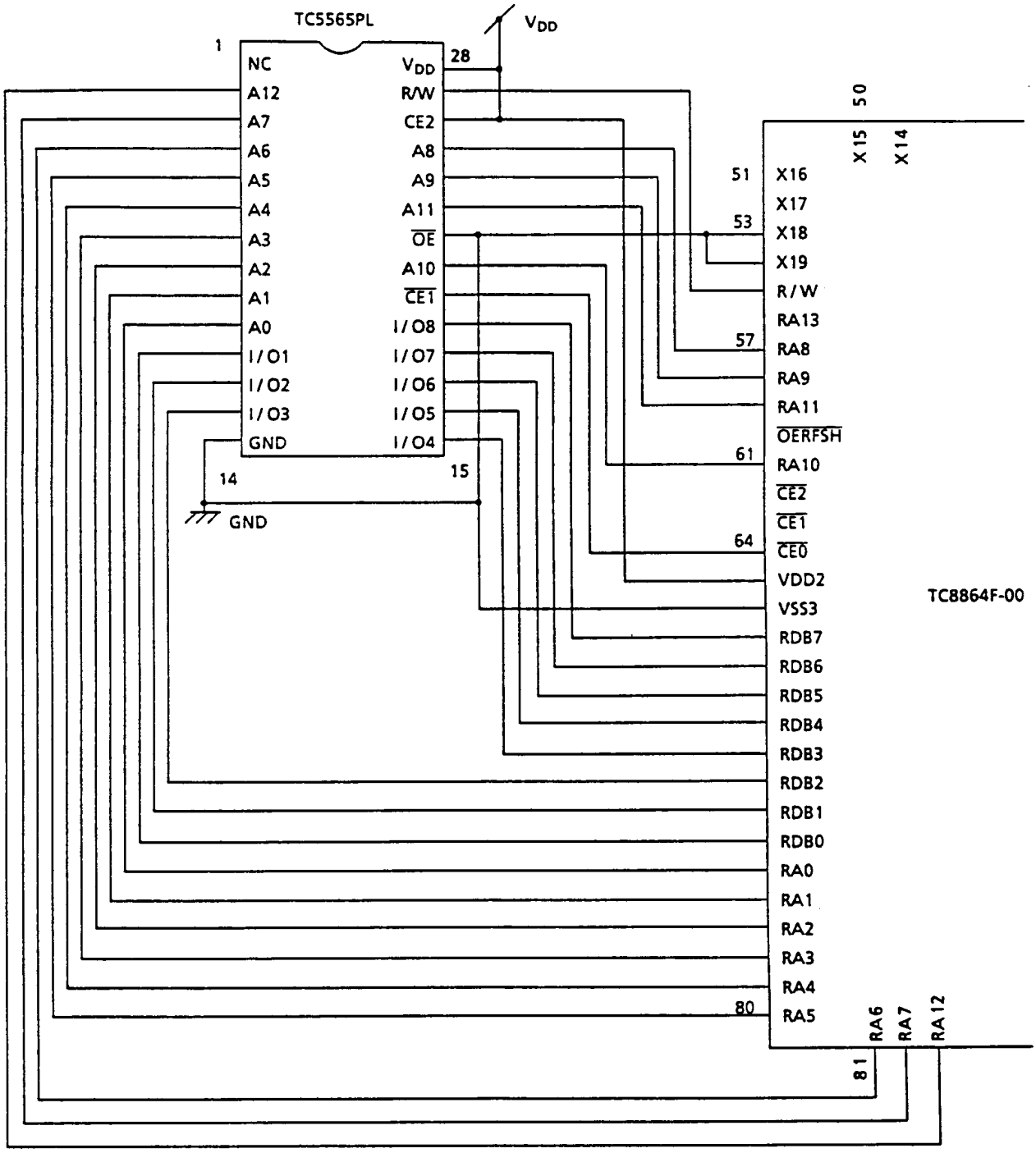


Fig. 6.7 External memory wiring diagram

6.2.4 Oscillation Circuit

TC8864F-00 obtains built-in oscillation circuit. Connect ceramic resonator and capacitors to XIN and XOUT terminals. When clock is supplied from external circuit, connect this clock signal to XIN terminal and don't connect any signal to XOUT terminal.

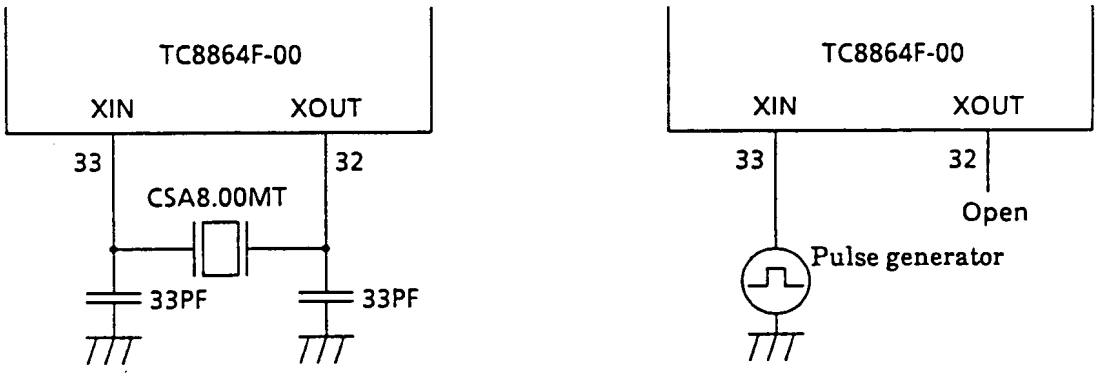


fig. 6.8 Oscillation Circuit

6.2.5 Method to Wire External Parts

Connect 0.01μF capacitor to CSTBY terminal for making start-up timing.

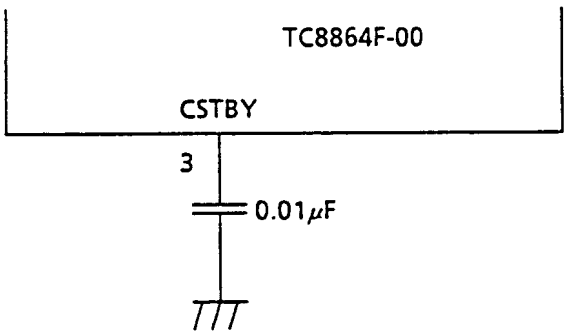


fig. 6.9 External Parts

6.2.6 TC8864F-00 List of Pins

Table 6.3 List of Pins on TC8864F-00

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
CDB0	22	I/O, 3-State	Internal data bus	*Hz
1	23	I/O, 3-State	Internal data bus	*Hz
2	24	I/O, 3-State	Internal data bus	*Hz
3	25	I/O, 3-State	Internal data bus	*Hz
4	26	I/O, 3-State	Internal data bus	*Hz
5	27	I/O, 3-State	Internal data bus	*Hz
6	28	I/O, 3-State	Internal data bus	*Hz
7	29	I/O, 3-State	Internal data bus	*Hz
ADCLK	18	Output	Clock output for TC8861F	H
$\overline{\text{CHSET}}$	14	Output	TC8861F control signal	H
$\overline{\text{ADSTAR}}$	15	Output	TC8861F control signal	H
$\overline{\text{ADOUT}}$	16	Output	TC8861F control signal	H
$\overline{\text{ADRDY}}$	30	Input	TC8861F status signal	–
$\overline{\text{RESET}}$	19	Output	System reset output	L
$\overline{\text{STBY}}$	17	Output	System stand-by output	L
HDB0	98	I/O, 3-State	Host system data bus	*Hz
1	97	I/O, 3-State	Host system data bus	*Hz
2	96	I/O, 3-State	Host system data bus	*Hz
3	95	I/O, 3-State	Host system data bus	*Hz
4	94	I/O, 3-State	Host system data bus	*Hz
5	93	I/O, 3-State	Host system data bus	*Hz
6	92	I/O, 3-State	Host system data bus	*Hz
7	91	I/O, 3-State	Host system data bus	*Hz
HA0	85	Input	Address signal input from Host system	–
1	86	Input	Address signal input from Host system	–
$\overline{\text{HCS}}$	87	Input	Control signal input from Host system	–
$\overline{\text{HRD}}$	88	Input	Control signal input from Host system	–
$\overline{\text{HWR}}$	89	Input	Control signal input from Host system	–
RDB0	74	I/O, 3-State	External memory data bus	H or L
1	73	I/O, 3-State	External memory data bus	H or L
2	72	I/O, 3-State	External memory data bus	H or L
3	71	I/O, 3-State	External memory data bus	H or L
4	70	I/O, 3-State	External memory data bus	H or L
5	69	I/O, 3-State	External memory data bus	H or L
6	68	I/O, 3-State	External memory data bus	H or L
7	67	I/O, 3-State	External memory data bus	H or L
$\overline{\text{CE0}}$	64	Output	External memory chip selection signal	H
$\overline{\text{CE1}}$	63	Output	External memory chip selection signal	H
$\overline{\text{CE2}}$	62	Output	External memory chip selection signal	H
$\overline{\text{OERFSH}}$	60	Output	Control signal for external memory	L
R/W	55	Output	Control signal for external memory	H

* Hz = High Impedance

(Continued)

Pin Name	Pin No.	Input/Output	Function	Status st stand-by
RA0	75	Output	External memory address bus	H
1	76	Output	External memory address bus	H
2	77	Output	External memory address bus	H
3	78	Output	External memory address bus	H
4	79	Output	External memory address bus	H
5	80	Output	External memory address bus	H
6	81	Output	External memory address bus	H
7	82	Output	External memory address bus	H
8	57	Output	External memory address bus	H
9	58	Output	External memory address bus	H
10	61	Output	External memory address bus	H
11	59	Output	External memory address bus	H
12	83	Output	External memory address bus	H
13	56	Output	External memory address bus	H
14	84	Output	External memory address bus	H
CSTBY	3	Input	For producing rising start-up timing	–
$\overline{\text{MSTBY}}$	4	Input	Manual stand-by input	–
XIN	33	Input	Ceramic resonator connecting terminal	–
XOUT	32	Input	Ceramic resonator connecting terminal	–
$\overline{\text{IORD}}$	5	Output	External I/O control signal	H
$\overline{\text{IOWR}}$	6	Output	External I/O control signal	H
$\overline{\text{EXTIO}}$	7	Output	External I/O control signal	H
P0	8	I/O, 3-State	External I/O port	*Hz
P1	9	I/O, 3-State	External I/O port	*Hz
P2	10	I/O, 3-State	External I/O port	*Hz
P3	11	I/O, 3-State	External I/O port	*Hz
P4	12	I/O, 3-State	External I/O port	*Hz
P5	13	I/O, 3-State	External I/O port	*Hz
8M	31	Output	Clock output	H
X0	34	Output	Test terminal	H
1	35	Output	Test terminal	H
2	36	Output	Test terminal	H
3	37	Output	Test terminal	H
4	38	Output	Test terminal	H
5	39	Output	Test terminal	H
6	41	Output	Test terminal	H
7	42	Output	Test terminal	H
8	43	Output	Test terminal	H
9	44	Output	Test terminal	H
10	45	Output	Test terminal	H

* Hz = High Impedance

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
X11	46	Output	Test terminal	H
X12	47	Output	Test terminal	H
X13	48	Output	Test terminal	H
X14	49	Output	Test terminal	H
X15	50	Output	Test terminal	H
X16	51	Output	Test terminal	H
X17	52	Output	Test terminal	H
X18	53	Input	Test terminal	–
X19	54	Input	Test terminal	–
$\overline{\text{TEST}}$	2	Input	Test terminal	–
TST1	99	Input	Test terminal	–
$\overline{\text{TST2}}$	100	Input	Test terminal	–
$\overline{\text{TSYN}}$	1	Input	Test terminal	–
VDD1	21	–	Power supply terminal	–
VDD2	65	–	Power supply terminal	–
VDD3	90	–	Power supply terminal	–
VSS1	20	–	Ground terminal	–
VSS2	40	–	Ground terminal	–
VSS3	66	–	Ground terminal	–

7. Electrical Characteristics

7.1 TC8861F

7.1.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	−0.3~+6.0	V
Input Voltage	VIN	−0.3~VDD+0.3	V
Output Voltage	VOUT	−0.3~VDD+0.3	V
Storage Temperature	Tstg	−55~+125	°C

7.1.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	4.5~5.5	V
Input Voltage	VIN	0~VDD	V
Output Voltage	VOUT	0~VDD	V
Operating Frequency	fCLK	1.9~2.1	MHz
Operating Temperature	Topr	-10~+70	°C

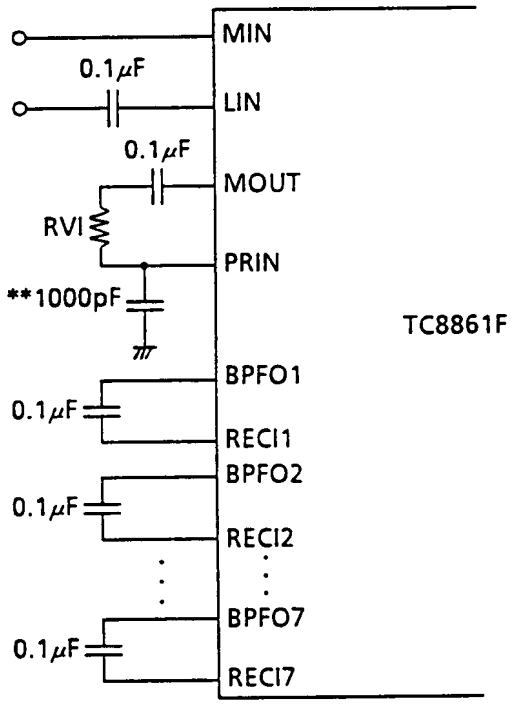
7.1.3 DC Characteristics (VDD = +5.0V ± 10%, Topr = -10 ~ +70°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Input Low Voltage		VIL		−	−	0.8	V
Input High Voltage	D0~D7	VIH		2.2	−	−	V
	Other than above			VDD-0.8	−	−	
Input Low Current		IIL	VIN = 0V	−	−	−5	μA
Input High Current		IIH	VIN = VDD	−	−	5	μA
Output Low Current		IOL	VOUT = 0.4V	1.76	−	−	mA
Output High Current		IOH	VOUT = VDD − 0.4V	−0.44	−	−	mA
Supply Current (1)		IDD-OPR	When A to D Converter not operating	−	13	25	mA
Supply Current (2)		IDD-STBY	At stand-by state	−	−	3	μA

7.1.4 Analog Input Terminal (VDD = +5.0V ± 10%, T_{opr} = -10~ +70°C)

ITEM		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Allowable input	MIN	Vin	RVI* = 0KΩ f = 1KHz	-	-	28	mVp-p
	LIN		RVI* = 75KΩ f = 1KHz	-	-	250	
Input Resistance	MIN	Rin	f = 1KHz	-	100	-	KΩ
	LIN			-	100	-	

* Condition: The following parts wiring scheme is employed.



** 1000pF capacitor is essential for normal operation

Fig. 7.1 Wiring Diagram

7.2 TC8864F-00

7.2.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	−0.3~+6.0	V
Input Voltage	VIN	−0.3~VDD+0.3	V
Output Voltage	VOUT	−0.3~VDD+0.3	V
Storage Temperature	Tstg	−55~+125	°C

7.2.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	4.5~5.5	V
Input Voltage	VIN	0~VDD	V
Output Voltage	VOUT	0~VDD	V
Operating Frequency	fCK	7.6~8.4	MHz
Operating Temperature	Topr	-10~+70	°C

7.2.3 DC Characteristics (VDD = +5.0V ± 10%, Topr = -10~+70°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
Input Low Voltage	VIL		−	−	0.8	V
Input High Voltage	VIH		2.2	−	−	V
Input Low Current	IIL	VIN = 0V	−	−	−5	μA
Input High Current	IIH	VIN = VDD	−	−	5	μA
Output Low Current	IOL	VOUT = 0.4V	1.76	−	−	mA
Output High Current	IOH	VOUT = VDD − 0.4V	−0.44	−	−	mA
Supply Current (1)	IDD-OPR	In no access state	−	20	30	mA
Supply Current (2)	IDD-STBY	In stand-by state	−	−	3	μA

7.2.4 AC Characteristics(VDD = +5.0V ± 10%, fCK = 8MHz, Topr = -10~+70°C, CL = 20PF (Control Signal), 100PF (Data Bus))

(1) Host System I/F Reading Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HRD}$ Pulse Width	tHRR		300	-	8,000	ns
Address Setup Time	tHAR		0	-	-	ns
Output Delay Time	tHRD		-	-	200	ns
Address Hold Time	tHRA		0	-	-	ns
Output Disable Time	tHDF		10	-	100	ns

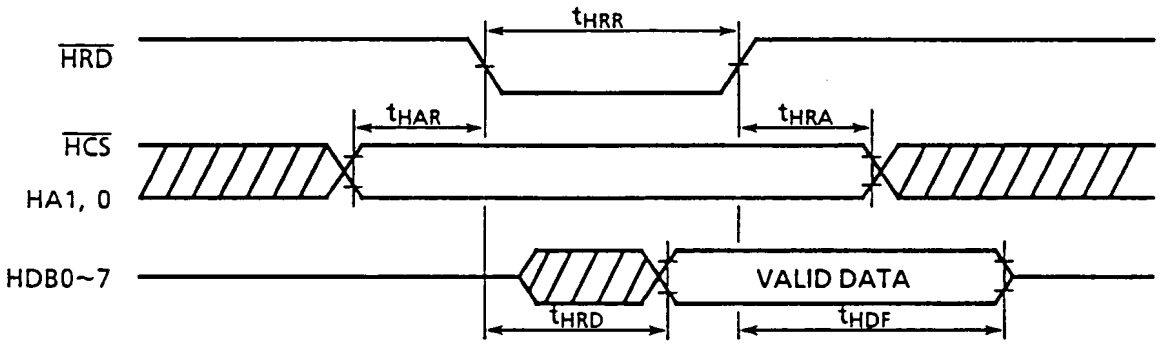


Fig. 7.2 Reading Cycle Timing Diagram on TC8864F-00 Host Interface

(2) Host System I/F Writing Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HWR}$ Pulse Width	tHWW		300	-	8,000	ns
Address Setup Time	tHAW		0	-	-	ns
Data Setup Time	tHDW		120	-	-	ns
Address Hold Time	tHWA		0	-	-	ns
Data Hold Time	tHWD		30	-	-	ns

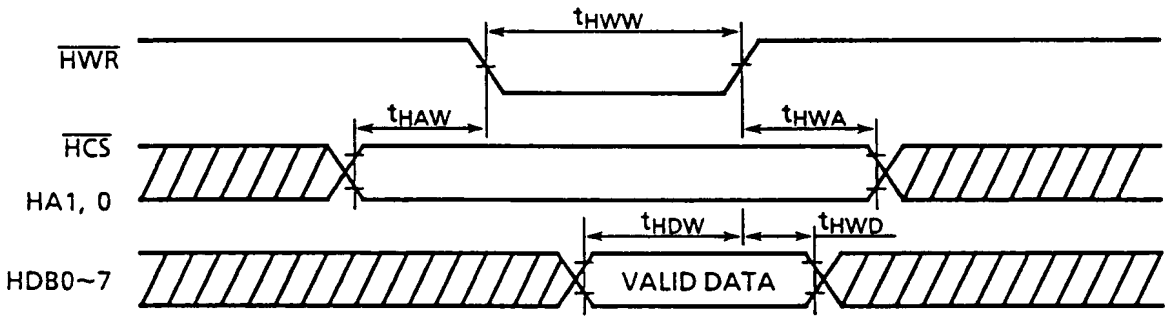


Fig. 7.3 Writing Cycle Timing Diagram on TC8864F-00 Host Interface

(3) External Memory I/F Reading Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{CE}$ Pulse Width	tRCC1	fCK = 8MHz	500	–	600	ns
Address Setup Time	tRAE	fCK = 8MHz	35	–	–	ns
Address Hold Time	tROA	fCK = 8MHz	50	–	–	ns
Data Setup Time	tRRS	fCK = 8MHz	300	–	–	ns
Data Hold Time	tRRH	fCK = 8MHz	0	–	–	ns

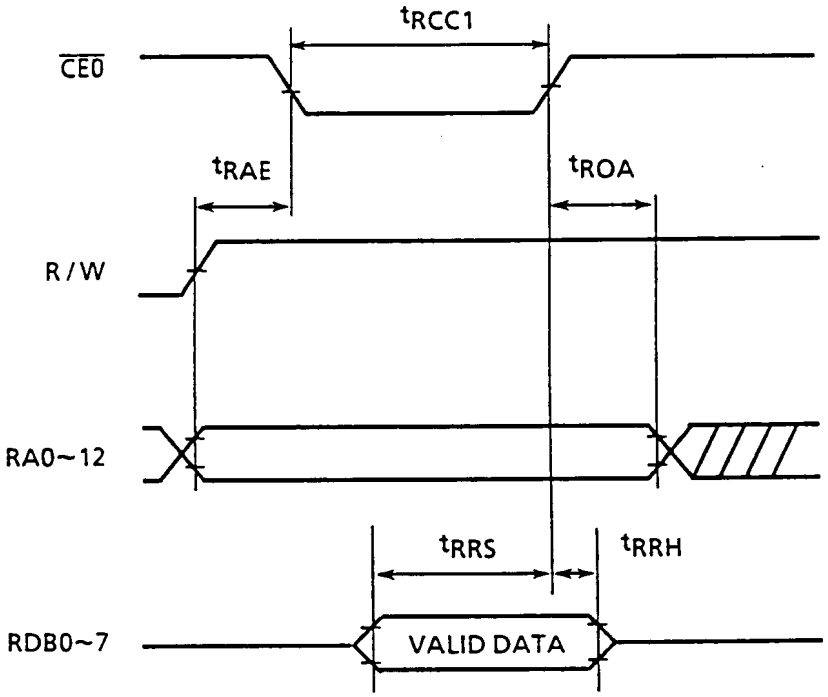


Fig. 7.4 Reading Cycle Timing Diagram on TC8864F-00 External Memory Interface

(4) External Memory I/F Writing Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{CE}$ Pulse Width	tRCC2	fCK = 8MHz	500	–	600	ns
R/W→$\overline{CE}$ Delay Time	tREW	fCK = 8MHz	0	–	–	ns
R/W Pulse Width	tRWW	fCK = 8MHz	200	–	–	ns
R/W→$\overline{CE}$ Delay Time	tRWE	fCK = 8MHz	0	–	–	ns
Address Setup Time	tRAW	fCK = 8MHz	180	–	–	ns
Address Hold Time	tRWA	fCK = 8MHz	100	–	–	ns
Data Setup Time	tRDW	fCK = 8MHz	0	–	–	ns
Data Hold Time	tRWD	fCK = 8MHz	1000	–	–	ns

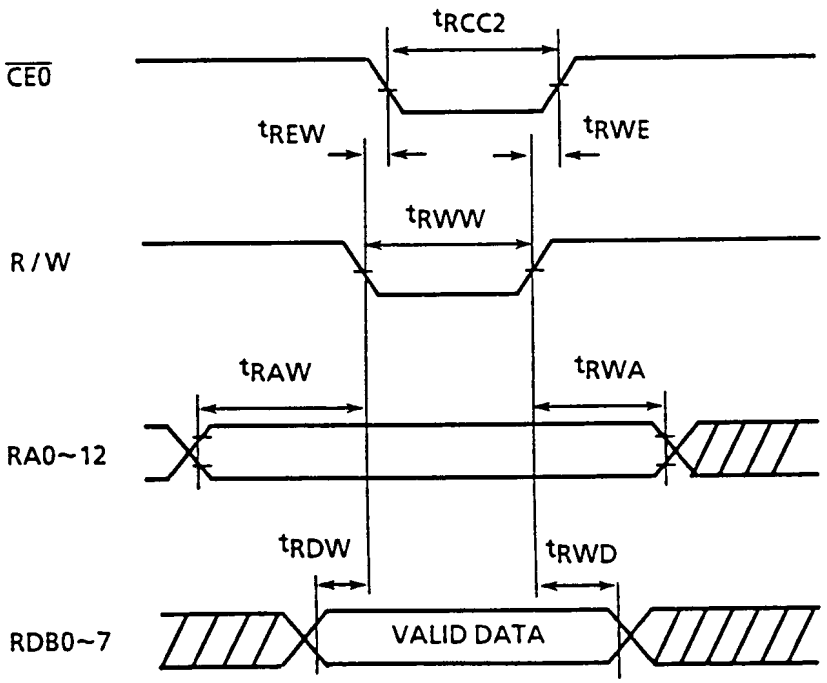


Fig. 7.5 Writing Cycle Timing Diagram on TC8864F-00 External Memory Interface

8. Package Dimensions

8.1 TC8861F

60-pin Mini-Flat Package (Package Code QFP60-P-1414A in Toshiba IC Package Manual)

Unit : mm

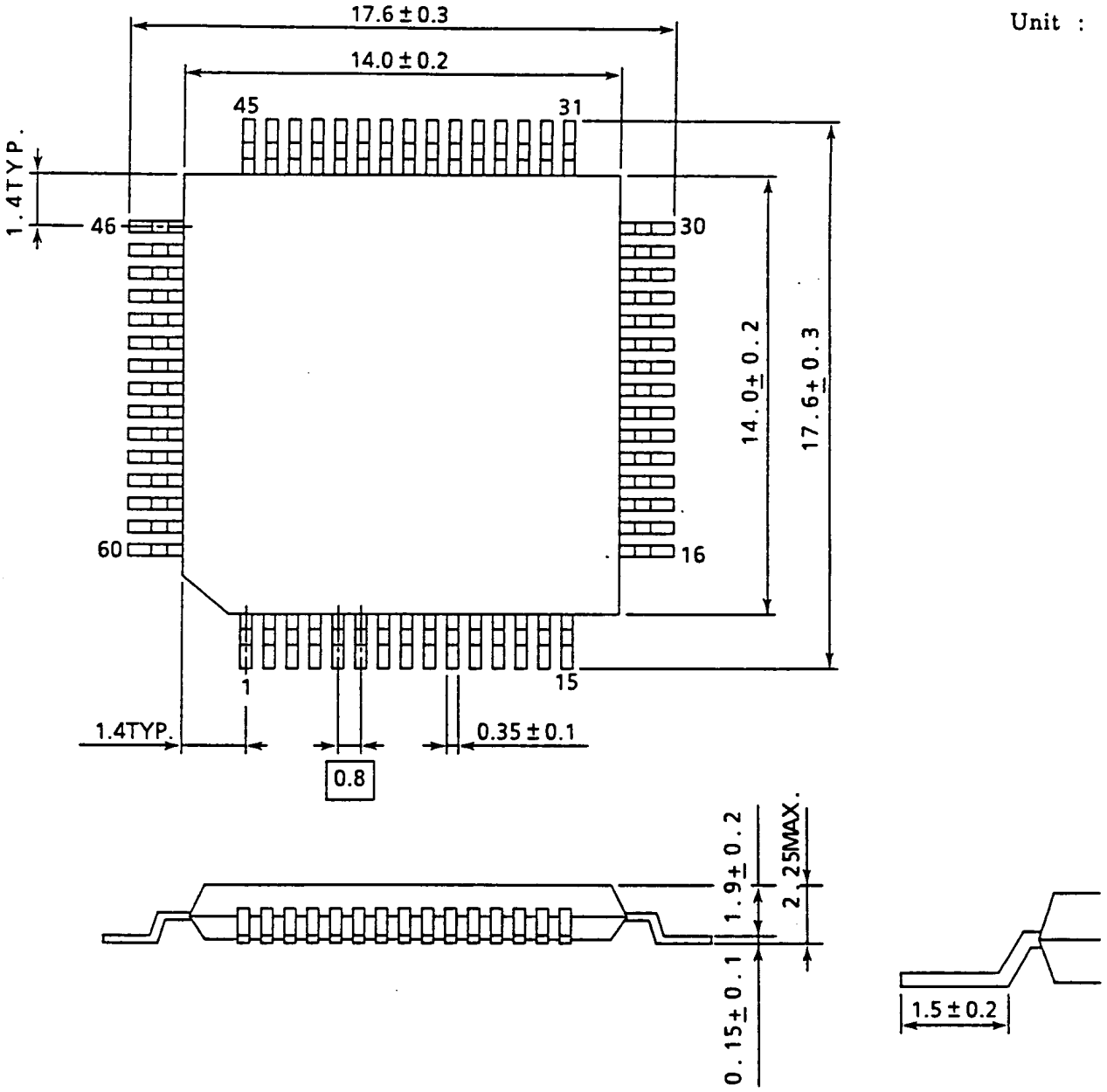


Fig 8.1 TC8861F Package Dimensions Diagram

8.2 TC8864F-00

100-pin Flat Package (Package Code QFP100-P-1420 in Toshiba IC Package Manual)

Unit : mm

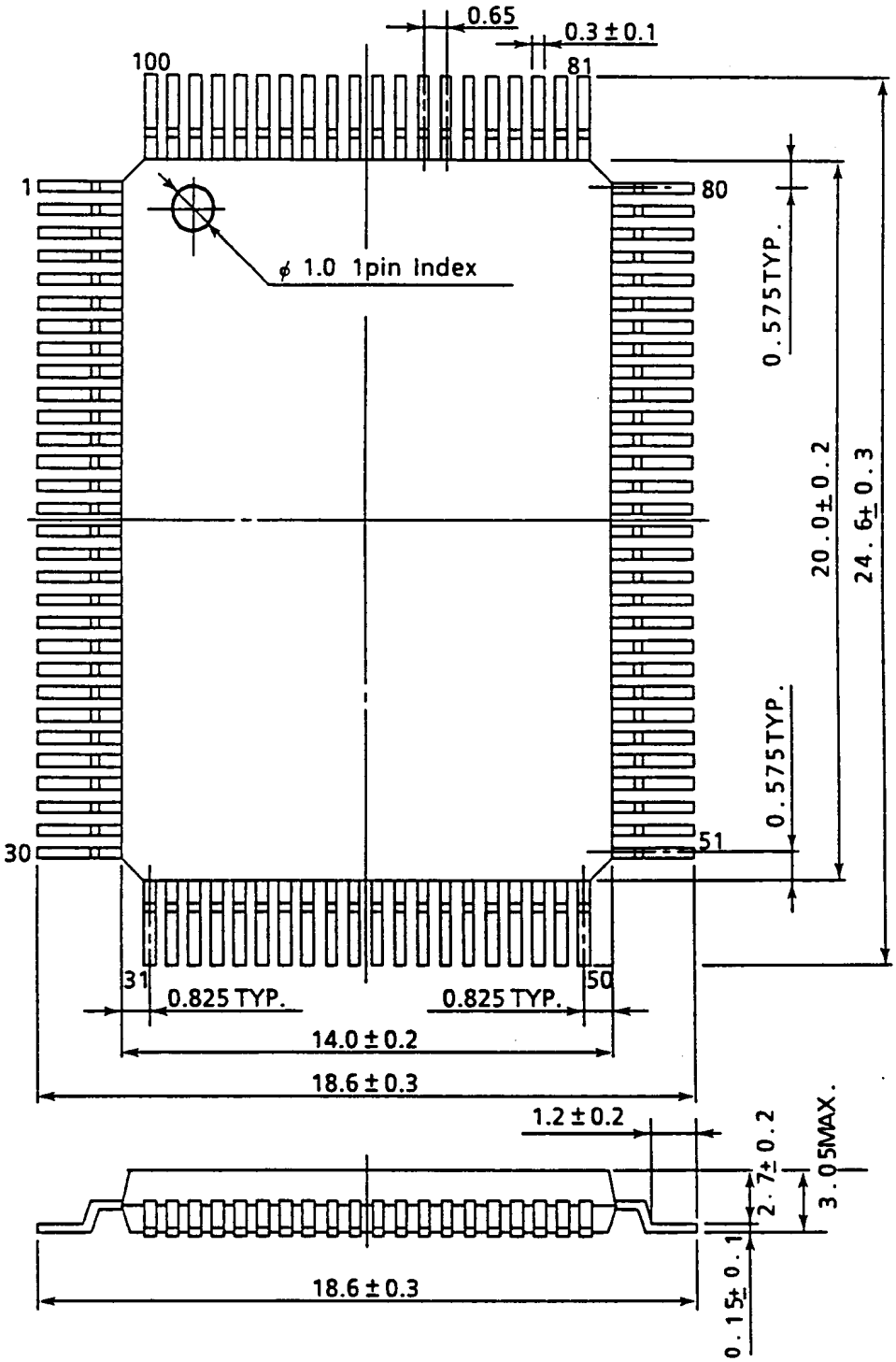
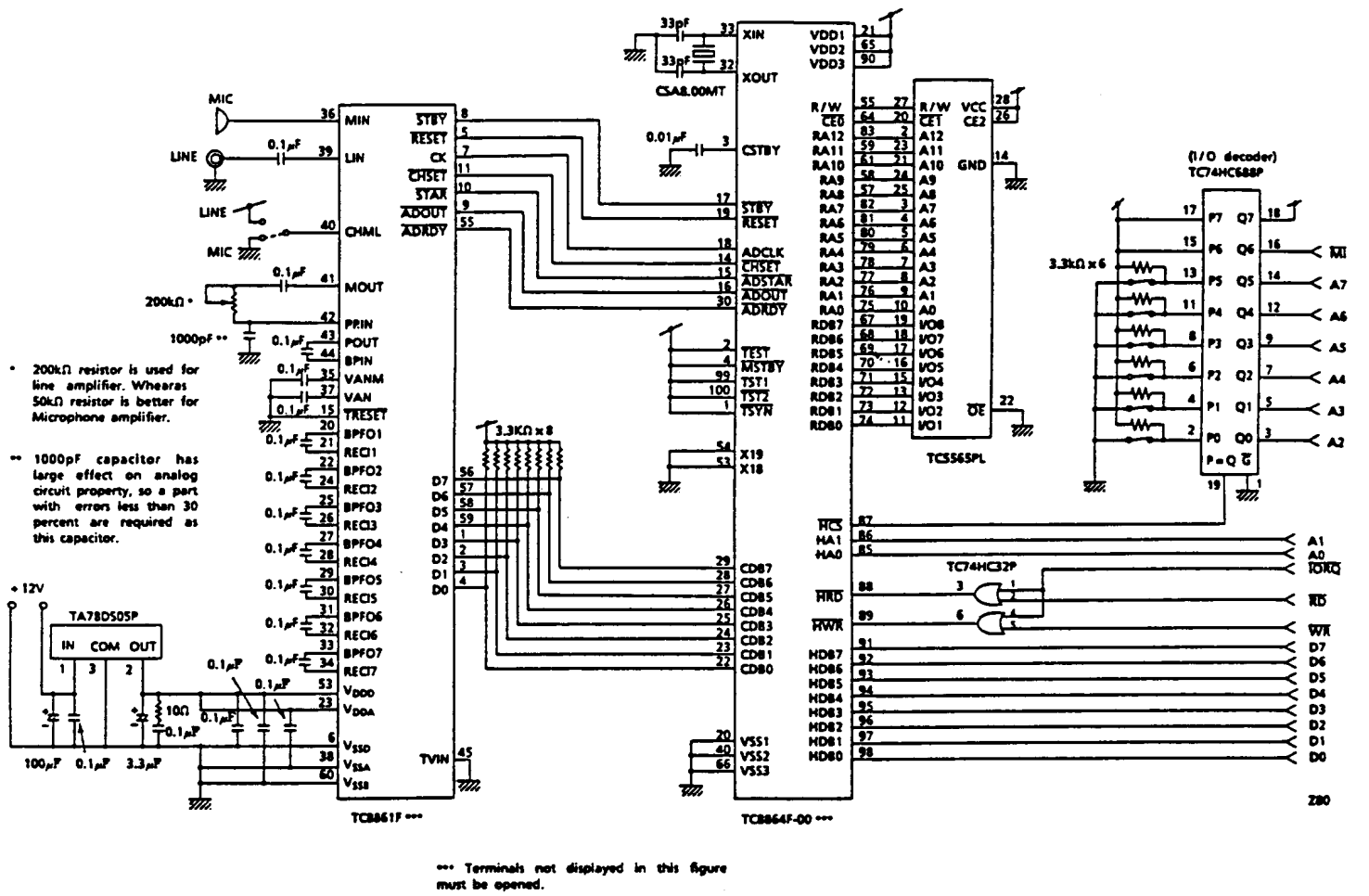


Fig. 8.2 TC8864F-00 Package Dimensions Diagram

9. Application Circuitry Example

Host CPU : Z80



*** Terminals not displayed in this figure must be opened.

Fig. 9.1 Application Circuitry Example