TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9316F,TC9316FA,TC9316FB

DTS Micro Controller Containing PLL, LCD Driver (DTS-11)

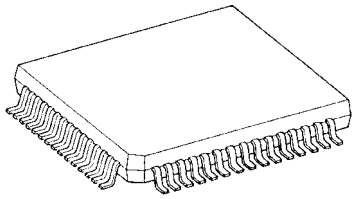
TC9316F/FA/FB are a 4 bit CMOS microcontroller for digital tuning system capable of making 3 V low voltage operation, and containing PLL circuit, LCD driver.

CPU has 4 bit parallel addition and substruction (AI/SI instructions, etc.), logical operation (OR and AN instructions, etc.), plural bit judge, comparison instructions (TM, SL instructions, etc.) and time base function.

The package is 60 pin mini-flat type (TC9316F), 64 pin mini-flat type (TC9316FA, TC9316FB) and has abundant I/O ports and exclusive key-input ports controlled by the powerful input/output instructions (IO, KEY instructions), besides containing PLL circuit.

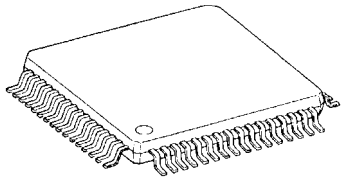
By combining with the prescaler TD6134AF or TD7101F or TD7103F, it permits the configuration of DTS that receives FM/AM and TV (VHF) bands.

TC9316F



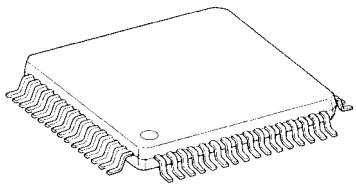
QFP60-P-1414-0.80E

TC9316FA



LQFP64-P-1010-0.50

TC9316FB



QFP64-P-1212-0.65

Weight
QFP60-P-1414-0.80E: 0.85 g (typ.)
LQFP64-P-1010-0.50: 0.32 g (typ.)
QFP64-P-1212-0.65: 0.45 g (typ.)

Features

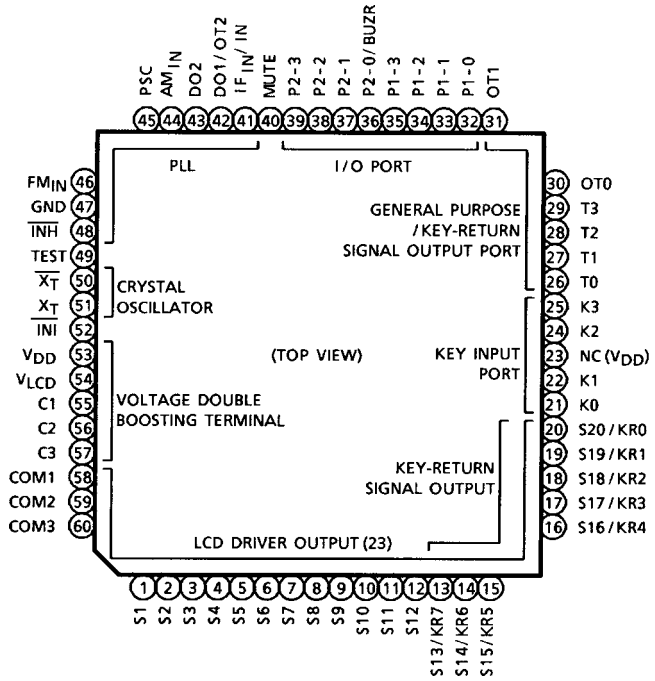
- 4 bit micro controller for digital tuning system use
- It is operated with 3 V single power supply. (V_{DD} = 1.8~3.6 V)
- Back-up of data memory (RAM) and each port are easily made. (by $\overline{INH}$ terminal)
- Built-in LCD driver (1/3 duty, 1/2 bias driving, driving frequency: 52 Hz), and boosting circuit for display
- Program memory (ROM): 16 bit × 2048 steps
- Data memory (RAM): 4 bit × 128 words
- Powerful instruction set of 65 kinds. (all single word instruction)
- Instruction executing time 80 μs. (75 kHz crystal connection)
- Abundant addition and substruction instructions. (addition instructions 12 kinds, substraction instructions 12 kinds)
- Powerful compound judge instructions. (TMTR, TMFR, TMT, TMF, TMTN, TMFN instructions)
- Data transfer in same low address is possible.
- Indirect transfer of register is possible. (MVRD, MVRS, MVGD, MVGS instructions)
- 16 powerful general registers. (arranged in RAM)
- Stack level: 1 level
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instruction can be freely made among 2048 steps.
- At the FM or TV band, swallow counter is composed by combining with prescaler TD6134AF or TD7103F, and is able to receive TV VHF band. At the AM or FM band, swallow counter is composed by combining with prescaler TD7101F, and is able to receive SW, AM, FM band.
- It is possible to freely refer to the content, 16 bits, of optional address within 1024 steps in program memory (ROM). (DAL instruction)
- Independent frequency input terminal at FM and AM (FM_{IN}, AM_{IN}), and two phase-comparator outputs. (DO1, DO2)
- 7 kinds of reference frequency can be selected with program.

- Powerful input/output instructions, (IO, KEY instructions)
- Exclusive input port (K0~K3) for key input use and abundant 23 exclusive LCD driving terminals.
- Abundant 15 I/O ports (ports for which input and output can be assigned for each bit: 8, exclusive output ports: 7)

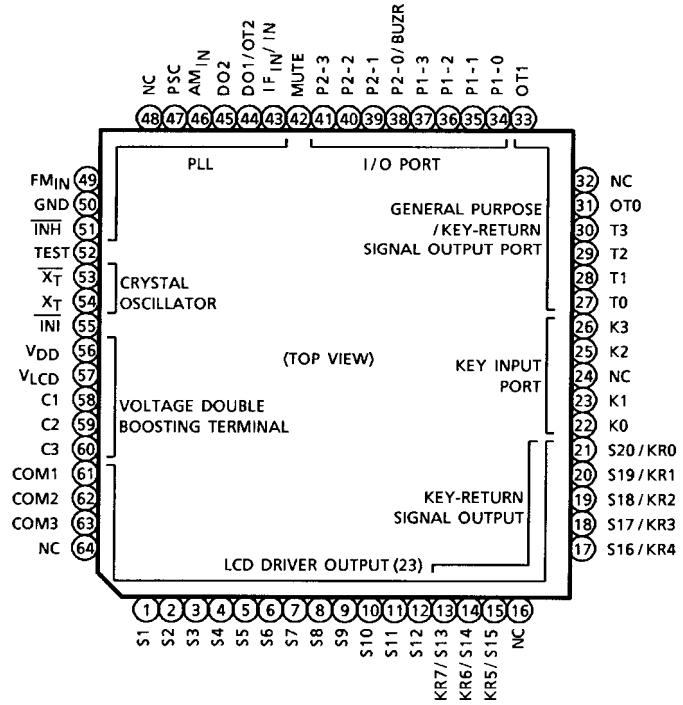
  IF_{IN} port and DO1 port are able to use IN port (exclusive input port) and OT2 port (exclusive output port) by changing instruction.
- 3 kinds of back-up mode (only CPU operating, crystal oscillation and clock stop) are possible by instructions.
- 2 Hz timer F/F and 10 Hz interval pulse output are contained. (internal port for time base use)
- Locked condition of PLL can be detected.
- Universal-type IF counter is built in.
- 8 output ports in LCD segment ports (S13~S20) are able to use as key return timing output ports. Exclusive output ports are not only use key return timing output ports but use the others.
- 16 bit universal-type IF counter is built in, it is able to detect the auto stop signal at auto-tuning mode with counting intermediate frequency of each band.
- Built-in 3 V voltage regulation circuit for driving LCD.

Pin Assignment (top view)

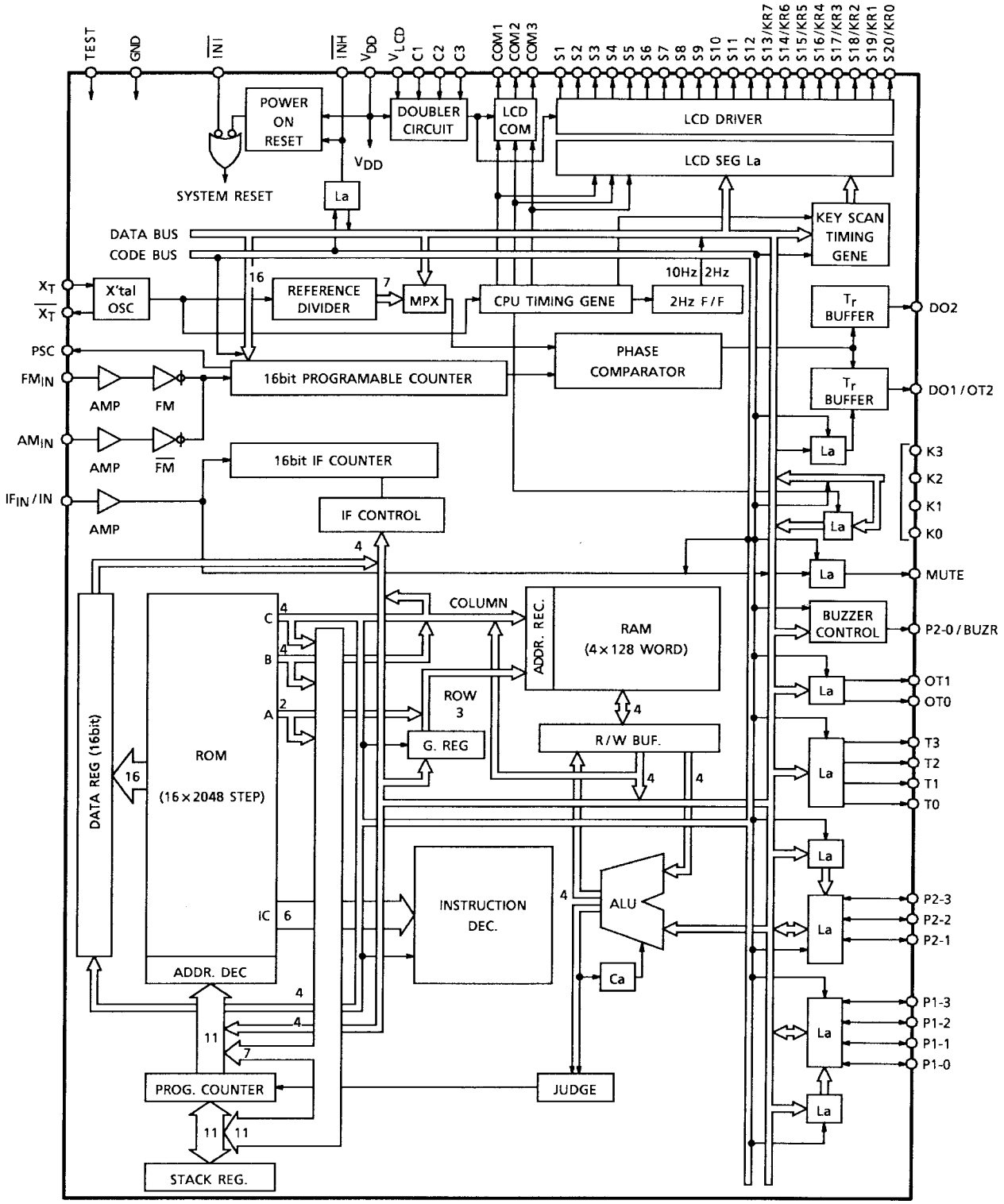
(TC9316F)



(TC9316FA, TC9316FB)

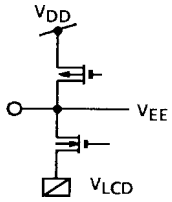
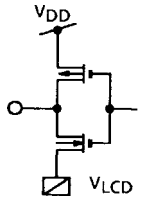
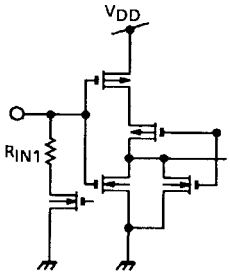
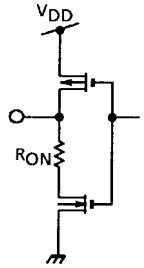
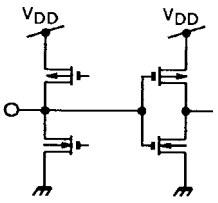


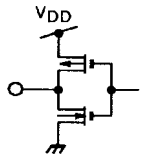
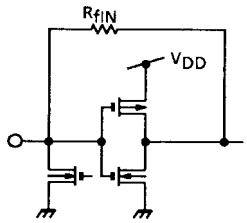
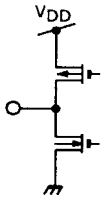
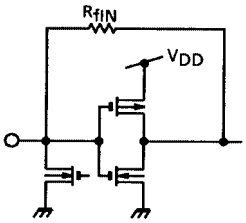
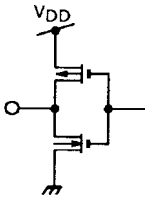
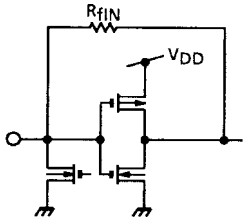
Block Diagram

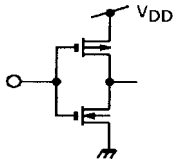
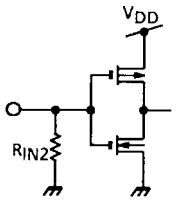
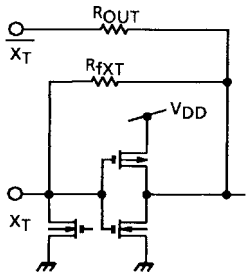
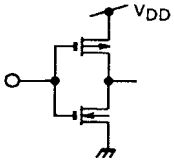


Pin Function

(data in parenthesises are for TC9316FA, TC9316FB)

Pin No.	Symbol	Pin Name	Explanation of Function and Operation	Remarks
58 (61)	COM1	LCD Common Output	This is a common signal output terminal to LCD. Indication of maximum 60 segments is possible with matrix made with S1~S20. To this terminal, three value levels of V_{DD}, V_{EE}, V_{LCD} are output with 3.2 ms interval and 52 Hz cycle.	
59 (62)	COM2			
60 (63)	COM3			
1~12	S1~S12	LCD Segment Output	This is a segment signal output terminal to LCD. Indication of maximum 60 segments is possible with matrix made with COM1, COM2 and COM3. The data for these terminals are output by the execution of SEG instruction and MARK instruction. S13/KR7~S20/KR0 are able to output LCD segment signal and Key Return Timing signal at same time by program. Maximum 32 (= 8 × 4) Key input be able to combine with matrix made with Key input ports K0~K3 without the other output port.	
13~20 (13~15 17~21)	S13/KR7~ S20/KR0	LCD Segment Output/Key Return Output		
21, 22 24, 25 (22, 23 25, 26)	K0~K3	Key Input Port	This is a 4 bit input port for key matrix input. It is able to input data of maximum total 56 key, maximum 24 key (= 6 × 4) with matrix made with Key Return Timing output port, besides maximum 32 key (8 × 4) with matrix made with LCD Segment Output S13/KR7~S20/KR0. All these terminals are built in pull down resistances.	
26~29 (27~30)	T0~T3	General Purpose /Key Return Timing Output Port	This is a 6 bit output port for General Purpose/Key Return Timing output. Besides use for general purpose output port, it is able to output the timing signal for key matrix by program. For making the key matrix, it is built in load resistance at N-ch FET side, useless the diode when uses Push key.	
30, 31 (31, 33)	OT0, OT1			
32~35 (34~37)	P1-0~P1-3	I/O Port	This is a 8 bit general purpose I/O Port. It is possible to assign input and output for each bit by program. P2-0 is able to use as the beep sound pulse output port by program. It is able to output 3 kinds of the beep sound pulse signal by program.	
36 (38)	P2-0/BUZR	I/O Port/Buzzer Pulse Output Port		
37~39 (34~41)	P2-1~P2-3	I/O Port		

Pin No.	Symbol	Pin Name	Explanation of Function and Operation	Remarks
40 (42)	MUTE	Muting Output Port	This is a 1 bit output port. This is usually used as muting control signal output.	
41 (43)	IF_{IN}/IN	If Counter Input Port/Input Port	This is an If signal input terminal of 16 bit general purpose IF counter. This terminal has built-in amplifiers, and operates with C-connection and small amplitude. It is able to use as a 1 bit general purpose input port by program.	
42 (44)	DO1/OT2	Phase Comparator Output/Output port	This is a phase comparator output terminal of PLL. DO1 and DO2 are parallel outputs. Therefore, optimum filter constant can be set for each band of FM/AM. DO1 is able to use as a 1 bit general purpose output port by program.	
43 (45)	DO2	Phase Comparator Output		
44 (46)	AM_{IN}	AM Programmable Counter Input	This is a programmable counter input terminal at 12 bit direct frequency-divider mode. Usually the local oscillator signal at AM band is input to this terminal. This terminal has built-in amplifiers, and operated with C-connection and small amplitude.	
45 (47)	PSC	Prescaler Control Output	This is an output terminal which controls 1/15 or 1/16 frequency-dividing mode of two modulus prescaler. This output signal controls two frequency-dividing mode of external prescaler as using programmable counter for pluse-swallow counter. "H": 1/16, "L": 1/15	
46 (49)	FM_{IN}	FM Programable Counter Input	This is an input terminal of programmable counter at 16 bit swallow-counter mode. This terminal is input the divided frequency output signal of external prescaler, and has built-in input amplifiers and operates with C-connection and small amplitude.	

Pin No.	Symbol	Pin Name	Explanation of Function and Operation	Remarks
48 (51)	$\overline{INH}$	Inhibit Input	This is a signal input terminal for selecting radio mode. "H": radio ON, "L": radio OFF	
49 (52)	TEST	Test Input	This is an input terminal for controlling test mode control. At "H" level, test mode is made, and at "L" level, normal operation is carried out. In the test mode, the device operates as evaluator chip, and program evaluation is made possible on EPROM base through combination with external simulation board. This terminal is built in a pull-down resistance.	
50 (53)	$\overline{X_T}$	Crystal Oscillation Terminal	This is a connecting terminal of crystal resonator. Reference crystal of 75 kHz is connected. During the execution of CKSTP instruction, oscillation is automatically stopped.	
51 (54)	X_T			
52 (55)	$\overline{INI}$	Initializing Input	This is a system reset signal input terminal of the device. During $\overline{INT}$ is at "L" level, reset is applied, and when it becomes "H" level, it is normal operation mode.	
54 (57)	V_{LCD}	Voltage Double Boosting Terminal	These are voltage double boosting terminal for driving LCD. Boosting capacitors are connected to these terminals. (typ. 0.1 μF~3.3 μF)	—
55 (58)	C1			
56 (59)	C2			
57 (60)	C3	Reference Voltage Stabilizing Capacitor Connecting Terminal	The stabilizing capacitor of Reference Voltage is connected to this terminal for LCD driving. (typ. 0.01 μF~0.1 μF)	—
53 (56)	V_{DD}	Power Supply Terminal	Power supply voltage is applied. V_{DD} = 1.8~3.6 V (typ. 3.0 V)	—
47 (50)	GND			

Explanation of Operation

CPU

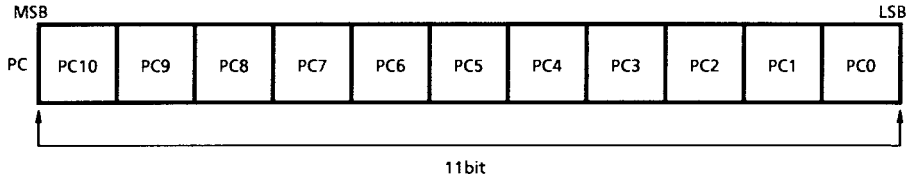
CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, carry F/F and judging circuit.

1. Program Counter (PC)

Program Counter is a block to designate the address of program memory (ROM), and is composed of 11 bits binary up counter. This is cleared by system reset, and the program starts from zero address.

Usually, it's increment is made one by one everytime the one instruction is executed, but when JUMP instruction or CAL instruction is executed, the address designated at operand part of that instruction is loaded.

Further, when the instruction (AIS, SLT, TMT, RNS instructions, etc.) having skip function is executed, two increments of program counter is made if the result is the condition to be skipped, and the succeeding instruction is skipped.



2. Stack Register (STACK)

This is a register composed of 1 × 11 bits during the execution of subroutine call instruction, the value obtained by adding +1 to the content of program counter, namely return address, is housed. The content of stack register is loaded on the program counter by the execution of return instruction. (RN, RNS instructions)

This stack level is 1 level, and nesting is 1 level.

3. ALU

ALU has binary 4 bits parallel addition and subtraction, logical operation, comparison and plural bit judge functions.

This CPU has no accumulator, and all operations directly treat the contents of data memory.

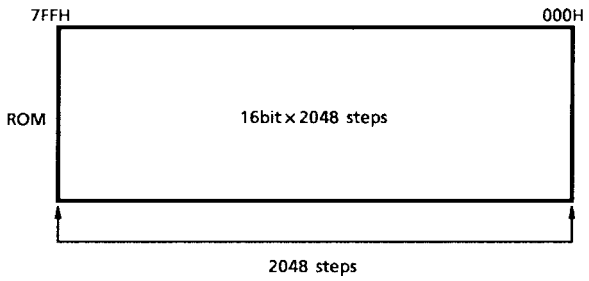
4. Program Memory (ROM)

Program memory is composed of 16 bit × 2048 steps and is the address of 000H~7FFH.

Program memory has no concept of page or field, so JUMP instruction and CAL instruction can be freely used among 2048 steps.

Further, it is possible to use optional address of program memory as data area, and its content, 16 bits, can be loaded to the data register by executing DAL instruction.

Note 1: Provide the data area at the address outside the program loop in the program memory.



Note 2: In DAL instruction, the address of program memory can be designated as the data area becomes 1024 steps of 000H~3FFH.

5. Data Memory (RAM)

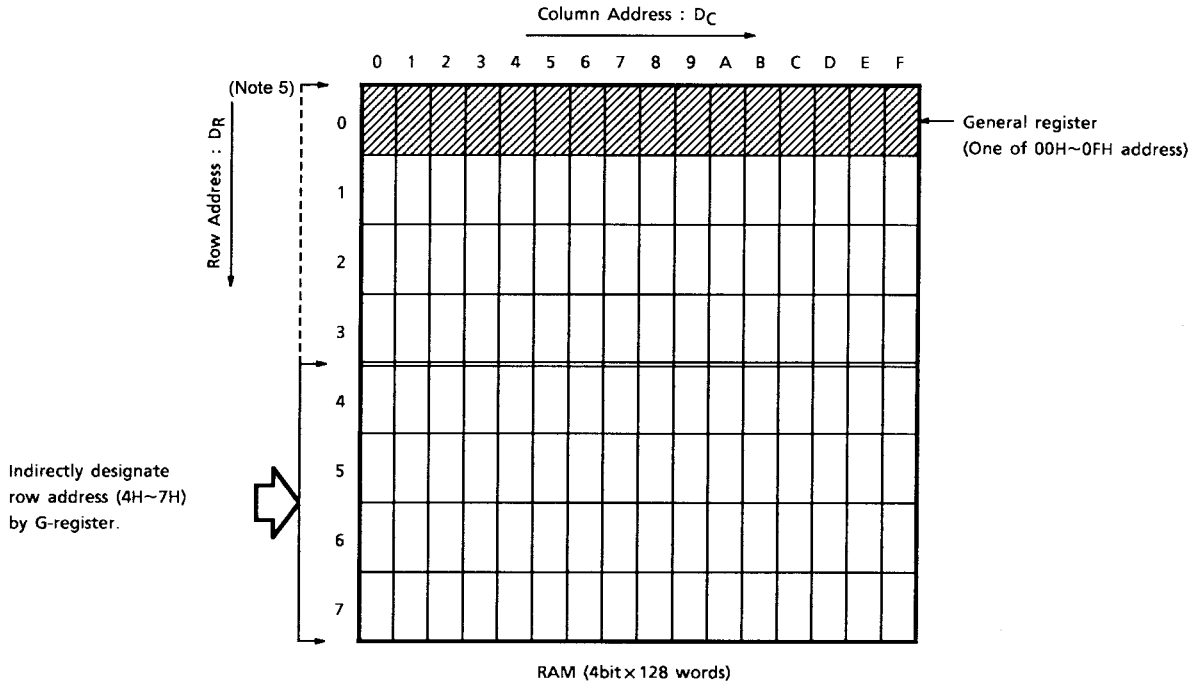
Data memory is composed of 4 bit × 128 words and used for storing data.

This 128 words are expressed with row address (3 bits) and column address (4 bits).

64 words (row address = 4H~7H) among the data memory are indirect addressing by G-register. For this reason, when carrying out data processing within this territory, it is necessary to designate row address by G-register beforehand Area of 00H~0FH address in data memory is called general register, and can be used only by designating column address (4 bits). These 16 general registers can be used for operation and transfer between data memories. Further, it can also be used as ordinary data memory.

Note 3: The column address (4 bits) to designate general register becomes register number of the general register.

Note 4: It is also possible to indirectly designate all of row address (= 0H~7H) by G-register.



Note 5: Indirect designation of row address (0H~7H) is also possible

6. G-Register (G-REG.)

G-register is a 3 bits register for addressing row address (D_R = 4H~7H) of 64 words in data memory.

Content of this register is effective during executing MVGD instruction, MVGS instruction, and is not related with the execution of other instructions.

This register is treated as one of the port, and its content is set by the execution of IO instruction among input and output instructions.

(refer to register port item 1)

7. Data Register (DATA REG.)

This is a register composed of 1 × 16 bits. In this register, 16 bits data of optional address among the program memory is loaded during executing of DAL instruction. This register is treated as one of the port, and when KEY instruction among input and output instruction is executed, it's content is read in the data memory in 4 bits unit.

(refer to register port item 2)

8. Carry F/F (C·F/F)

This is set when carry or borrow is produced as a result of executing operational instruction, and is reset when it is not produced. Content of carry F/F changes only when addition and subtraction instruction is executed, and does not change during the execution of other instructions.

9. Judging Circuit (J)

When a instruction with skip function is executed, this circuit judges it's skip condition. When skip condition is satisfied, this circuit makes two increments of program counter, and skips the succeeding instruction.

It is provided with 31 kinds of instructions having abundant skip function.

(refer to Item 11, explanation list of function and operation of instructions, * marked instruction)

10. List of Instructions Set

65 kinds of instruction set are included, all of which consisting of one word instruction.

These instructions are expressed with 6 bits instruction code.

Higher Rank 2 Bits / Lower Rank 4 Bits		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	LD r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	ST M, r	SGEI M, I
0010	2	AIN M, I	ADN r, M	MVRD r, M	SEQI M, I
0011	3	SI M, I	SU r, M	MVRS M, r	SNEI M, I
0100	4	SIS M, I	SUS r, M	MVSR M_1, M_2	SLT r, M
0101	5	SIN M, I	SUN r, M	MVIM M, I	SGE r, M
0110	6	CAL $ADDR_1$	ORR r, M	MVGD r, M	SEQ r, M
0111	7		ANDR r, M	MVGS M, r	SNE r, M
1000	8	AIC M, I	AC r, M	PLL M, C	TMTR r, M
1001	9	AICS M, I	ACS r, M	SEG M, C	TMFR r, M
1010	A	AICN M, I	ACN r, M	MARK M, C	TMT M, N
1011	B	SIB M, I	SB r, M	IO M, C	TMF M, N
1100	C	SIBS M, I	SBS r, M	KEY M, C	TMTN M, N
1101	D	SIBN M, I	SBN r, M	WAIT P	TMFN M, N
1110	E	JUMP $ADDR_1$	ORIM M, I	XORIM M, I	DAL $ADDR_2$, r
1111	F		ANIM M, I	XORR r, M	RN, RNS, CKSTP, NOOP

11. Explanation List of Function and Operation of Instructions (explanation of symbols)

M: Data memory address
Normally, one of 00H~3FH address of data memory.
r: General register
One of 00H~0FH address of data memory.
PC: Program counter (11 bit)
STACK: Stack register (11 bit)
G: G-register (3 bit)
DATA: Data register (16 bit)
I: Immediate data (4 bit)
N: Bit position (4 bit)
—: All "0"
C: Code No. of port (4 bit)
C_N: Lower rank 3 bit of port code No.
R_N: General register No. (4 bit)
$ADDR_1$: Program memory address in page 0 or 1 (10 bit)
$ADDR_2$: Higher rank 6 bit of program memory address in page 0
Ca: Carry
b: Borrow
PLL: Port treated during the execution of PLL instruction
SEG: Port treated during the execution of SEG instruction
MARK: Port treated during the execution of MARK instruction
IO: Port treated during the execution of IO instruction
KEY: Port treated during the execution of KEY instruction
( ): Register or data memory content
[ ] $_C$: Content of port indicated by code No. C (4 bit)
[ ]: Content of data memory indicated by the content of register or data memory
[ ] $_P$: Content of program memory (16 bit)
IC: Instruction code (6 bit)
*: Instruction having skip function
D_C: Data memory column address (4 bit)
D_R: Data memory row address (2 bit)
P: Wait condition select bit at WAIT instruction

Note 6: Address 000H~3FFH of program memory address: Page 0 area

Address 400H~7FFH of program memory address: Page 1 area

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
ADDITION INSTRUCTION	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	D_R	D_C	I
	AIS	M, I	*	Add immediate data to memory, then skip if carry	M ← (M) + I Skip if carry	000001	D_R	D_C	I
	AIN	M, I	*	Add immediate data to memory, then skip if not carry	M ← (M) + I Skip if not carry	000010	D_R	D_C	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	001000	D_R	D_C	I
	AICS	M, I	*	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + ca Skip if carry	001001	D_R	D_C	I
	AICN	M, I	*	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + ca Skip if not carry	001010	D_R	D_C	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	010000	D_R	D_C	R_N
	ADS	r, M	*	Add memory to general register, then skip if carry	r ← (r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN	r, M	*	Add memory to general register, then skip if not carry	r ← (r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	011000	D_R	D_C	R_N
	ACS	r, M	*	Add memory to general register with carry, then skip if carry	r ← (r) + (M) + ca Skip if carry	011001	D_R	D_C	R_N
	ACN	r, M	*	Add memory to general register with carry, then skip if not carry	r ← (r) + (M) + ca Skip if not carry	011010	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
SUBTRACTION INSTRUCTION	SI	M, I		Subtract immediate data from memory	M ← (M) – I	000011	D_R	D_C	I
	SIS	M, I	*	Subtract immediate data from memory, then skip if borrow	M ← (M) – I Skip if borrow	000100	D_R	D_C	I
	SIN	M, I	*	Subtract immediate data from memory, then skip if not borrow	M ← (M) – I Skip if not borrow	000101	D_R	D_C	I
	SIB	M, I		Subtract immediate data from memory, with borrow	M ← (M) – I – b	001011	D_R	D_C	I
	SIBS	M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN	M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU	r, M		Subtract memory from general register	r ← (r) – (M)	010011	D_R	D_C	R_N
	SUS	r, M	*	Subtract memory from general register, then skip if borrow	r ← (r) – (M) Skip if borrow	010100	D_R	D_C	R_N
	SUN	r, M	*	Subtract memory from general register, then skip if not borrow	r ← (r) – (M) Skip if not borrow	010101	D_R	D_C	R_N
	SB	r, M		Subtract memory from general register with borrow	r ← (r) – (M) – b	011011	D_R	D_C	R_N
	SBS	r, M	*	Subtract memory from general register with borrow, then skip if borrow	r ← (r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN	r, M	*	Subtract memory from general register with borrow, then skip if not borrow	r ← (r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N
COMPARISON INSTRUCTION	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SLT	r, M	*	Skip if general register is less than memory	Skip if (r) < (M)	110100	D_R	D_C	R_N
	SGE	r, M	*	Skip if general register is greater than or equal to memory	Skip if (r) ≧ (M)	110101	D_R	D_C	R_N
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	110110	D_R	D_C	R_N
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	110111	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
TRANSFER INSTRUCTION	LD	r, M		Load memory to general register	$r \leftarrow (M)$	100000	D_R	D_C	R_N
	ST	M, r		Store general register to memory	$M \leftarrow (r)$	100001	D_R	D_C	R_N
	MVRD	r, M		Move memory to destination memory referring to general register in the same row	$[D_R, (r)] \leftarrow (M)$	100010	D_R	D_C	R_N
	MVRS	M, r		Move source memory referring to general register to memory in the same row	$M \leftarrow [D_R, (r)]$	100011	D_R	D_C	R_N
	MVSR	M1, M2		Move memory to memory in the same row	$(D_R, D_{C1}) \leftarrow (D_R, D_{C2})$	100100	D_R	D_{C1}	D_{C2}
	MVIM	M, I		Move immediate data to memory	$M \leftarrow I$	100101	D_R	D_C	I
	MVGD	r, M		Move memory to destination memory referring to G-register and general register	$[(G), (r)] \leftarrow (M)$	100110	D_R	D_C	R_N
	MVGS	M, r		Move source memory referring to G-register and general register to memory	$M \leftarrow [(G), (r)]$	100111	D_R	D_C	R_N
INPUT AND OUTPUT INSTRUCTION	PLL	M, C		Input PLL port data to memory	$M \leftarrow [PLL]_C$	101000	D_R	D_C	0 C_N
				Output contents of memory to PLL port	$[PLL]_C \leftarrow (M)$		D_R	D_C	1 C_N
	SEG	M, C		Output contents of memory to SEG port	$[SEG]_C \leftarrow (M)$	101001	D_R	D_C	1 C_N
	MARK	M, C		Input MARK port data to memory	$M \leftarrow [MARK]_C$	101010	D_R	D_C	0 C_N
				Output contents of memory to MARK port	$[MARK]_C \leftarrow (M)$		D_R	D_C	1 C_N
	IO	M, C		Input IO port data to memory	$M \leftarrow [IO]_C$	101011	D_R	D_C	0 C_N
				Output contents of memory to IO port	$[IO]_C \leftarrow (M)$		D_R	D_C	1 C_N
	KEY	M, C		Input KEY port data to memory	$M \leftarrow [KEY]_C$	101100	D_R	D_C	0 C_N
				Output contents of memory to KEY port	$[KEY]_C \leftarrow (M)$		D_R	D_C	1 C_N
LOGICAL OPERATION INSTRUCTION	ORR	r, M		Logical OR of general register and memory	$r \leftarrow (r) \vee (M)$	010110	D_R	D_C	R_N
	ANDR	r, M		Logical AND of general register and memory	$r \leftarrow (r) \wedge (M)$	010111	D_R	D_C	R_N
	ORIM	M, I		Logical OR of memory and immediate data	$M \leftarrow (M) \vee I$	011110	D_R	D_C	I
	ANIM	M, I		Logical AND of memory and immediate data	$M \leftarrow (M) \wedge I$	011111	D_R	D_C	I
	XORIM	M, I		Logical exclusive OR of memory and immediate data	$M \leftarrow (M) \oplus I$	101110	D_R	D_C	I
	XORR	r, M		Logical exclusive OR of general register and memory	$r \leftarrow (r) \oplus (M)$	101111	D_R	D_C	I

Inst. Gr.	Mnemonic	Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
					IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
BIT JUDGE INSTRUCTION	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	111000	D_R	D_C	R_N
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	111001	D_R	D_C	R_N
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	111010	D_R	D_C	N
	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	111011	D_R	D_C	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	111100	D_R	D_C	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	111101	D_R	D_C	N
SUBROUTINE INSTRUCTION	CALL $ADDR_1$		Call subroutine in page 0	STACK ← (PC) + 1 and PC ← $ADDR_1$ in page 0 or 1	000110	$ADDR_1$ (10 bit)		
			Call subroutine in page 1		000111			
	RN		Return to main routine	PC ← (STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	01	—	—
JUMP INST.	JUMP $ADDR_1$		Jump to the address specified in page 0	PC ← $ADDR_1$ in page 0 or 1	001110	$ADDR_1$ (10 bit)		
			Jump to the address specified in page 1		001111			
OTHER INSTRUCTION	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode)	Wait at condition P	101101	P	—	—
			At P = "1" H, except for clock generator, all function is waiting (hard wait mode)				—	—
	DAL $ADDR_2$, r		Load program memory in page 0 to DATA register	DATA ← [$ADDR_2$ + (r)] P in page 0	111110	$ADDR_2$ (6 bit)		R_N
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH}$ = "0"	111111	10	—	—
	NOOP		No operation	—	111111	11	—	—

Note 7: During the execution of input and output instruction, control of input/output instruction is automatically carried out at the most significant bit in code No. (C) of port.

- MSB = "1" of code No. (C): Output instruction
- MSB = "0" of code No. (C): Input instruction

Note 8: In the TC9316F, TC9316FA, TC9316FB, only the SEG instruction is carried out output instruction in spite of Code No. (C) of MSB.

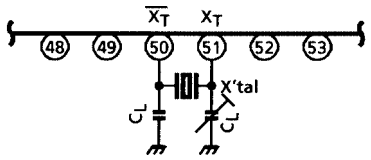
Note 9: Among 10 bits of the program memory address assigned by DAL instruction, the lower rank of 4 bits become indirect addressing based on the content of general register.

DAL instruction executing time is 160 μs.

Connection of Crystal Resonator

Connect 75 kHz crystal resonator with the crystal oscillator terminals (X_T, $\overline{X_T}$ terminal) of the device as shown below. This oscillation signal is supplied to clock generator and reference frequency divider, and produced each timing signal of CPU and reference frequency signal.

Adjust the crystal oscillation frequency while monitoring LCD segment output terminal.



X'tal = 75 kHz

C_L = 30 pF typ.

Note 10: In TC9316FA, TC9316FB, $\overline{X_T}$ = pin 53, X_T = pin 54.

Note 11: Use crystal resonator of low CI value and satisfactory starting characteristics.

System Reset

System reset is applied to the device when "L" level is given to $\overline{INI}$ terminal, or when the voltage, 0 V → 1.8 V~3.6 V is supplied to V_{DD} terminal (power on reset).

After the lapse of 100 ms stand-by time succeeding to the system reset, program starts from zero address.

As power on reset function is employed usually, $\overline{INI}$ terminal is fixed at "H" level.

Note 12: During the system reset time and the succeeding stand-by time, LCD common output and segment output are fixed at "L" level.

Note 13: After system reset, all of I/O ports are set at input mode, but initialization of output port and internal port (G-register, etc.) is not carried out. Especially, at the initial power on stage, content of these ports is indefinite, and therefore it is necessary to make initialization with program according to your use.

Back Up Mode

If CKSTP instruction or WAIT instruction is executed when $\overline{INH}$ terminal is at "L" level, it can select for the three kinds of back up mode.

1. Clock Stop Mode

If CKSTP instruction is executed when $\overline{INH}$ terminal is at "L" level, clock generator and CPU internal of the device stop operation completely, and memory back up state can be realized at low current consumption (1 μA max at V_{DD} = 3 V).

At this time, LCD display driver terminals and output ports are all fixed at "L" level or off condition. During this clock stop mode, supply voltage can be reduced down to 1.2 V and used for exchange of battery.

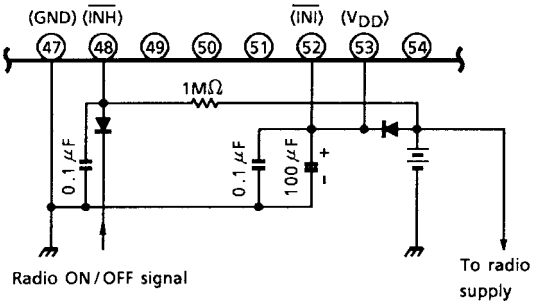
So this mode is available when the battery is changed in the radio set.

In clock stop mode, program stops at the execution address of CKSTP instruction.

The clock stop mode is released at $\overline{INH}$ = "H" level or changing the input condition of I/O port (IO0~IO3) set at input mode, and the next address is executed after the lapse of stand-by time of 100 ms.

Note 14: In the clock stop mode, the condition of output terminal is all fixed at "L" level or off but output port holds on the data just before clock stop mode.

Note 15: When CKSTP instruction is executed during $\overline{INH}$ = "H" level, the same operation as NOOP instruction is made (clock stop mode is not entered).



Note 16: In TC9316FA, TC9316FB change pin No. changes as below.

47 → 50

48 → 51

≀ ≀

52 → 55

53 → 56

Example of the Memory Back Up Circuit Using Capacitor at Clock Stop Mode

2. Waiting Mode

If WAIT instruction is executed when $\overline{INH}$ terminal is at "L" level, it can select the hardware waiting mode or the software waiting mode.

(1) Software waiting mode

If WAIT instruction is executed at designated operand port [P = 0H], only CPU internal of the device stop operation, and software waiting mode can be realized at low current consumption. Since the other part of clock generator and display circuit operate normally, at the time of using the program of clock function, the software waiting mode is effective to realize at low current consumption during the clock operation.

(2) Hardware waiting mode

If WAIT instruction is executed at designated operand part [P = 1H], all the function without crystal oscillator are stopped and hardware waiting mode can be realized at lower current consumption than software waiting mode (under 100 μA at V_{DD} = 3.0 V). At this time, CPU and display circuit stop operation, output terminal for LCD display is fixed at "L" level automatically.

In these waiting mode, program stops at the execution address of WAIT instruction, and waiting is released in following condition, so next address is executed.

(3) Released condition of waiting mode

- Changing to $\overline{INH}$ = "H" level
- Key input terminal (K0~K3) is set at "H" level.
- 2 Hz timer F/F is set at "1".
- Changing the input condition of I/O port (IO0~IO3) set at input mode
- MUTE port is set at "1".

Note 17: In waiting mode, each of output terminal is held on the condition just before waiting mode.

I/O Map

I/O Port / Code No.		PLL (ϕ1)				SEG (ϕ2)				MARK (ϕ3)				IO (ϕ4)				KEY (ϕ5)			
		Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
INPUT PORT (K)	0					S1			*	KEY RETURN DATA (KR0, T0)				MUTE	0	0	0				
						COM1	COM2	COM3		K0	K1	K2	K3								
	1	IF COUNTER				S2			*	KEY RETURN DATA (KR1, T1)				I/O PORT-1				KEY RETURN DIGIT No.			SCAN BUSY
		F0	F1	F2	F3	COM1	COM2	COM3		K0	K1	K2	K3	P1-0	P1-1	P1-2	P1-3	SCAN1	SCAN2	SCAN3	
	2	IF COUNTER				S3			*	KEY RETURN DATA (KR2, T2)				I/O PORT-2				KEY INPUT			
		F4	F5	F6	F7	COM1	COM2	COM3		K0	K1	K2	K3	P2-0	P2-1	P2-2	P2-3	k_0	k_1	k_2	k_3
	3	IF COUNTER				S4			*	KEY RETURN DATA (KR3, T3)											
		F8	F9	F10	F11	COM1	COM2	COM3		K0	K1	K2	K3								
	4	IF				S5			*	KEY RETURN DATA (KR4, OT0)				$\overline{INH}$	0	0	0	DATA REGISTER			
		F12	F13	F14	F15	COM1	COM2	COM3		K0	K1	K2	K3					D_0	D_1	D_2	D_3
	5	IF COUNTER				S6			*	KEY RETURN DATA (KR5, OT1)				2 Hz F/F	10 Hz	KEY ON	0	DATA REGISTER			
		BUSY	MANUAL	OVFLOW	0	COM1	COM2	COM3		K0	K1	K2	K3					D_4	D_5	D_6	D_7
	6	UNLOCK DETECTION	TEST ENABLE	IN	0	S7			*	KEY RETURN DATA (KR6)								DATA REGISTER			
						COM1	COM2	COM3		K0	K1	K2	K3					D_8	D_9	D_{10}	D_{11}
	7					S8			*	KEY RETURN DATA (KR7)								DATA REGISTER			
						COM1	COM2	COM3		K0	K1	K2	K3					D_{12}	D_{13}	D_{14}	D_{15}
OUTPUT PORT (L)	8	REF SELECT			FM	S9			*	S17			*	MUTE	*	*	*	MUTE CONTROL			BUZR CONTROL
		#0	#1	#2		COM1	COM2	COM3		COM1	COM2	COM3						$\overline{INH}$	I/O	POL	
	9	PROGRAMMABLE COUNTER				S10			*	S18			*	I/O PORT-1				I/O PORT-1 CONTROL			
		P0	P1	P2	P3	COM1	COM2	COM3		COM1	COM2	COM3		P1-0	P1-1	P1-2	P1-3	P1-0	P1-1	P1-2	P1-3
	A	PROGRAMMABLE COUNTER				S11			*	S19			*	I/O PORT-2				I/O PORT-2 CONTROL			
		P4	P5	P6	P7	COM1	COM2	COM3		COM1	COM2	COM3		P2-0	P2-1	P2-2	P2-3	P2-0	P2-1	P2-2	P2-3
	B	PROGRAMMABLE COUNTER				S12			*	S20			*	BUZR CONTROL				KEY RETURN CONTROL			
		P8	P9	P10	P11	COM1	COM2	COM3		COM1	COM2	COM3		#0	#1	#2	#3	#0	#1	PULL-DOWN	ENABLE
	C	PROGRAMMABLE COUNTER				S13			*	DISP OFF	*			G-RESISTER			*	LCD KEY RETURN CONTROL			
		P12	P13	P14	P15	COM1	COM2	COM3						#0	#1	#2		#0	#1	#2	ENABLE
	D	IF COUNTER CONTROL				S14			*					2 Hz RESET	CLOCK RESET	*	*	OUTPUT PORT KEY RETURN CONTROL			
		STA/$\overline{STP}$	MANUAL	#0	#1	COM1	COM2	COM3										#0	#1	#2	ENABLE
	E	UNLOCK RESET	IN CONTROL	*	*	S15			*					GENERAL OUTPUT PORT							
						COM1	COM1	COM3						T0	T1	T2	T3				
F						S16			*					GENERAL OUTPUT PORT			OT2 CONTROL	TEST			*
						COM1	COM2	COM3						OT0	OT1	OT2		#0	#1	#2	

Note 18: Only the SEG instruction is carried out OUTPUT instruction in spite of code No. (C).

I/O Map

All ports in the device are expressed by matrix of five input and output instruction (PLL instruction, SEG instruction, MARK instruction, IO instruction, KEY instruction) and 4 bits of code No.C.

Assignment of these ports is indicated previously as I/O map. In the I/O map, port names treated in the execution of each input and output instruction are assigned horizontally, while code No. of port are assigned vertically. G-register and data register are also treated as port.

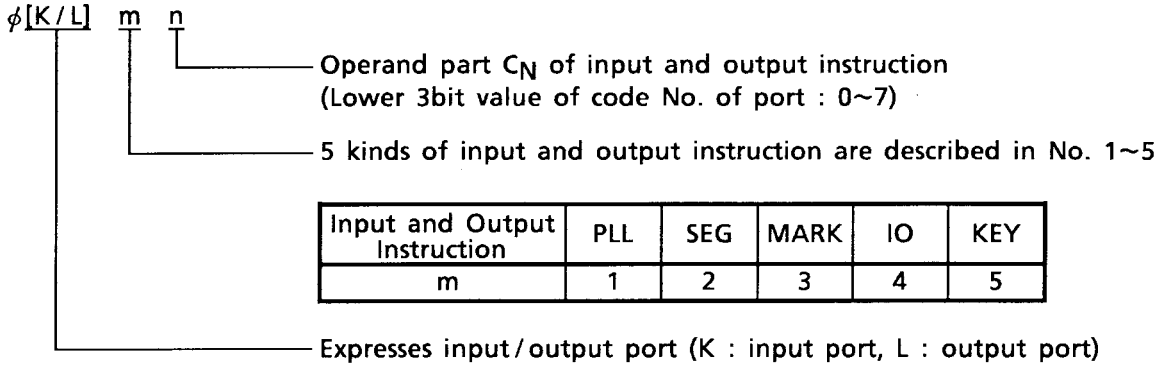
Basically, the data is treated at each port as 4 bits unit, and code No. (C) = 0H~7H are assigned to input port, while code No. (C) = 8H~FH are assigned to output port.

Note 19: The port indicated with oblique line on I/O map is a port not existing in the device. In the execution of output instruction, when data is output to the non-existing output port, no effect is given to the content of other port or data memory. When non-existing input port is designated during the execution of input instruction, the content read into the data memory becomes indefinite.

Note 20: Among the output ports on I/O map, * marked port is unused port. The data output here becomes “don’t care”.

Note 21: Regarding the content of port expressed in 4 bits, Y1 corresponds to the least significant of the data of data memory, and Y8 to the most significant bit. Data of each port is all treated with positive logic.

Note 22: Each port assigned by five input and output instruction and code No. C is coded as follows:



Input and Output Instruction	PLL	SEG	MARK	IO	KEY
m	1	2	3	4	5

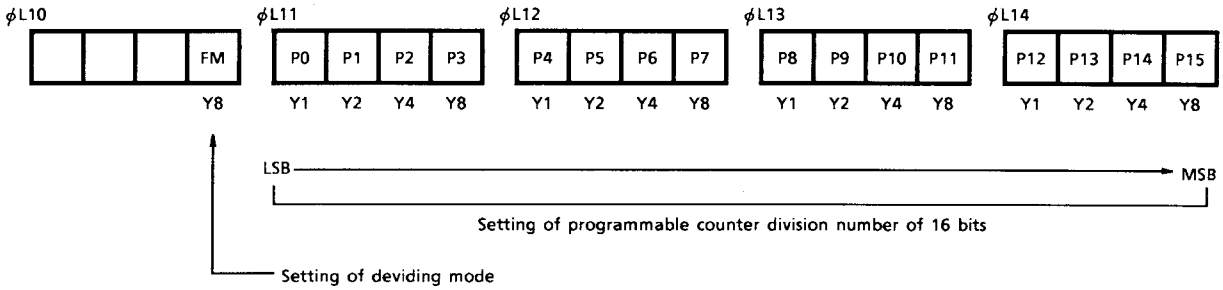
Programmable Counter

Programmable counter block is composed of external two modulus prescaler TD6134AF, 4 bits + 12 bits programmable binary counter, and PLL output ports to control them.

1. PLL Output Port (ϕL10~ϕL14)

The exclusive PLL port is used to control the division number and the dividing mode and made access by PLL output instruction designated operand part [C_N = 0~4].

(1) Structure of PLL port



(2) Setting of dividing mode

Pulse swallow mode or direct dividing mode are selected by FM port. In AM band, it selects the direct dividing mode. In SW, FM, VHF or TV band, it selects pulse swallow mode combined with external two modulus prescaler, TD6134AF, TD7101F, TD7103F.

FM	Dividing Mode	Example of Reception Band	Operating Frequency Range	Input Terminal	Division Number	Prescaler
0	Direct diving mode	MW/LW	0.2~5.0 MHz	AM_{IN}	n	—
1	(1/15 or 1/16) Pulse swallow mode	SW	(Note 23) 1.5~35 MHz	FM_{IN}	n	TD7101F
	1/4 (1/15 or 1/16) Pulse swallow mode	FM	(Note 23) 50~150 MHz		4·n	TD6134AF TD7101F TD7103F
	1/8 (1/15 or 1/16) Pulse swallow mode	VHF/TV	(Note 23) 50~250 MHz		8·n	TD6134F TD7103F

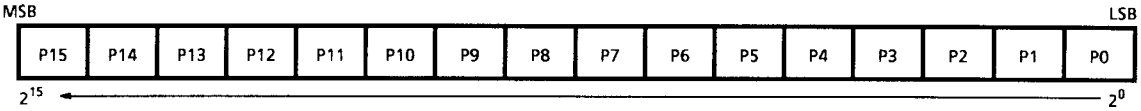
Note 23: This shows the input frequency range to TD6134AF, TD7101F, TD7103F.

Note 24: “n” shows the programmed division number.

(3) Setting of frequency division number

Division number of programmable counter is set on P0~P15 ports with binary.

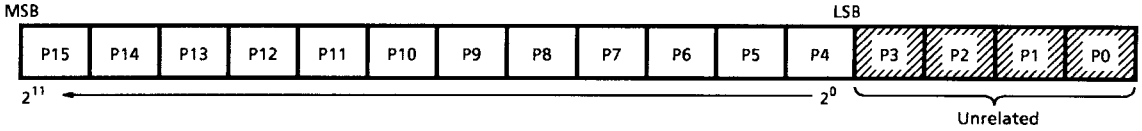
- Pulse-swallow mode (16 bit)



Note 25: Frequency division number setting range (pulse swallow mode)

n = 210H~FFFFH (528~65535)

- Direct dividing mode (12 bit)



Note 26: Frequency division number setting range (direct dividing mode)

n = 10H~FFFH (16~4095)

Note 27: As the programmable counter is not provided with dividing offset, the programmable number becomes the actual frequency division number.

However, in the case of FM band, the actual frequency division number becomes four times of programmed value, and in VHF/TV band, the actual frequency division number becomes eight times of programmed value in combination with prescaler TD6134AF, TD7101F and TD7103F.

Note 28: In case of direct dividing mode, P0~P3 port (ϕL11) data becomes unrelated and P4 port becomes LSB.

Note 29: Frequency division number is entirely renewed at the time of data setting of MSB port (ϕL14).

So this prevents wrong influence from giving to the lock up time.

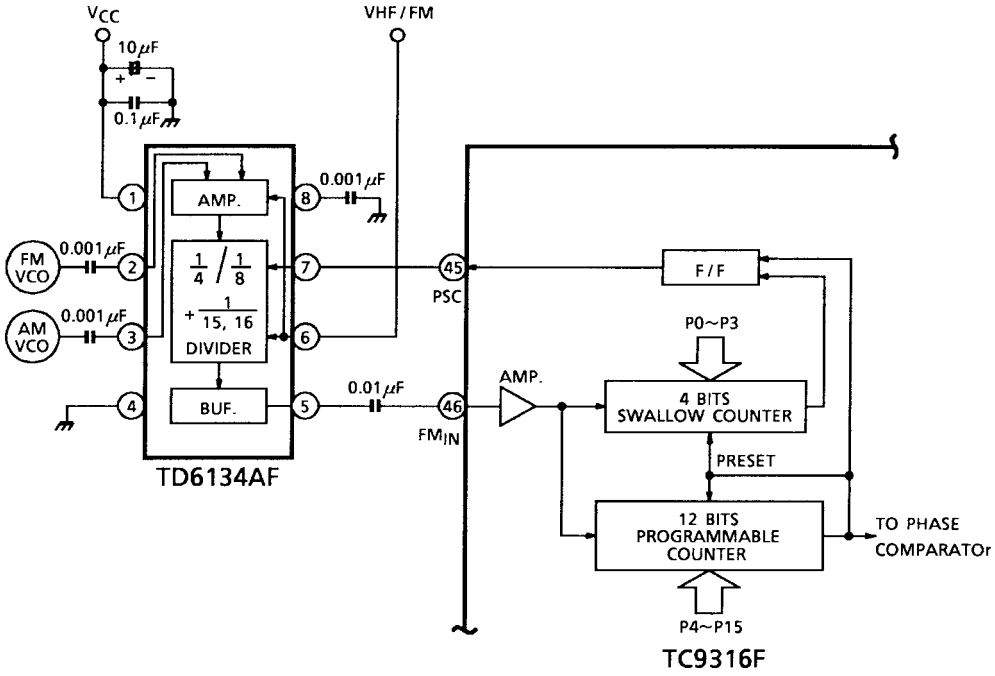
For this reason, the data of MSB port (ϕL14) must be set at the end of division number. Even when the data setting is considered unnecessary (when the data is same as the previous one), the data setting of MSB port (ϕL41) must be executed.

2. Circuit Construction of External Prescaler and Programmable Counter

(1) Circuit construction of pulse swallow dividing mode

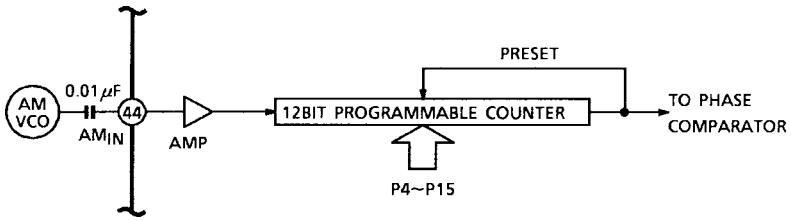
The circuit is composed of (1/4 or 1/8 × 1/15, 1/16) 2-modulous prescaler TD6134AF, TD7101F, TD7103F and swallow counter of 4 bits and binary programmable counter of 12 bits. In the case of FM band, it selects 1/4 divider to the front stage of 2-modulous prescaler, and in VHF/TV band, it selects 1/8 divider to the front stage of 2-modulous prescaler.

The block diagram including prescaler is shown as follows.



(2) Circuit construction of direct dividing mode

In this case, it is unnecessary to use the external prescaler, 12 bits programmable counter is only used.



Note 30: Both FM_{IN} and AM_{IN} have built-in amplifiers, and the small amplitude operation is possible through the capacitor coupling.

Note 31: In TC9316FA, TC9316FB, the pin No. changes as below.

44 → 46

45 → 47

46 → 49

Reference Frequency Divider

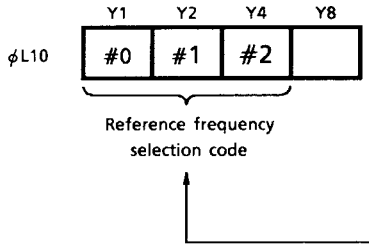
This block divides oscillating frequency of external 75 kHz crystal, and produces seven kinds of PLL reference signal, 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, 25 kHz. Selection of reference signal is carried out with the data of REF select port.

The selected signal is supplied to the phase comparator as the reference frequency.

1. REF Select Port (ϕL10)

This is an internal port to select seven kinds of reference frequency signal.

Normally, this port is made access by PLL instruction designated the operand part [$C_N = 0$] (ϕL10).



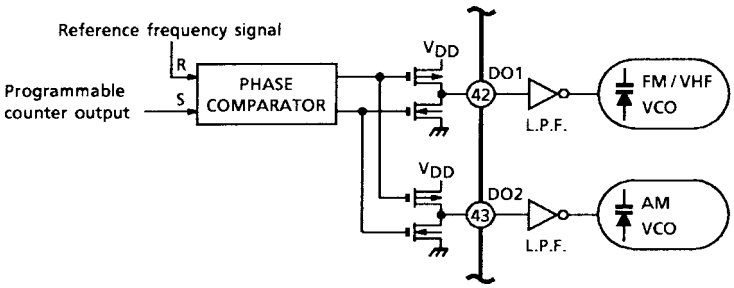
REF. output code table

#2	#1	#0		REFERENCE FREQUENCY
0	0	0	0	1kHz
0	0	1	1	3kHz
0	1	0	2	3.125kHz
0	1	1	3	5kHz
1	0	0	4	6.25kHz
1	0	1	5	12.5kHz
1	1	0	6	25kHz
1	1	1	7	REF. output is stopped

Phase Comparator

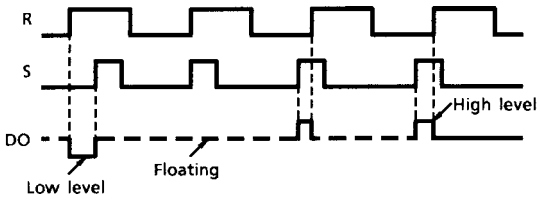
The phase comparator outputs the error amount comparing the phase difference between the reference frequency signal supplied from the reference frequency divider and the programmable counter dividing output. VCO is controlled through low-pass filter so that the frequencies and the phase-difference of these two signals may coincide.

Since two tri-state buffer DO1 and DO2 terminals are parallel output from the phase comparator, the filter constant can be optimumly designed for each band of FM/VHF and AM.

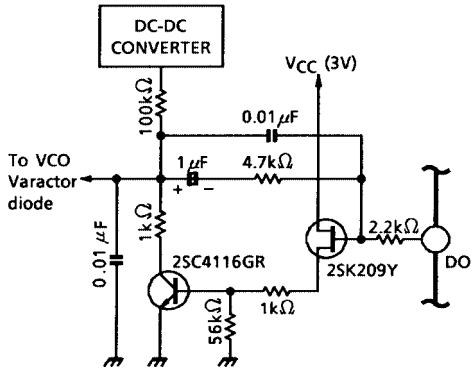


Note 32: In TC9316FA, TC9316FB, the pin No. changes as below.

42 → 44, 43 → 45



DO Output Timing Chart



Example of Active Low-Pass Filter Circuit (for reference)

DO output timing chart and example of active low-pass filter circuit structured by darlington connection of FET and transistor are shown in the above figures.

The filter circuit shown in the above figure is an example for reference, and the actual circuit should be investigated and designed conforming to the system band construction and the required characteristics.

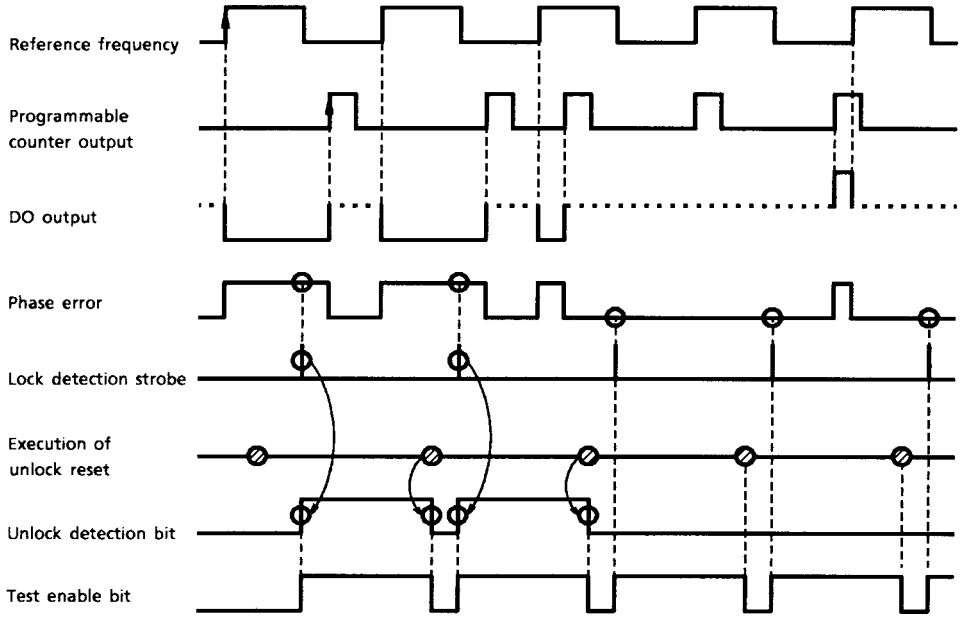
Unlock Detection Bit (ϕLK16)

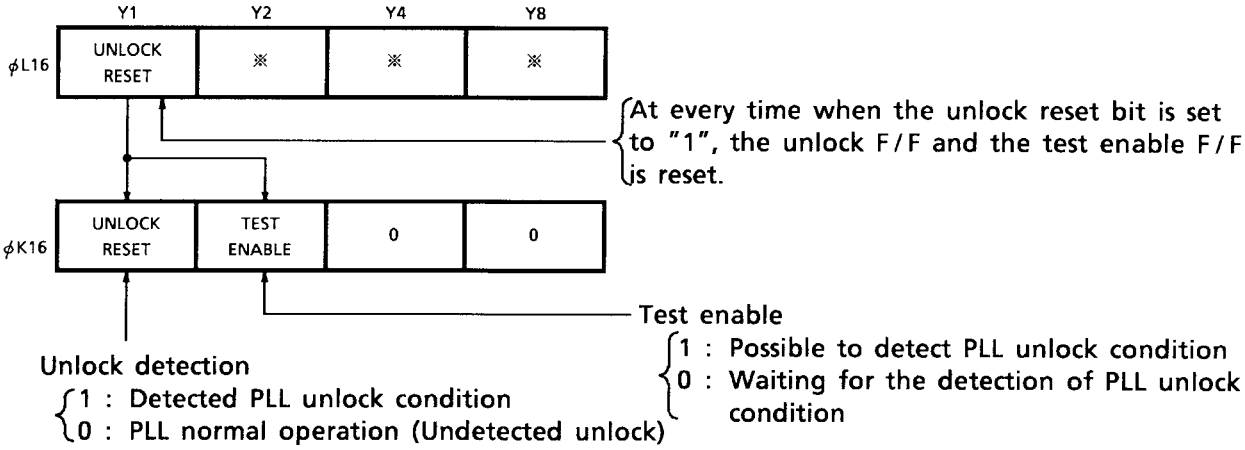
This is the bit for detecting the locked state of PLL system. When PLL system is unlocked state, namely, in the state in which the reference signal and the dividing frequency of programmable counter do not coincide, the pulse is output from the phase comparator to the unlock F/F with the cycle of the reference frequency.

By this pulse, the unlock F/F is set. At every time when the unlock-reset bit is set to "1" by PLL output instruction designated the operand part [$C_N = 6$], the unlock F/F is reset (ϕL16).

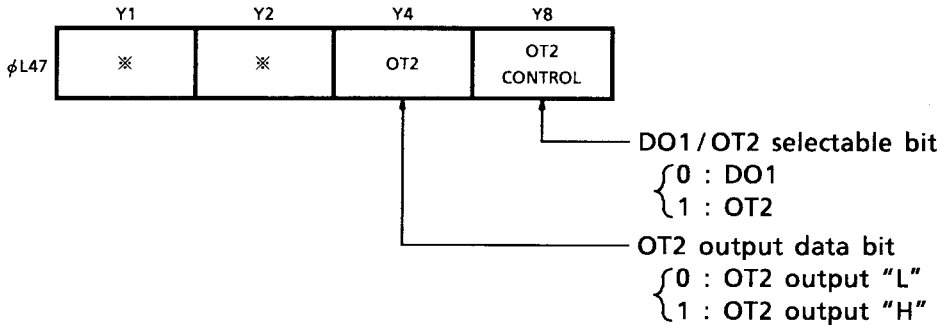
After the unlock F/F is reset, the locked condition can be detected by access the unlock detection bit with PLL input instruction (ϕK16). Since the pulse is input with the cycle of the reference frequency, after the unlock F/F is reset, it is necessary to make access the unlock detection bit after the time exceeding the cycle of the reference frequency. If the time is shorter than the cycle, the correct locked condition can not be detected.

So the test enable F/F is prepared. Every time when the unlock reset bit is set to "1", the test enable F/F is reset and set to "1" with the unlock detection timing. In short, it is able to detect the unlock condition correctly at "1" state of the test enable bit (ϕK16).





DO1 terminal is able to general output (OT2) by setting general output port (φL47).

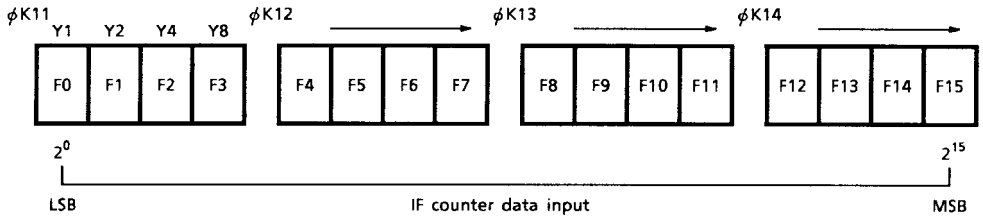


General IF Counter

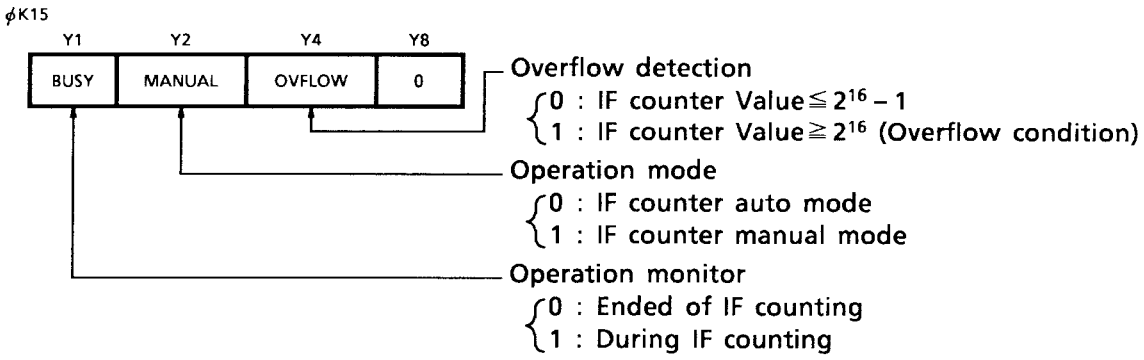
16 bits general IF counter is able to detect the auto-stop signal with counting intermediate frequency (IF) of FM or AM band at auto-tuning mode. The general IF counter is available for auto tuning function of IF counting type easily in combination with TA8132F, a AM/FM IF + MPX IC corresponding to DTS. IF counter block is composed of 16 bits binary counter and the port for IF counter control.

1. IF Counter Data Port (ϕK11~ϕK15)

This is the data input port for input the counted data of IF counter and operating condition. The data is read into data memory by PLL input instruction designated the operand part [C_N = 1~5].



The counted data of IF counter is inputted with binary from the input port, F0~F15.

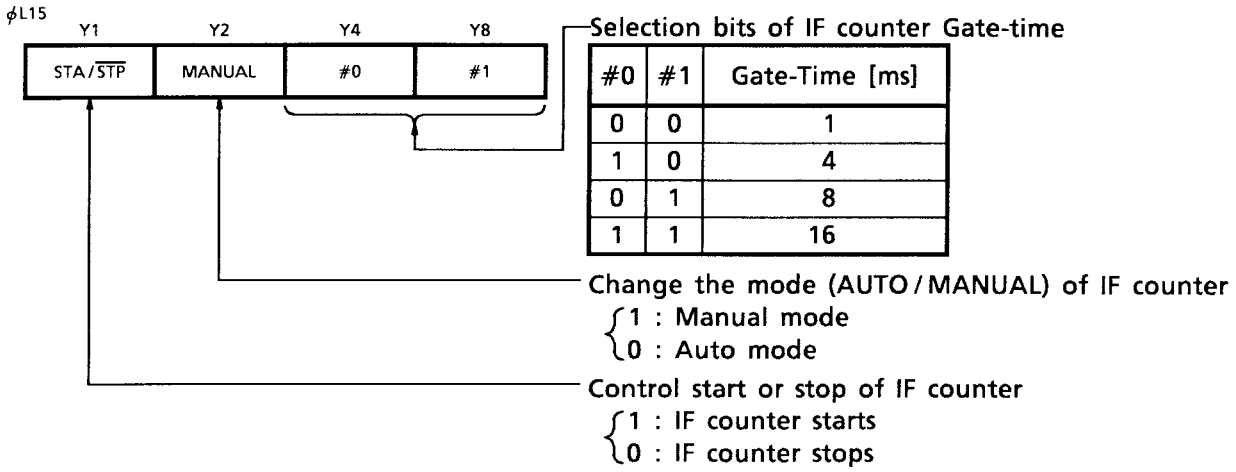


This is the input port for detecting operation condition of IF counter (ϕK15).

In case of using IF counter, the counted data (F0~F15) should be calculated after confirming "0" of BUSY bit (end of IF counting) and OVFLOW bit (not overflow condition).

2. IF Counter Control Port (ϕL15)

This is the data output port controlled for IF counter operation. This port is made access by PLL output instruction designated the operand part [C_N = 5].



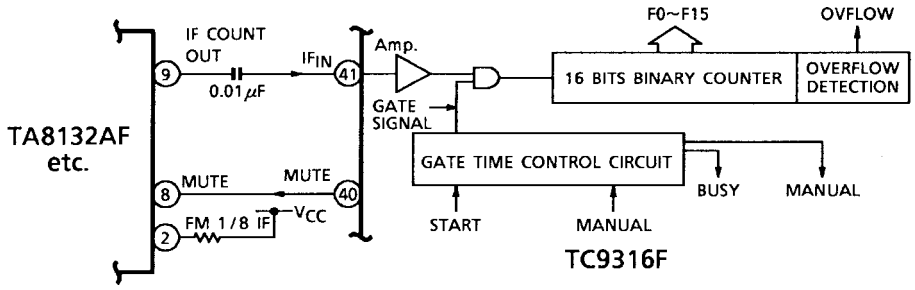
At the auto mode (MANUAL bit is set to "0"), the STA/$\overline{STP}$ bit is set to "1" every time, IF counter starts. IF counter counts during the gate time selected by #0, #1 bits, and it ends automatically.

At manual mode, when the STA/$\overline{STP}$ bit is set to "1", IF counter counts continuously until the STA/$\overline{STP}$ bit is set to "0".

Note 33: At $\overline{INH}$ = "0", IF counter is reset by compulsorily.

3. Circuit Construction of IF Counter

IF counter is composed of input Amp., gate-time control circuit, 16 bits binary counter.



Note 34: In TC9316FA, TC9316FB, pin No. changes as below.

41 → 43, 40 → 42

Note 35: IF_{IN} terminal has built-in amplifier, and the small amplitude operation is possible through the capacitor coupluing.

LCD Driver

The TC9316F/FA/FB contains LCD driver of 1/3 duty and 1/2 bias driving (frame frequency = 104 Hz). Three common terminals (COM1, COM2, COM3) output three potentials of voltage, V_{DD}, V_{EE}, V_{LCD} level respectively with 1/6 phase difference.

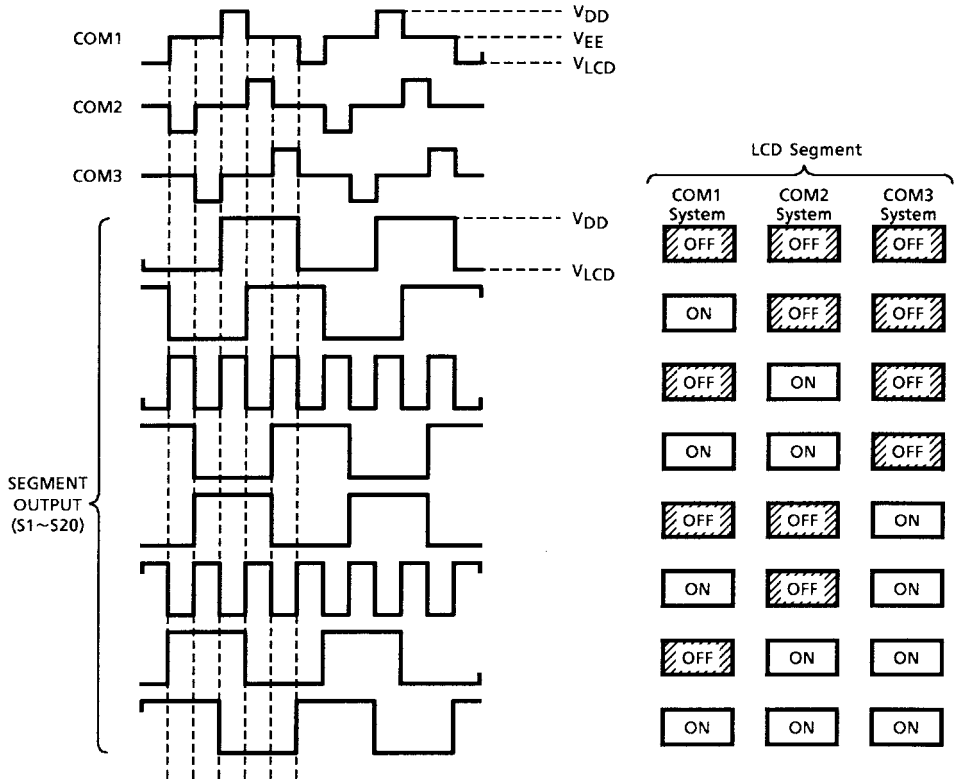
60 segments can be displayed by the combination of these common outputs and 20 segment outputs (S1~S20). That is to say, COM1 system segment COM2 segment system and COM3 system segment can be displayed by one segment output, what is called dynamic display method.

LCD driver does not contain segment decoder, so 60 segments can be freely used by program for 7 segment display or mark segment display.

S1~S16 segment output is controlled by execution of SEG instruction and S17~S20 segment output is by execution of MARK instruction.

1. Timing Chart of LCD Driver

Below are shown the timing chart of COM1~COM3 output wave form and four kinds of segment output wave form.



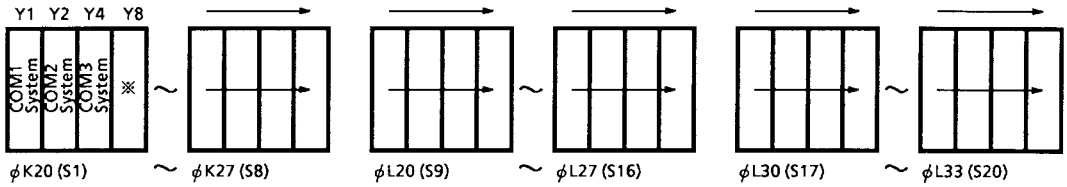
Note 36: During system reset and back up mode (CKSTP instruction executing), common output and segment output are all fiexd at “L” lavel automatically.

2. Segment Port (ϕK20~ϕK27, ϕL20~ϕL27, ϕL30~ϕL33)

This is a port group to output segment data. ϕL20~ϕL27 ports are made access by SEG instruction and corresponded to S1~16.

ϕL30~ϕL33 ports are made access by MARK output instruction and corresponded to S17~S20.

At each port, Y1, Y2 and Y4 are corresponded to COM1, COM2 and COM3 system in order from LSB. MSB (Y8) port don't care. Selected port, designated segment and COM system segment turns "ON" when setted to data "1", COM system segment turns "OFF" when setted to data "0".

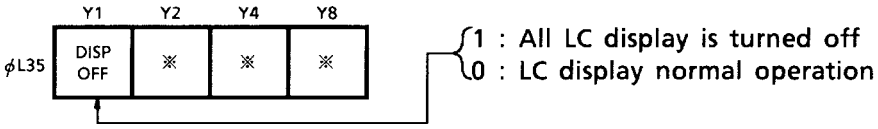


- DISP OFF bit (ϕL35)

  This bit controls turning on or off of LC display. When data "1" is set to this bit, common outputs and segment outputs are all fixed at "L" level, all display becomes turned off. When data "0" is set to this bit, display becomes normal action. And this bit is reset to "0" after system reset.

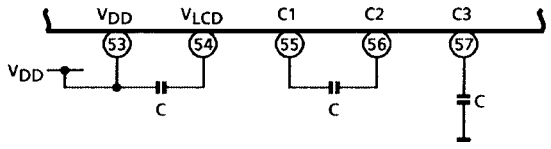
Note 37: The name of segment port corresponds to the name of segment output terminal, respectively. And as the content of each port don't accept DISP OFF bit's influence, even display off made by DISP OFF bit, it is able to output the data to each segment port normally.

Note 38: Decoding of segment can be made by providing the segment decode pattern in the program memory and reading it into the data memory by using DAL instruction. Therefore LCD driver doesn't have built-in segment decoder especially.



3. Voltage Boosting Circuit for LC Display

TC9316F has built-in voltage boosting circuit for LC display, it is able to stabilize LC display driving at the low voltage operation. This circuit is composed with 1.5 V reference voltage circuit (V_{EE}) and voltage double boosting circuit (V_{LCD}), be connected the boosting capacitor as follows.



V_{DD} = 1.8~3.6 V

3.0 V typ.

C = 0.1 μF typ.

Note 39: In TC9316FA, TC9316FB, the pin No. changes as below.

53 → 56, 54 → 57, 55 → 58, 56 → 59, 57 → 60

Input and Output Port

1. I/O Port P1-0~P1-3 (ϕKL41), P2-0~P2-3 (ϕKL42)

I/O port (P1-0~P1-3, P2-0~P2-3) are 4 bits CMOS type, and is capable of making input and output setting with each bit.

Input and output setting of I/O port is made by the content of I/O control internal port.

Setting to input port can be made by setting "0" to the bit of I/O control port corresponding to I/O port, while setting to output port can be made by setting "1" in the same.

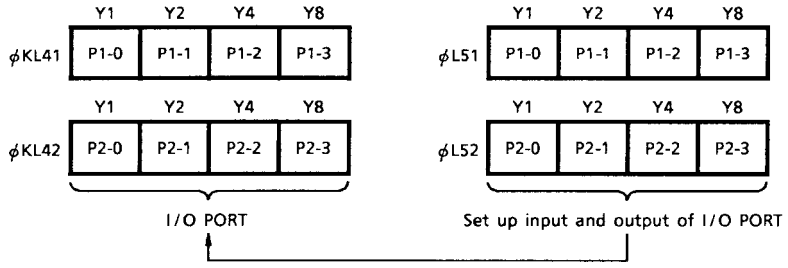
In case of input port setting, the present data input I/O port is read into the data memory by the execution of IO input instruction designated the operand part [C_N = 1, 2] (ϕK41, ϕK42). At this time, input data is set to output latch of I/O port (ϕL41, ϕL42) in the same.

In case of output port setting, output condition of I/O port is controlled execution of IO output instruction designated the operand part [C_N = 1, 2]. And the present output data of I/O port is read into the data memory by the execution of IO input instruction (ϕK41, ϕL42).

Note 40: I/O control port is made access by KEY instruction designated the operand part [C_N = 1, 2]. After system reset, the content of this port is all reset to "0", and I/O port is all set up input mode.

Note 41: During the clock stop mode (executing CKSTP instruction), output condition of I/O port set at output mode is all fixed at "L" level automatically, but each output latch holds on the data just before the clock stop mode.

Note 42: At the time of changing input condition of P1-0~P1-3 port set at input mode, it cancels the execution of WAIT and CKSTP instructions and makes the operation restart. In case of setting "1" to I/O bit of MUTE control port, MUTE port is made to set to "1" compulsorily by the same condition.



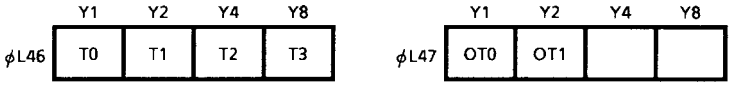
2. General Output Port T0~T3 (ϕL46), OT0, OT1 (ϕL47)

T0~T3 and OT0, OT1 are exclusive output port of 4 bits and 2 bits.

In case of using LCD segment output for key matrix and be short for key functions. It is used as output of key return timing signal for key matrix. So the resister is built-in at N-ch transistor side and sink current is decreased.

Therefore, of using push key, the diode can be omitted on the key matrix. Output port is made access by IO output instruction designated the operated part [C_N = 6, 7] (ϕL46, ϕL47). In case of using for normal output port, take care to make the external circuit because of output impedance of "L" level increased.

Note 43: During the clock stop mode (excusing CKSTP instruction), T0~T3 and OT0, OT1 output is fixed at "L" level automatically, but the content of port is held on the previous data.

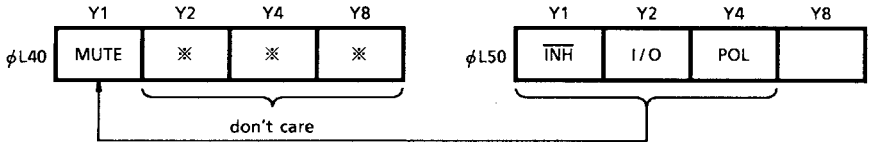


3. MUTE Port (ϕKL40)

This is a 1 bit CMOS type exclusive output for muting control. Normally, it is made access by IO output instruction designated operand part [C_N = 0] (ϕL40).

Further, by the execution of IO input instruction designated operand part [C_N = 0], content of present output data is read into data memory (ϕK40).

And according to the data of MUTE control port (ϕL50), MUTE port is controlled.



- $\overline{INH}$ bit

  In case of setting "1" to this bit, MUTE port is set to "1" compulsorily by changing of $\overline{INH}$ input level ("L" → "H" or "H" → "L").

- I/O bit

  In case of setting "1" to this bit, MUTE port is set to "L" compulsorily by input level changing of I/O port set at input mode.

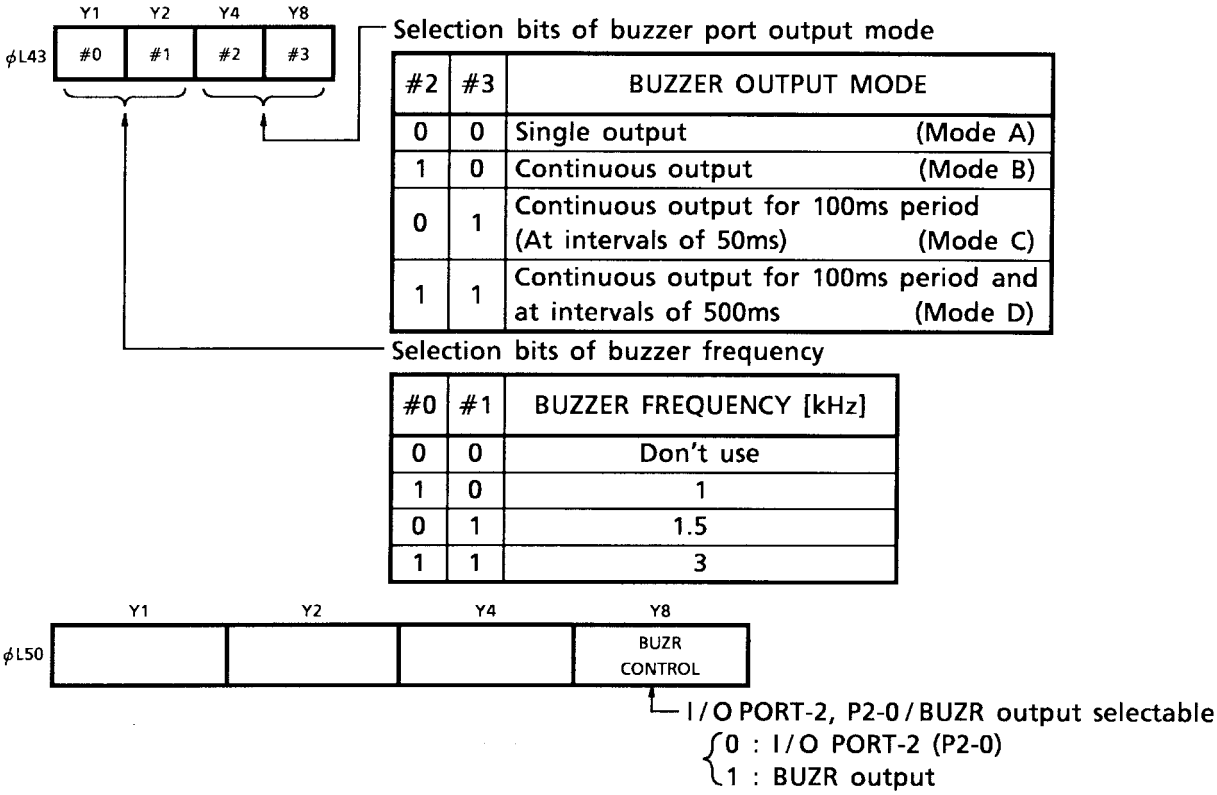
- POL bit

  The bit controls output polarity of MUTE port. In case of setting "0" to this bit, the data of MUTE port is output with positive logic. In case of setting "1" to the bit, the data of MUTE port is output with negative logic.

Note 44: After system reset, the content of $\overline{INH}$, I/O, POL each bit is reset to "0".

Buzzer Port

Buzzer output is available as beep sound for confirmation of key operation, and as alarm sound. It uses as 1 bit general output port. The buzzer output condition is controlled by buzzer control port (ϕL43) as follows. Buzzer control port is made access by IO output instruction designated the operand part [C_N = 3].



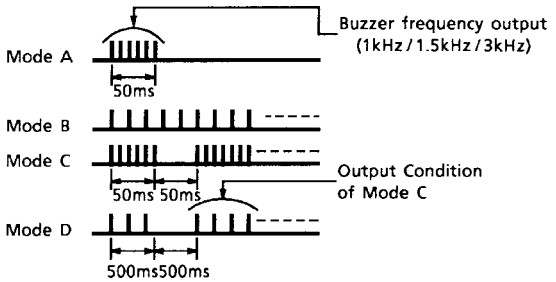
#2	#3	BUZZER OUTPUT MODE
0	0	Single output (Mode A)
1	0	Continuous output (Mode B)
0	1	Continuous output for 100ms period (At intervals of 50ms) (Mode C)
1	1	Continuous output for 100ms period and at intervals of 500ms (Mode D)

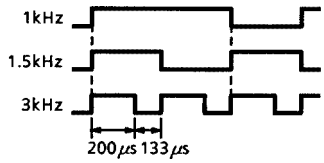
#0	#1	BUZZER FREQUENCY [kHz]
0	0	Don't use
1	0	1
0	1	1.5
1	1	3

It is able to use both as BUZR output and I/O PORT (P2-0).
If BUZR CONTROL bit is setted to "1", the terminal changes from P2-0 output to BUZR output.

Note 45: In case of using as general output port, output is fixed at "L" level by executing CKSTP instruction, but the content of this port is held on.

Below are shown the timing chart of buzzer signal output and buzzer frequency wave form.





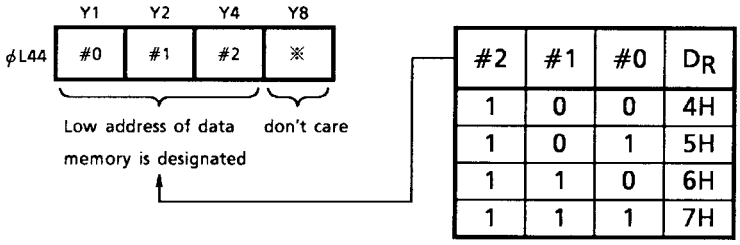
Register Port

G-register and data register stated in the explanation of CPU are also treated as one of internal ports.

1. G-Register (ϕL44)

This is a register to make addressing of low address (D_R = 4H~7H) of data memory during the execution of MVGD instruction and MVGS instruction. This register is made access by IO output instruction designated the operand part [C_N = 4].

Note 46: Content of this register is effective only during the execution of MVGD instruction and MVGS instruction, and gives no effect during the execution of other instructions.



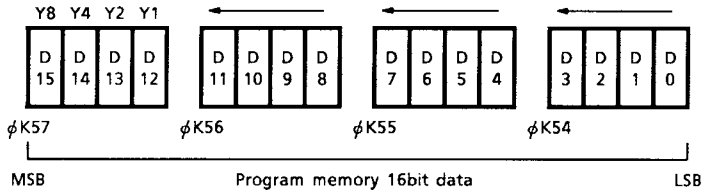
#2	#1	#0	D_R
1	0	0	4H
1	0	1	5H
1	1	0	6H
1	1	1	7H

Note 47: It is possible to indirectly designate all low address of data memory by setting data 0H~7H on G-register. (D_R = 0H~7H)

2. Data Register (ϕK54~ϕK57)

This is 16 bit register on which the data of program memory is loaded by the execution of DAL instruction. Content of this register is read into the data memory in 4 bit unit by the execution of KEY input instruction designated the operand part [C_N = 4~7].

This register is available for the decoding of LCD segment, or for the taking of band edge data of radio and coefficient data during binary to BCD conversion.



Key Input

The three basic key scanning methods are listed below.

(1) The general-purpose output ports (T0~T3, OT0 and OT1) function as the key source and are scanned by software.

(2) The general-purpose output ports (T0~T3, OT0 and OT1) function as the key source and are scanned by hardware.

(3) The LCD segment output (S20/KR0~S13/KR7) functions as the key source and is scanned by hardware.

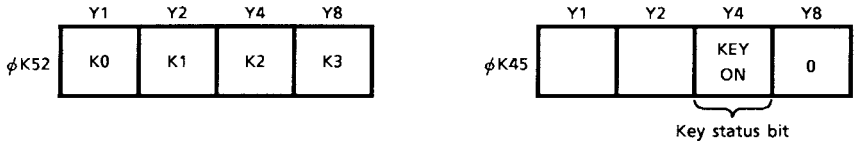
The advantages and disadvantages of these methods are listed below.

	Advantages	Disadvantages
(1)	• Allows rapid key scanning.	• The general-purpose output ports are used for key scanning only. • Configuration of a large number of keys is impossible.
(2)	• Allows configuration of the largest number of keys when the general-purpose output ports are used together with the LCD segment output to construct a key matrix.	• The general-purpose output ports are used for key scanning only. • Slow (could be faster than (3) depending on configuration).
(3)	• The general-purpose output ports need not be used for key scanning. • Allows configuration of a relatively large number of keys.	• Slow.

Four different key matrices can be configured by combining these three methods. Select one which suits your system.

1. Key Input Port (ϕK52)

A 4 bit dedicated input port whose primary use is to scan keys by software scanning. When a key input instruction specifying (CN = 2) as an operand is executed, the key input pin data are loaded to data memory. When this happens, the data set in the key return control port (ϕL53) bits for use in hardware scanning become undefined.



2. Key Status Bit (ϕK45)

The key status bit (“key on”) indicates the present key input status.

When an I/O input instruction specifying (CN = 5) as an operand is executed, the contents of this bit are loaded to data memory.

- Key on bit

  This bit outputs the results of logically OR the data from pins K0~K3.

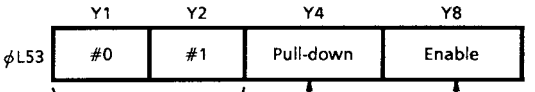
  Pins set for use in hardware scanning by the key return control port (ϕL53), however, are not logically OR.

  This bit can be used to determine whether or not there is any key input.

  When the key on bit is 1 (when high level is input to key input pins K0~K3), execution of the wait instruction is cancelled and operation restarts.

3. Key Return Control Port

This port sets the key input port (K0~K3).



Hardware scan enable bit

1 : Enables output of key return signals from the LCD segment output and the general-purpose output ports (S20 / KR0~S13 / KR7, T0~T3, OT0 and OT1) at the LCD output change timing.

0 : Disables, by hardware, output of key return signals output from the LCD segments and the general-purpose output ports. In this state, all key inputs (K0~K3) remain pulled down, and the #0, #1 and key input pull-down bits are invalid.

Key input pull-down bit

1 : All key inputs (K0~K3) remain pulled down.

0 : Key input corresponding to bits #0 and #1 are used in hardware scanning (dynamically pulled down). All other key inputs remain pulled down. This setting is usually used for hardware scanning.

Key input hardware scan setting bits

The setting of these bits determines which key inputs are used in hardware scanning.

#1	#0	K0	K1	K2	K3
0	0	○	◇	◇	◇
0	1	○	○	◇	◇
1	0	○	○	○	◇
1	1	○	○	○	○

○: Dynamically pulled down at the LCD output change timing and the key input data are input to the key return ports (φK30~φK37). Bits corresponding to the key input port (φK52) become undefined. (hardware scanning)

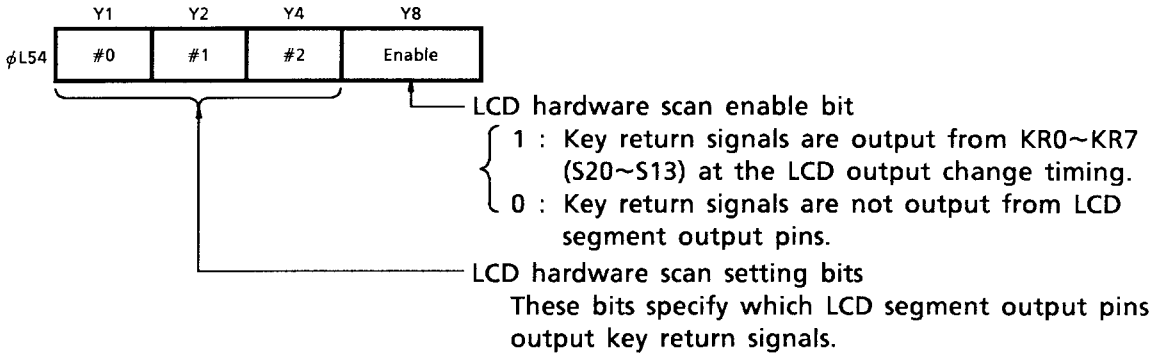
◊: Remain pulled down and data input from the key input port (φK52) are loaded to RAM (software scanning)

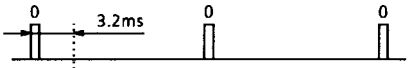
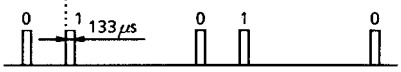
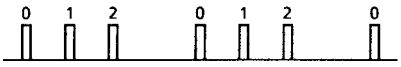
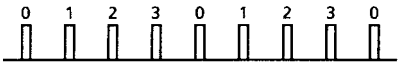
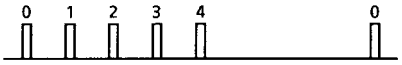
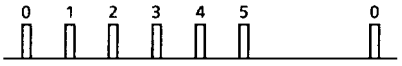
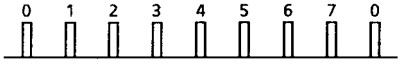
Note 48: During execution of the wait instruction, when high level is applied to key input pins which are continuously pulled down, wait is cancelled. Wait is not cancelled, however, for other pins (pins set for hardware scanning) even when high level is applied.

Note 49: When power is turned on, the hardware scan enable bit is set to 0 and the other bits are set to 1 (hardware scanning disabled).

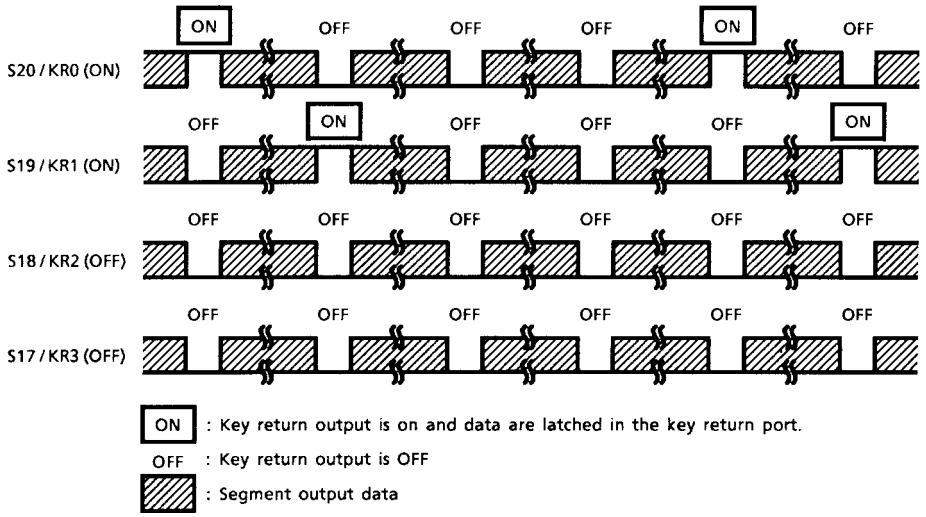
4. LCD Key Return Control Port

This port sets hardware scanning using output from the LCD segments. It determines which LCD segment output pins output key return signals for hardware scanning.



	#2	#1	#0	Key Return Signal Output Pins	Conceptual Diagram of Output Waveforms (numbers signify "n" in "KRn")
0	0	0	0	KR0	
1	0	0	1	KR0, KR1	
2	0	1	0	KR0~KR2	
3	0	1	1	KR0~KR3	
4	1	0	0	KR0~KR4	
5	1	0	1	KR0~KR5	
6	1	1	0	KR0~KR6	
7	1	1	1	KR0~KR7	

Note 50: When bits #0, #1 and #2 are set to 1, 0 and 0, respectively (setting 1), the actual output waveforms are as shown below.



Note 51: When power is turned on, only the LCD hardware scan enable bit is reset to 0.

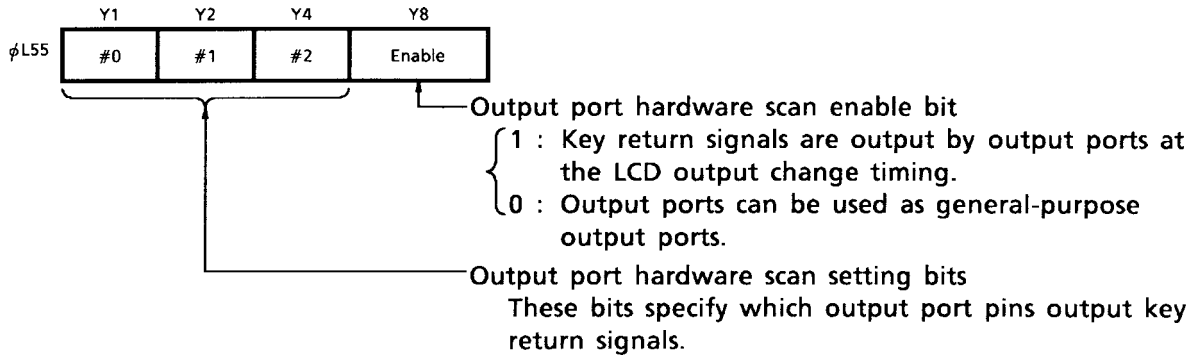
Note 52: When bits #0~#2 are set according to settings 0~3, key scanning is completed in 12.8 ms. When these bits are set according to settings 4~7, key scanning is completed in 25.6 ms.

Note 53: Off waveforms are output by all LCD segment output pins (S13~S20) which are not set for key return output.

Note 54: The key return control port is disabled when the hardware scan enable bit is set to 0.

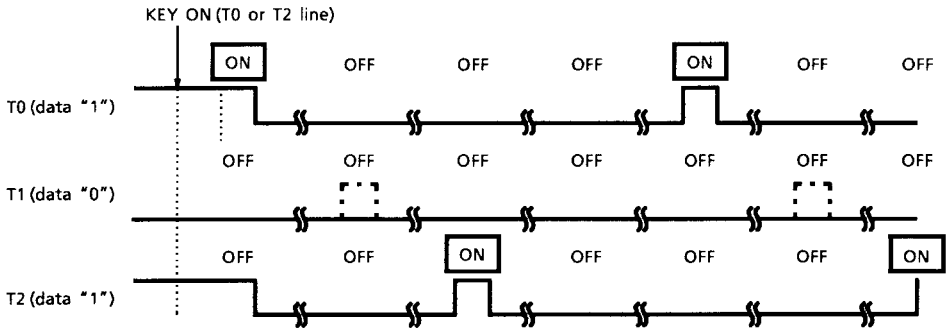
5. Output Port Key Return Control Port

Sets hardware scanning using the output ports. This port determines which output port pins output key return signals for hardware scanning. The output ports are usually used together with the LCD output for hardware scanning when a large number of keys is required.



	#2	#1	#0	Key Return Signal Output Pins	Conceptual Diagram of Output Waveforms
0	0	0	0	T0	
1	0	0	1	T0, T1	
2	0	1	0	T0~T2	
3	0	1	1	T0~T3	
4	1	0	0	T0~T3, OT0	
5	1	0	1	T0~T3, OT0, OT1	
6	1	1	0	Disabled	—
7	1	1	1		

Note 55: When bits #0, #1 and #2 are set to 0, 1 and 0, respectively (setting 2), the actual output waveforms are as shown below.



T3, OT0, OT1 : Output port data are output unchanged.

When the output port hardware scan enable bit is set to 1, the output ports continue to output data unchanged. In this state, if the line key of an output port pin which is outputting 1 is pressed, key scanning begins, key return signals are output according to the timing shown above, and the key data are latched. Only pins which are set to 1 output key return signals. There is no output from pins set to 0 (pin T1 in the above example).

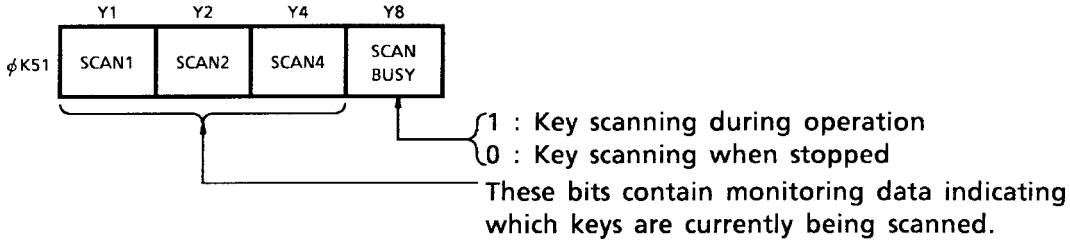
Note 56: When power is turned on, only the output port hardware scan enable bit is reset to 0.

Note 57: When bits #0~#2 are set according to settings 0~3, key scanning is completed in 12.8 ms. When these bits are set according to settings 4 or 5, key scanning is completed in 25.6 ms.

Note 58 This port is enabled only when the key return control port hardware scan enable bit is 1 and the LCD key return control port LCD hardware scan enable bit is 0.

6. Key Return Digit No. Port, SCAN BUSY Bit

The scan busy bit detects whether keys are being scanned by key return output in sync with LCD output.



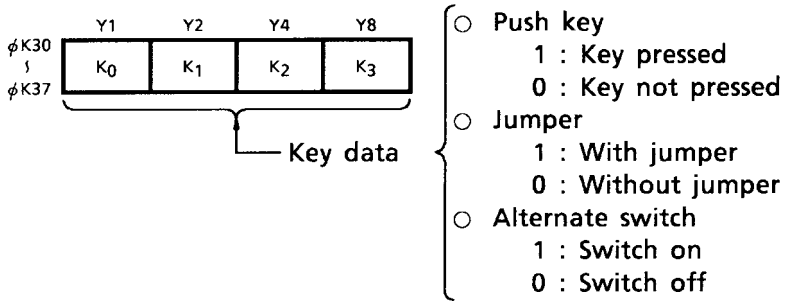
	SCAN4	SCAN2	SCAN1	SCAN Digit Output
0	0	0	0	KR0 or T0
1	0	0	1	KR1 or T1
2	0	1	0	KR2 or T2
3	0	1	1	KR3 or T3
4	1	0	0	KR4 or OT0
5	1	0	1	KR5 or OT1
6	1	1	0	KR6
7	1	1	1	KR7

Note 59: When the output ports are set for key return signal output but no keys are being pressed, the SCAN BUSY bit becomes 0 and the SCAN1~SCAN4 bits all become 1.

Note 60: When the operation is cancelled by clock stop or hard wait, the SCAN1~SCAN4 bits start from 0.

7. Key Return Data Ports

The ϕK30 to ϕ37 ports store the data which result from key scanning by key return output in sync with LCD output.



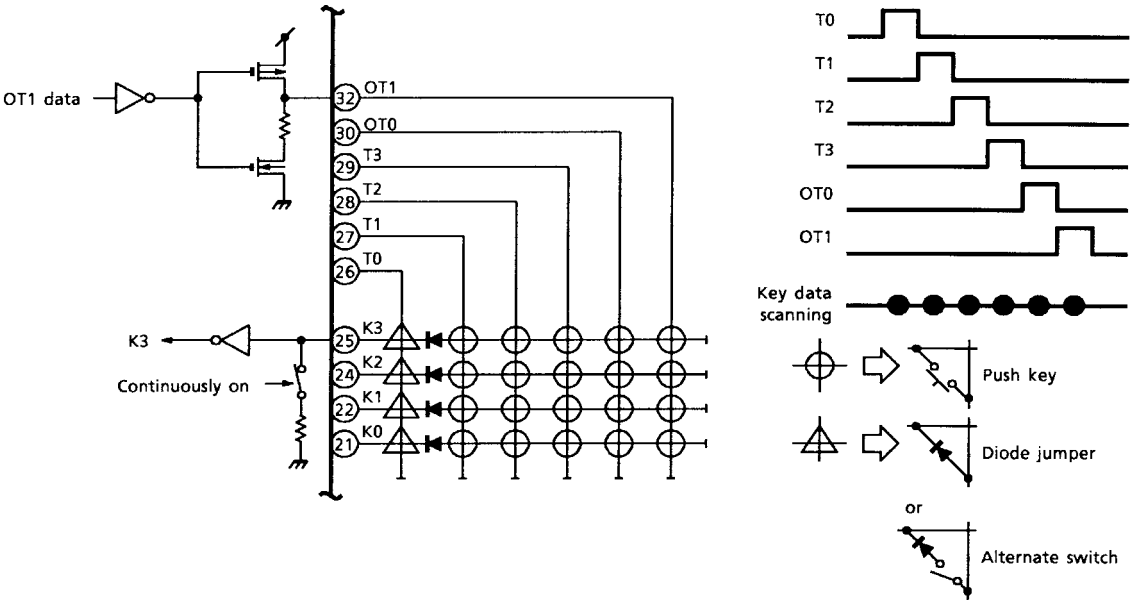
These ports are all set to 0 when the key return control port, the LCD key return control port, and the output port key return control port (ϕL53~ϕL55) are set.

When one cycle of SCAN1~SCAN4 is completed, the data in these ports are loaded to RAM.

8. Key Matrix Configurations

The following four key matrices can be configured.

(1) Key data scanning by software (software scanning)



Note 61: Pin numbers apply to TC9316F.

A key matrix like the one shown above is configured when key data are scanned by software.

This configuration limits key use to 4 × 6 = 24, but it allows fast key data scanning. Since T0~T3, OT0 and OT1 have built-in high resistance in their n-channel FETs, no diodes are needed to prevent reverse current when multiple keys are pressed simultaneously.

With this method, the general-purpose output port data (ϕL46, ϕL47) for the key lines to be scanned are set to high level. The key input port (ϕK52) data are then loaded to memory to determine whether a key is pressed.

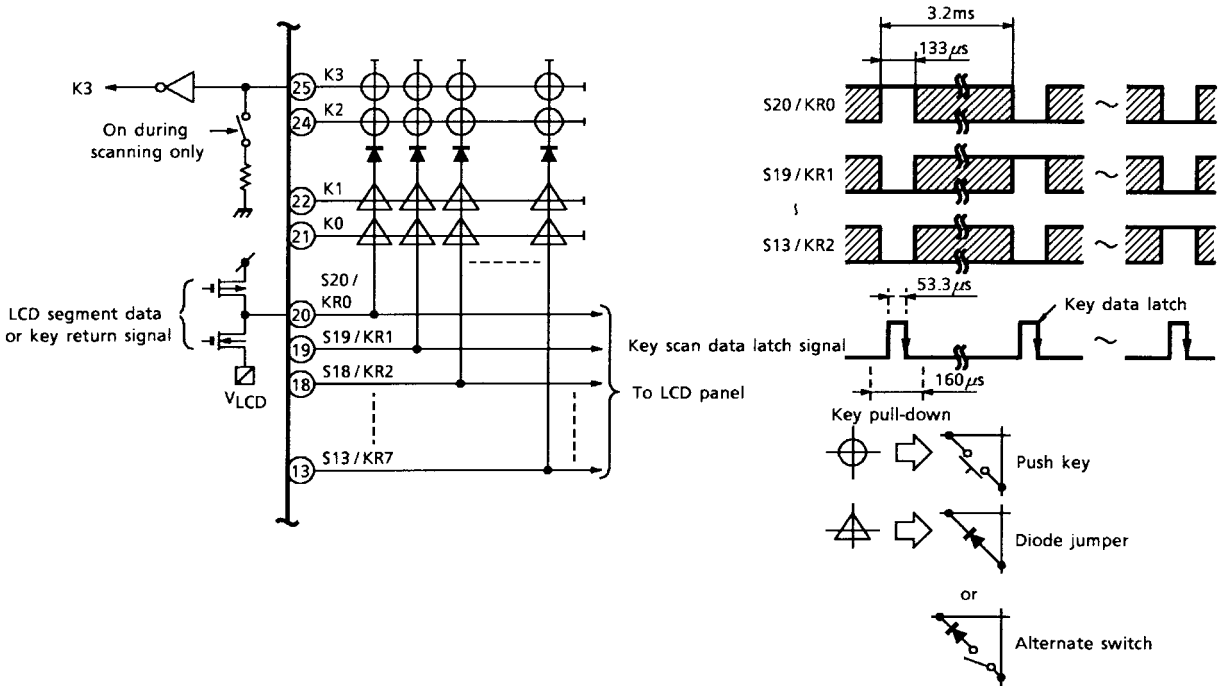
General-purpose output port data which are set to low level are not scanned at this time. When a key is pressed, key input port data = 1 is loaded to data memory; when a key is not pressed, key input port data = 0 is loaded to data memory.

Port Settings for Software Scanning

Port Name	Symbol	Bit (s)	Setting/Use
Hardware Scan Enable Bit	ϕL53	Y8	"0": Disables hardware scanning.
General-Purpose (T0~T3)	ϕL46	Y1~Y8	Sets scanning data
Output Ports (OT0, OT1)	ϕL47	Y1, Y2	(only for ports used in scanning).
Key Input Port (K0~K3)	ϕK52	Y1~Y8	Reads input data.

Note 62: When high level is applied to the key input pins during execution of a wait instruction (ie, during wait mode), wait is cancelled and the CPU is restarted.

(2) Key data scanning by LCD segment output (LCD hardware scanning)



Note 63: Pin numbers apply to TC9316F.

A key matrix like the one shown above is configured when key data are loaded according to the LCD segment output. This key matrix requires diodes to prevent reverse current so be sure these diodes and the diode jumpers are connected pointing in the right direction.

This configuration is used when the general-purpose ports are otherwise employed and are therefore not available for key data scanning and when fast key data scanning is unnecessary. This configuration features a maximum of $4 \times 8 = 32$ keys.

With this method, the key data are scanned at the LCD output change timing. Normally, V_{DD} potential and the V_{LCD} ($V_{DD} - 3$ V) potential are updated and output every 3.2 ms from the LCD segment output in accordance with the segment setting. At the output change timing, the segment signal used to load the key data is set to V_{DD} potential (active), thus pulling the key input pin down to GND. If a key is pressed (or if a diode jumper is connected) at this time, voltage for one diode (V_{DD} – about 0.6 V) is input from V_{DD} potential to the key input pin. If a key is not pressed (or if a diode jumper is not connected), GND potential is input to the key input pins. The potential input is latched in the key return data ports (ϕK30~ϕK37) corresponding to the active LCD segment output lines. At this time, data = 1 when keys are pressed and 0 when not pressed.

Port Settings for LCD Hardware Scanning

Port Name	Symbol	Bits	Setting/Use
Key Return Control	ϕL53	Y1~Y8	LSB (Note 64) "1101" Enables hardware scanning. Specifies dynamic pull-down; K0~K3 all used for hardware scanning.
LCD Key Return Control	ϕL54	Y1~Y8	LSB "×××1" Enables LCD hardware scanning. Y1, Y2 and Y4 bit settings specify which LCD segment output is used for hardware scanning.
LCD Segment Output (S20/KR0~S13/KR7)	—	—	Outputs key return signals.
Key Return Data	ϕK30~ϕK37	Y1~Y8	Latches key data.

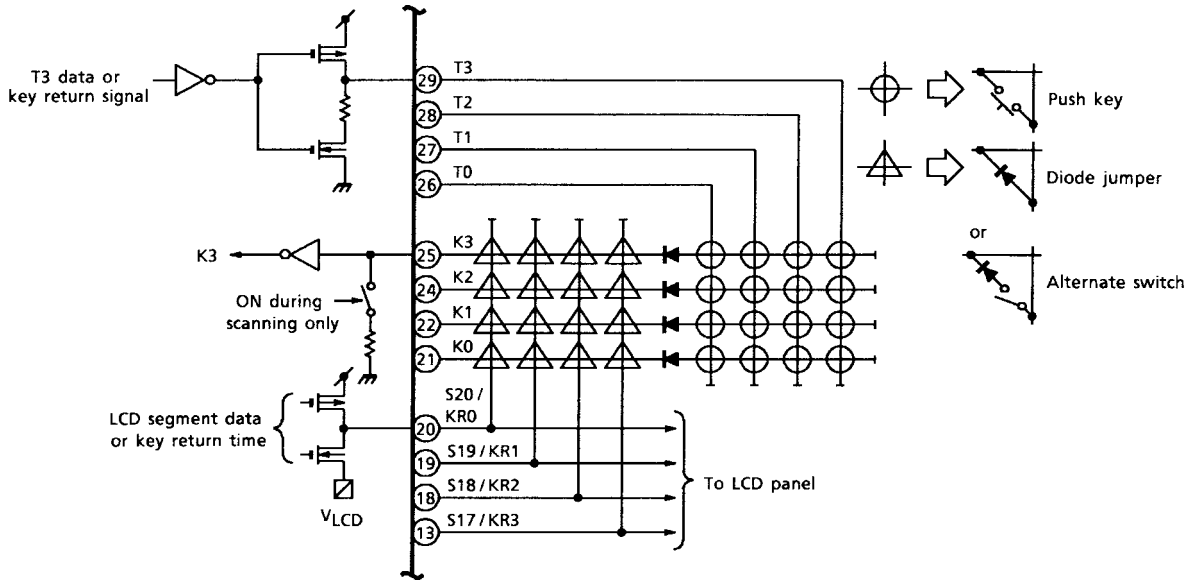
Note 64: The number of key input pins used for LCD hardware scanning can be switched arbitrarily by setting other data in Y1 and Y2. (except K0, which must always be hardware scanned).

Note 65: Since hardware scanning is not synchronous with CPU operation, check the key return digit number port and scan busy bit (ϕL51) to determine the status of key data scanning.

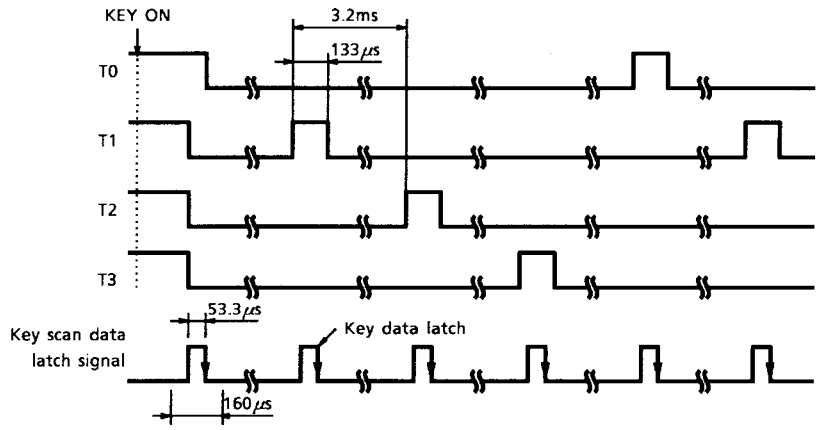
Note 66: Since key data are stored in port latches, the data can be used without first loading them to data memory if necessary, by referencing the ports where the data are stored.

Note 67: Key data are stored in port latches. Thus, key data can be used without loading them to memory just by referencing the ports where key data are stored as necessary. Of LCD segment output S1~S20, only S13~S20 can be used in LCD hard ware scanning.

(3) Key data scanning by LCD segment output and general-purpose output ports (1) (LCD/output port hardware scanning)



Note 68: Pin numbers apply to TC9316F.



The LCD side output waveforms are the same as those in section 8-(2), LCD hardware scanning.

There are two ways to scan key data by the LCD segment output and general-purpose output ports. One is to construct a key matrix like the one shown above, the other is to construct a key matrix as described in the following section.

The key matrix shown above uses time division switching to utilize both the LCD segment output and general-purpose output ports for key data scanning by hardware scanning. In the above key matrix, key data are loaded using hardware scanning by switching the scanning of LCD segment output and general-purpose port by time division.

This method is used when many keys are required or when LCD hardware scanning alone is too slow. This configuration features a maximum of 4 × 14 = 56 keys. It usually features jumpers or alternate switches on the LCD side and push keys on the output port side.

When the jumpers are scanned by the initialization routine, they rarely need to be re-scanned by the main routine, too. Here, they are scanned by initialization routine LCD hardware scanning.

The main routine switches the system to output port hardware scanning, and the push-key data are scanned. If there are fewer than 16 push keys, that is, the same number as in the example in section 8-(2) (OT0 and OT1 are not used), one cycle of hardware scanning takes 12.8 ms. This is half the time required (25.6 ms) for LCD hardware scanning alone.

For a description of LCD hardware scanning, see 8-2 below.

As with LCD hardware scanning, the key data are scanned at the LCD output change timing when the general-purpose output ports are used for hardware scanning. If the general-purpose output port data (ϕL46 and ϕL47) used for hardware scanning are set to high level, scanning begins when a key is pressed. While the key is being pressed, T0 outputs a sequence of V_{DD} potential (active) in sync with the 3.2 ms LCD output change timing. At the same time, the key input pin is pulled down to GND. When a key is pressed at this time, voltage for one diode (V_{DD} minus approx. 0.6 V) is input from V_{DD} potential to the key input pin. When a key is not pressed, GND potential is input to the key input pin.

The input potential is latched in the key return data ports (ϕK30~ϕK37) corresponding to the active general-purpose output port lines.

At this time, data = 1 when a key is pressed; 0 when a key is not pressed.

When the key is released, key scanning stops after completion of the scan operation currently underway. The general-purpose output ports used for hardware scanning revert to high level.

Port Settings for LCD/Output Port Hardware Scanning

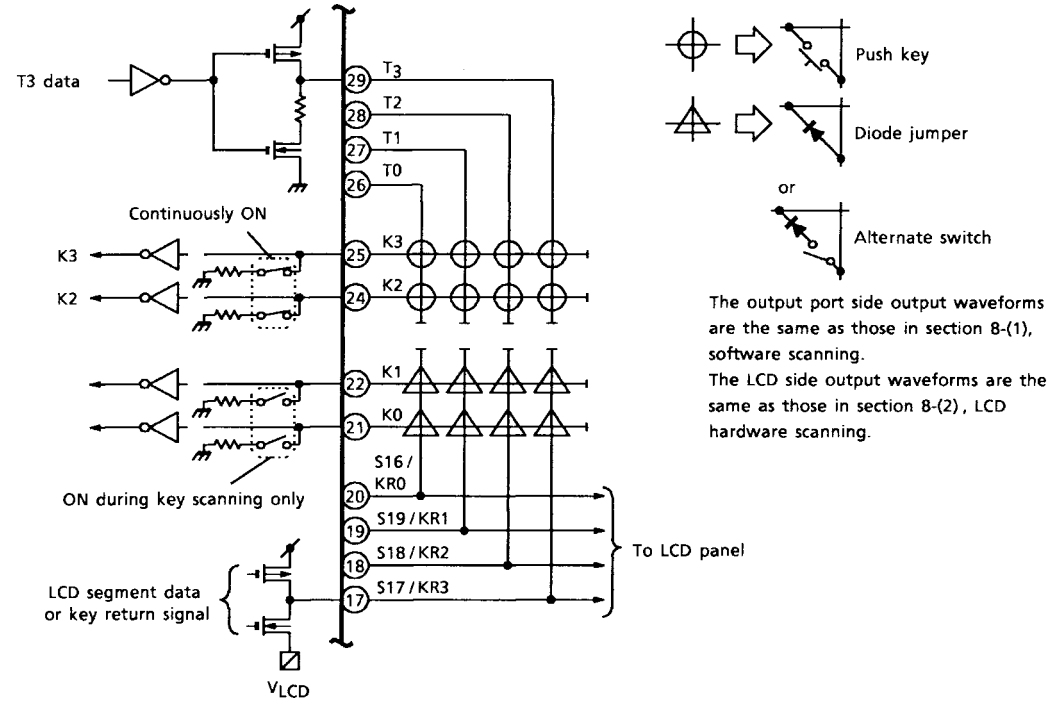
Port Name	Symbol	Bits	Setting/Use
Key return control	ϕL53	Y1~Y8	LSB (Note 69) "1101" Enables hardware scanning. Specifies dynamic pull-down; K0 to K3 all used for hardware scanning.
LCD key return control	ϕL54	Y1~Y8	LSB "×××1/0" Y8: 1 during LCD hardware scanning Y8: 0 during output port hardware scanning Y1, Y2 and Y4 bit settings specify which LCD segment output is used for hardware scanning.
Output port key return control	ϕK55	Y1~Y8	LSB "×××1" Enables output port hardware scanning. Y1, Y2 and Y4 bit settings specify which general- purpose output port pins are used for hardware scanning.
LCD segment output (S20/KR0~S13/KR7)	—	—	Outputs key return signal.
General-purpose (T0~T3) output ports (OT0, OT1)	ϕL46 ϕL47	Y1~Y8 Y1, Y2	Output port pins used for hardware scanning output key return signals when they are set to 1.
Key return data	ϕK30~ϕK37	Y1~Y8	Latches key data.

Note 69: The number of key input pins used for LCD hardware scanning can be switched arbitrarily by setting other data in Y1 and Y2. (except K0, which must always be hardware scanned).

Note 70: Since hardware scanning is not synchronous with CPU operation, check the key return digit number port and SCAN BUSY bit (ϕL51) to determine the status of key data scanning.

Note 71: Key data are stored in port latches. Thus, key data can be used without loading them to memory just by referencing the ports where key data are stored as necessary.

(4) Key data scanning by LCD segment output port and general-purpose output ports (2) (software + LCD hardware scanning)



Note 72: Pin numbers apply to TC9316F

This is the second kind of key matrix which can be used to scan key data by the LCD segment output and general- purpose output ports. The key matrix is configured as shown above.

This configuration uses software scanning on the output port side and hardware scanning on the LCD side. Key data can be scanned simultaneously by both sides since dedicated key input pins are assigned to each side. As the above configuration shows, two key input pins each are assigned to the output port side and the LCD side. This allows a maximum of $2 \times 6 + 2 \times 8 = 28$ keys. This configuration is used when fast key data scanning is required; also, when jumpers are required.

For a description of software scanning, see section 8-(1); for LCD hardware scanning, see section 8-(2).

Port Settings for Software + LCD Hardware Scanning

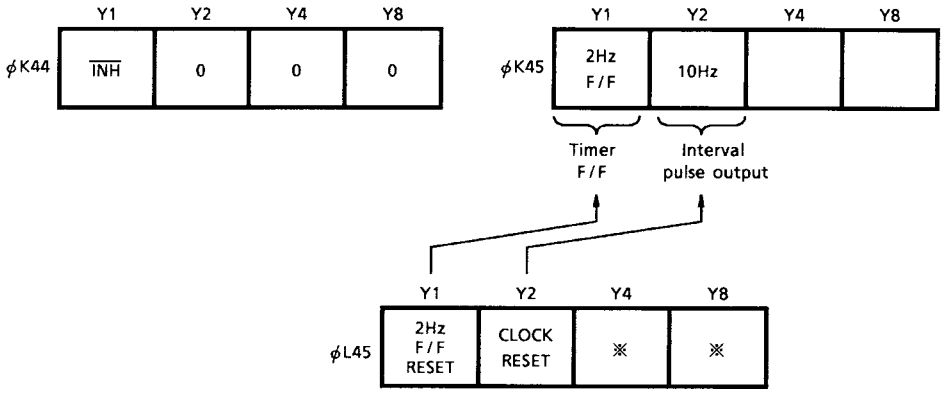
Port Name	Symbol	Bits	Setting/Use
Key Return Control	ϕL53	Y1~Y8	LSB "××01" } Enables hardware scanning. Specifies dynamic pull-down. Y1 and Y2 bit settings specify which key input pins are used for hardware scanning..
LCD Key Return Control	ϕL54	Y1~Y8	LSB "×××1" } Enables LCD hardware scanning. Y1, Y2 and Y4 bit settings specify which LCD segment output is used for hardware scanning.
LCD Segment Output (S20/KR0~S13/KR7)	—	—	Outputs key return signal (LCD side).
Key Return Data	ϕK30~ϕK37	Y1~?	Latches key data (LCD side).
General-Purpose Output Ports (T0~T3)	ϕL46 ϕL47	Y1~Y8 Y1, Y2	} Sets scanning data (only sets ports used for scanning on output port side)
Key Input Port (?~K3)	ϕL52	?~Y8	Reads input data (output port side).

Note 73: Since hardware scanning is not synchronous with CPU operation, check the key return digit number port and SCAN BUSY bit (ϕL51) to determine the status of key data scanning.

Note 74: When high level is applied to the key input pins assigned to the output port side (software scanning) during execution of a wait instruction, wait is cancelled and the CPU is restarted.

Internal Control Port

Internal control port is used for reading into data memory the inside condition of device which must be known in the execution of program, or for resetting the inside condition of device.



1. $\overline{INH}$ Input Port (ϕK44)

This is an input port for inputting the data of $\overline{INH}$ input terminal. Content of this port is read into the data memory by IO instruction designated the operand part [C_N = 4]. Data "1" and "0" represent radio "ON" mode and "OFF" mode, respectively.

At radio off mode, it stops operating of PLL and IF counter block. When $\overline{INH}$ bit of MUTE control port is "1", MUTE port is set to "1" compulsorily by changing the data of $\overline{INH}$ input port. At $\overline{INH}$ input port is "1", it releases execution of CKSTP instruction and the operation is removed. By changing the condition of $\overline{INH}$ input port, execution of WAIT instruction is released.

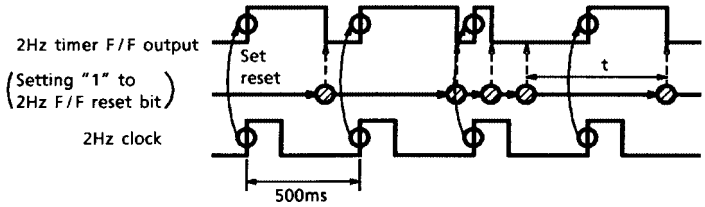
2. 2 Hz Timer F/F (ϕK45)

2 Hz timer F/F is set by 2 Hz (500 ms) signal. With the execution of IO output instruction designated the operand part [C_N = 5] this timer is reset by setting data "1" to 2 Hz F/F RESET bit. This F/F output is read into the data memory by execution of IO input instruction designated the operand part [C_N = 5].

As 2 Hz timer F/F is automatically set every 500 ms, it is usually available for counting of clock.

Since 2 Hz timer F/F is reset only by 2 Hz F/F RESET bit, count error takes place unless data "1" is set to 2 Hz F/F RESET bit within 500 ms period, and correct times is not obtainable.

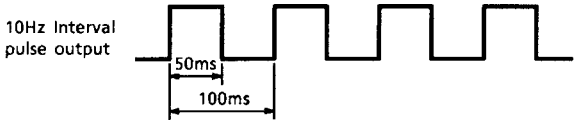
Note 75: Condition of 2 Hz timer F/F output becomes "0" at power on reset or after execution of CKSTP instruction.



t < 500 ms

3. 10 Hz Interval Pulse (ϕK45)

10 Hz interval pulse is output to 10 Hz bit with 100 ms period, duty 50% pulse. This is read into the data memory by the execution of IO input instruction designated the operand part [C_N = 5]. This output has no flip flop and is available for mute time counting etc.



4. Other Control Bit (ϕL45)

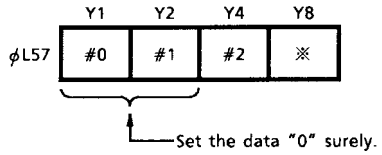
- Clock reset bit

  Every time data "1" is set to this bit, clock of under 50 Hz is reset (10 Hz interval pulse is also reset). This bit is used for adjusting time of clock.

  Accuracy of clock at this time is –0, +0.02 second.

5. TEST Port (ϕL57)

This is an internal port for testing function of device. It is made access by KEY output instruction designated the operand part [C_N = 7]. Never fail to set data "0" in ordinary program.

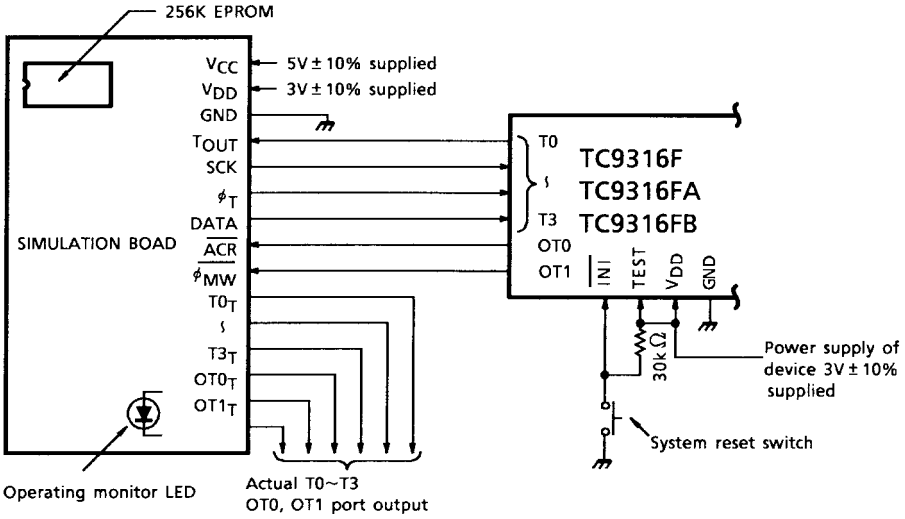


Application to Evaluator Chip

When "H" level is supplied to TEST terminal (test mode), device operates as evaluator chip, and functional evaluation of developing program can be made by utilizing external simulation board and EPROM. In the test mode, the device operates with the program written in EPROM, irrespective of the content of program memory in the device.

As key timing output port (T0~T3) and output port (OT0, OT1) are transferred to the input and output terminal for control of simulation board at this time, actual T0~T3 and OT0, OT1 port signal are output from the simulation board side.

Below is shown connection diagram of the device and simulation board in case that it is used as evaluator chip.



Note 76: Supply 3 V ± 10% voltage to the device and 5 V ± 10% voltage to the simulation board even during back-up mode.

Note 77: Each terminal of the device except that shown above can be used normally.

Note 78: In case of back-up mode (execution of CKSTP instruction), operating monitor LED on the simulation board turns off.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~4.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10~60	°C
Storage temperature	T_{stg}	−55~125	°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = 3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD}	—	—	1.8	3.0	3.6	V
Memory holding voltage range	V_{HD}	—	Crystal oscillation stops (excuting CKSTP Instruction) (Note 79)	1.2	—	3.6	V
Operating power supply current	I_{DD1}	—	Normal operation, output No-load	—	0.7	2.0	mA
	I_{DD2}	—	At only CPU operation (radio off, lighting display)	—	60	150	μA
	I_{DD3}	—	At stand-by mode (radio off, only crystal oscillation)	—	50	100	
Memory holding power supply current	I_{HD}	—	Crystal oscillation stop (excuting CKSTP instruction)	—	0.1	1.0	μA
Crystal oscillation frequency	f_{XT}	—	(Note 79)	—	75	—	kHz
Crystal oscillation starting time	t_{ST}	—	Crystal oscillation = 75 kHz	—	—	1.0	s

Note 79: Marked items are guaranteed by all conditions of V_{DD} = 1.8~3.6 V, Ta = −10~60°C

Voltage Double Boosting Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Voltage double reference voltage	V_{EE}	—	V_{DD} Reference (C3)	−1.2	−1.5	−1.8	V
Voltage double boosting voltage	V_{LCD}	—	V_{DD} Reference (V_{LCD})	−2.4	−3.0	−3.6	V
V_{LCD} pull-down resistance	R_{IN3}	—	(V_{LCD})	0.75	1.5	3.0	MΩ

Programmable Counter, IF Counter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating frequency range	f_{IN1}	—	V_{IN} = 0.3 V_{p-p} (FM_{IN}, AM_{IN}) (Note 79)	0.2	—	5.0	MHz
	f_{IN2}	—	V_{IN} = 0.3 V_{p-p} (IF_{IN}) (Note 79)	0.35	—	12.0	
Operating input amplitude range	V_{IN1}	—	f_{IN} = 0.2~5.0 MHz (FM_{IN}, AM_{IN}) (Note 79)	0.3	—	V_{DD} − 0.3	V_{p-p}
	V_{IN2}	—	f_{IN} = 0.35~12.0 MHz (IF_{IN}) (Note 79)	0.3	—	V_{DD} − 0.3	

Note 79: Marked items are guaranteed by all conditions of V_{DD} = 1.8~3.6 V, Ta = −10~60°C

Programmable Counter, IF Counter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN}-PSC transfer delay time	tpd	—	V_{IN} = 0.3 V_{p-p}, C = 15 pF (FM_{IN}) (Note 79)	—	—	200	ns
PSC maximum load capacity	C_L	—	(PSC) (Note 79)	—	—	15	pF

Note 79: Marked items are guaranteed by all conditions of V_{DD} = 1.8~3.6 V, Ta = −10~60°C

LCD Common Output (COM1~COM3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{LCD} = 0 V, V_{OH} = 2.7 V	−100	−200	—	μA
	"L" level	I_{OL1}	—	V_{LCD} = 0 V, V_{OL} = 0.3 V	100	200	—	

LCD Segment Output (S1~S20)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH2}	—	V_{LCD} = 0 V, V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL2}	—	V_{LCD} = 0 V, V_{OL} = 0.3 V	50	100	—	μA

Key Return Output Port, General Purpose Output Port (T0~T3, OT0~OT1)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
"H" level output current	I_{OH3}	—	V_{OH} = 2.7 V (T0~T3)	−0.5	−1.0	—	mA
N-ch FET side load resistance	R_{ON}	—	V_{OL} = 3.0 V (T0~T3)	75	150	300	MΩ

Mute, Psc Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH4}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL4}	—	V_{OL} = 0.3 V	300	600	—	

DO1/OT2, DO2 Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH4}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL4}	—	V_{OL} = 0.3 V	300	600	—	
Output off-leakage current		I_{TL}	—	V_{TLH} = 3.0 V, V_{TLL} = 0 V	—	—	±100	nA

General Purpose I/O Port (P1-0~P1-3, P2-0~P2-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH4}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL4}	—	V_{OL} = 0.3 V	300	600	—	
Input leakage current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH1}	—	—	2.4	—	3.0	V
	"L" level	V_{IL1}	—	—	0	—	0.6	

$\overline{INI}$ Input, IF_{IN}/IN Port (when using in port)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH2}	—	($\overline{INI}$, IN0~IN3)	2.4	—	3.0	V
	"L" level	V_{IL2}	—	($\overline{INI}$, IN0~IN3)	0	—	0.6	

Key Input Port (K0~K3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance		R_{IN1}	—	—	75	150	300	kΩ
Input voltage	"H" level	V_{IH2}	—	—	1.8	—	3.0	V
	"L" level	V_{IL2}	—	—	0	—	0.3	

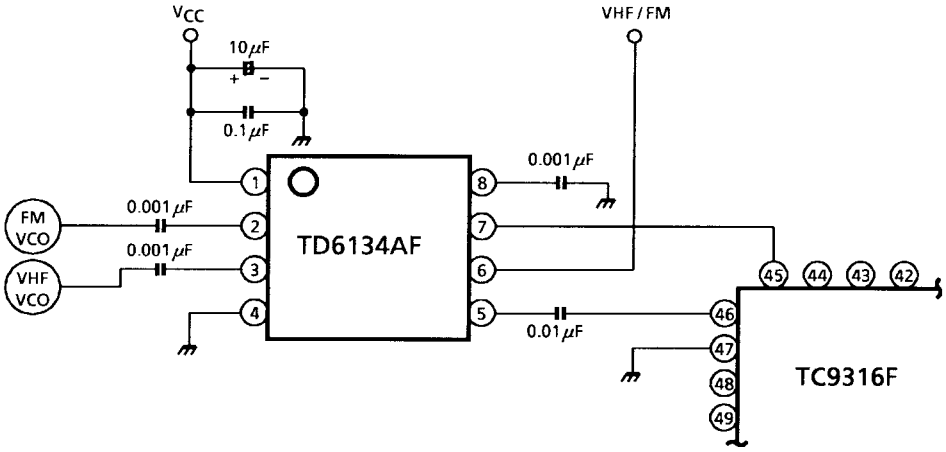
$\overline{INH}$ Input Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH3}	—	—	2.6	—	3.0	V
	"L" level	V_{IL3}	—	—	0	—	1.2	

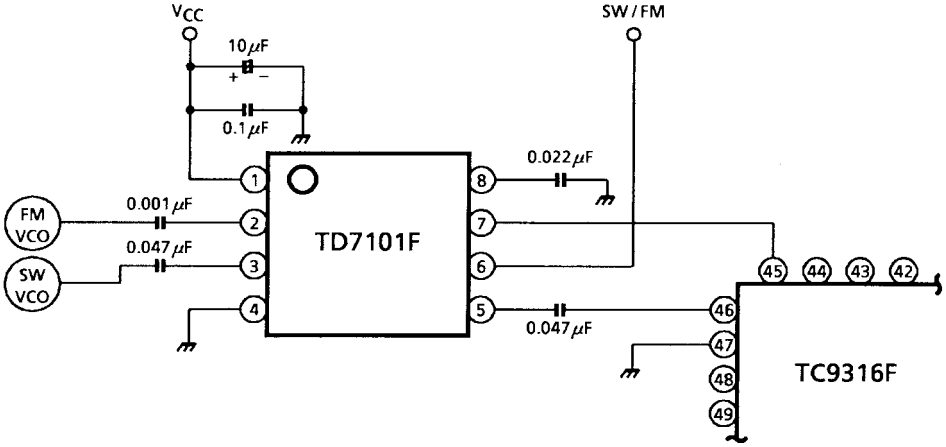
Other

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	R_{IN2}	—	(TEST)	25	50	100	kΩ
X_T input feedback resistance	R_{fXT}	—	(X_T~ $\overline{X_T}$)	3.75	7.5	15.0	MΩ
$\overline{X_T}$ output resistance	R_{OUT}	—	($\overline{X_T}$)	50	100	200	kΩ
Input pull-down resistance	R_{fIN}	—	(FM_{IN}, AM_{IN}, IF_{IN})	375	750	1500	kΩ

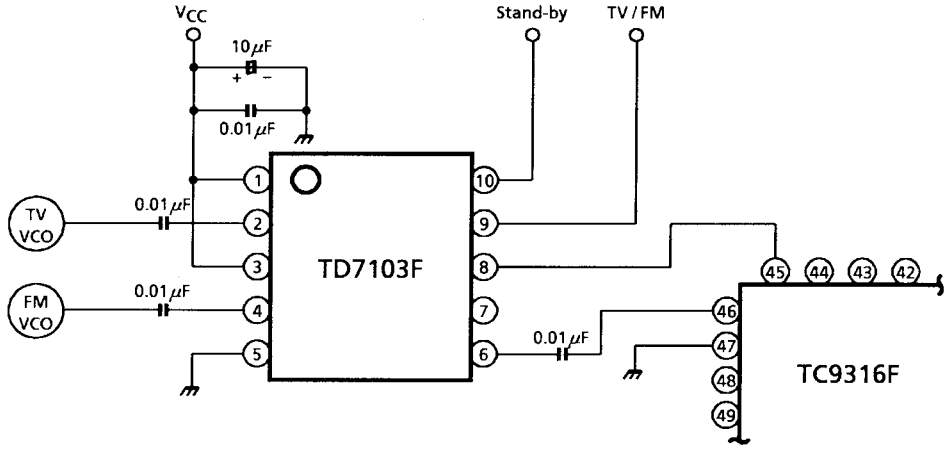
Example of Connection to Prescaler TD6134AF



Example of Connection to Prescaler TD7107F



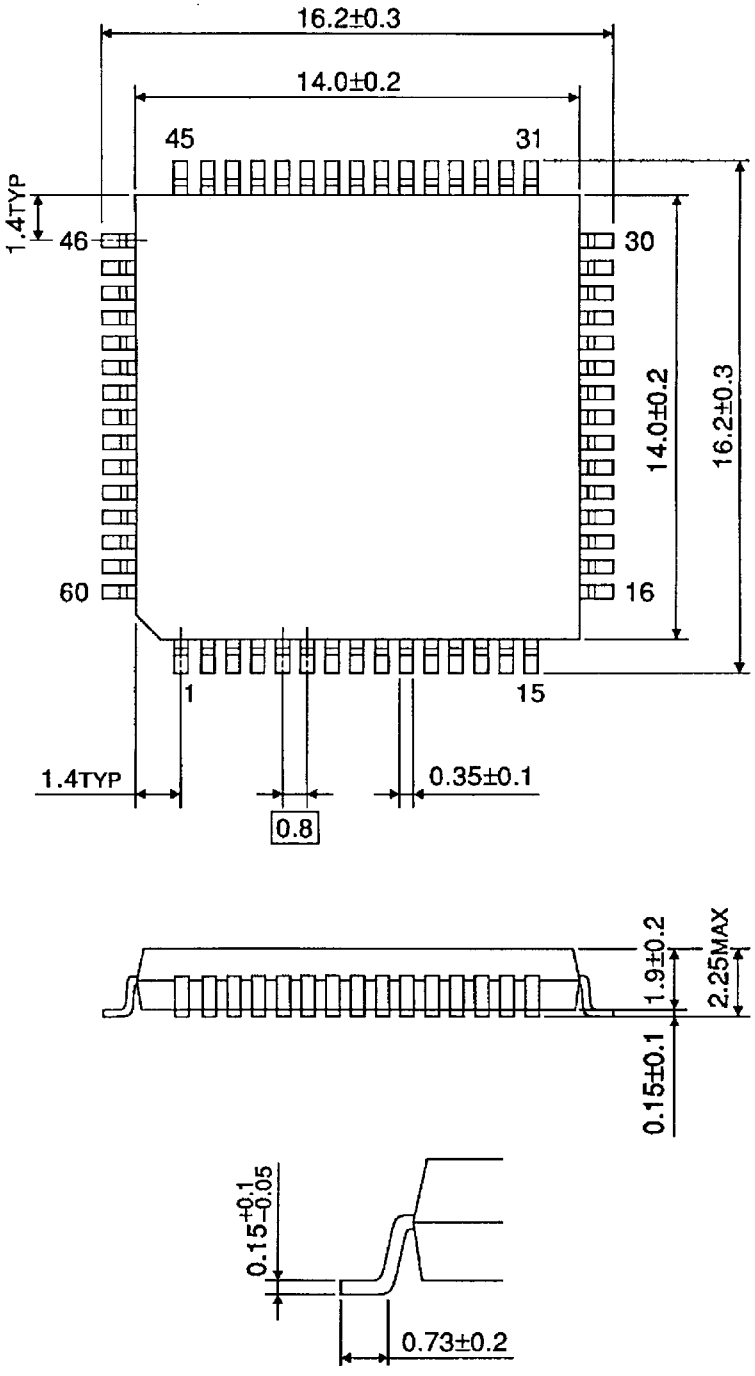
Example of Connection to Prescaler TD7103F



Note 80: TC9316FA, TC9316FB: Pin No. 45, 46 and 47 is change 47, 49 and 50.

Package Dimensions

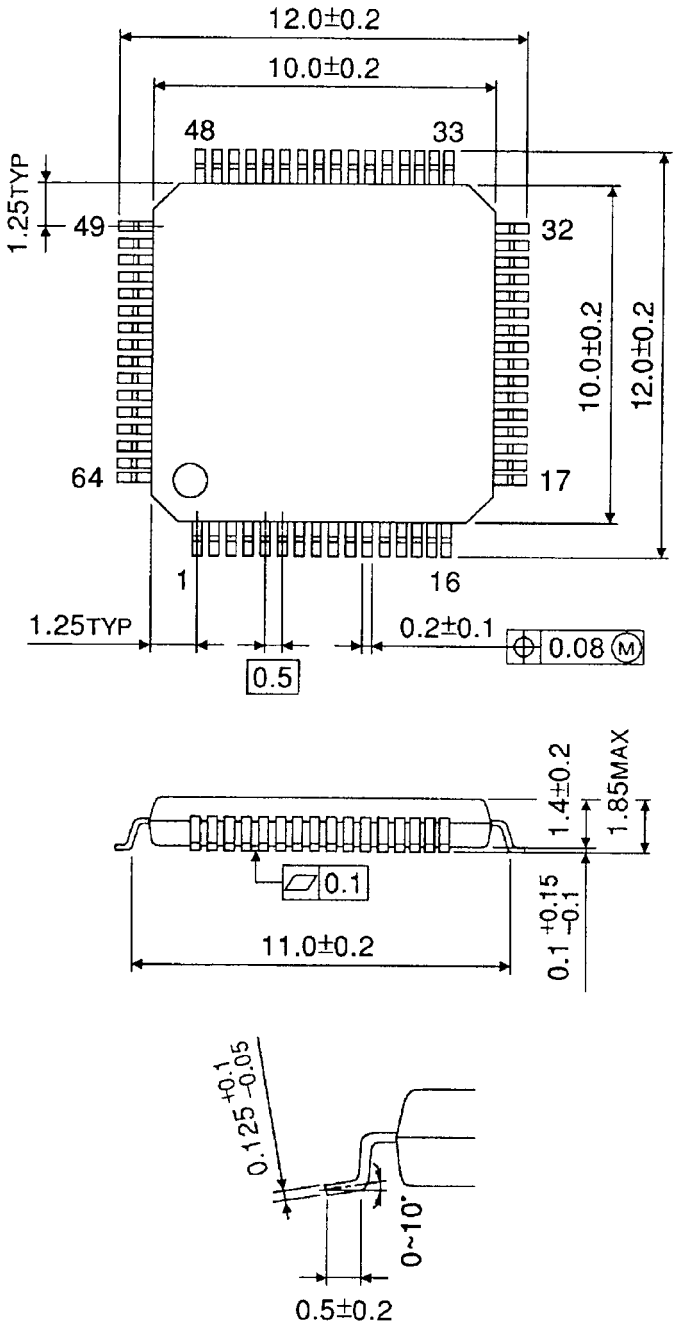
QFP60-P-1414-0.80E Unit : mm



Weight: 0.85 g (typ.)

Package Dimensions

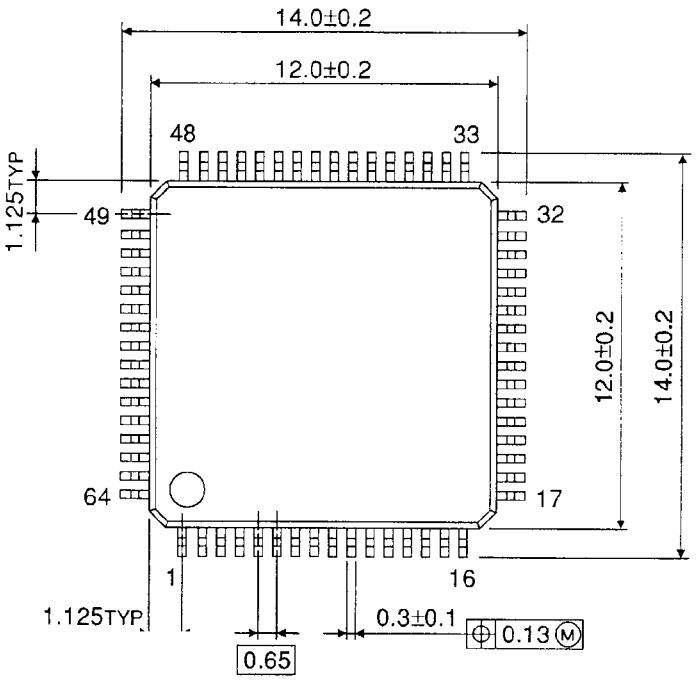
LQFP64-P-1010-0.50 Unit : mm

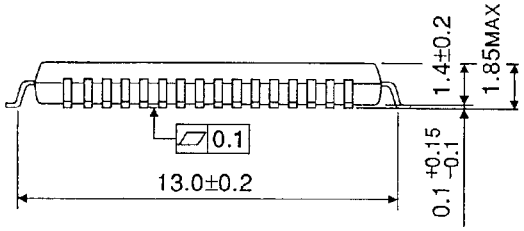


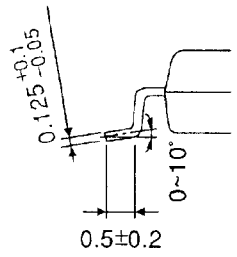
Weight: 0.32 g (typ.)

Package Dimensions

QFP64-P-1212-0.65 Unit : mm







Weight: 0.45 g (typ.)

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