

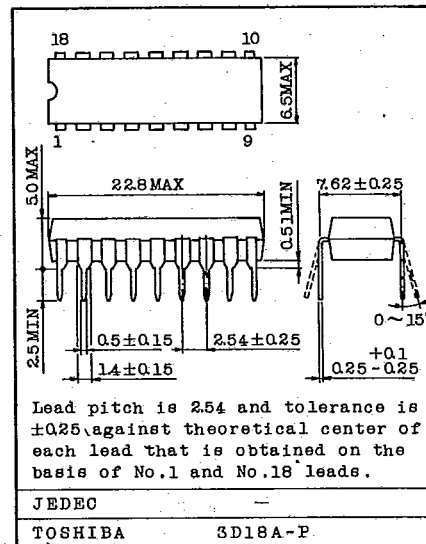
# TC9109BP

TENTATIVE

## TC9109BP CB TRANSCEIVER PLL FREQUENCY SYNTHESIZER

- TC9109BP (C-MOS LSI) may be used a 40 channels CB transceiver frequency synthesizer.
- Included high speed programmable counter, operated direct division of VCO can be used a simplified external circuit high quality PLL synthesizer in two-way.
- Outline is a 18 pin DIP.

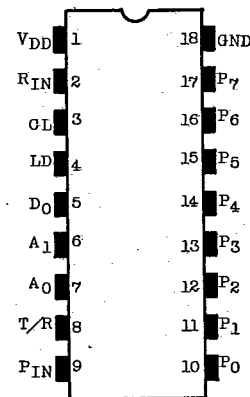
Unit in mm



### MAXIMUM RATINGS ( Ta = 25°C )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ +10	V
Input Voltage	VIN	-0.3 ~ VDD + 0.3	V
Operation Temperature	T <sub>opr</sub>	-30 ~ 70	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ 125	°C

### PIN CONNECTION



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## FEATURE

- Single X-tal (10.24MHz), All 40 channels CB transceiver.
- Direct division of VCO oscillation frequency due to high speed programmable counter, not necessary mixing down.

The following Fig. 1 and Fig. 2 show the external circuit difference between present single X-tal type and TC9109BP (Toshiba new single X-tal). TC9109BP can simplify external circuit

Fig. 1 PRESENT SINGLE X-TAL METHOD

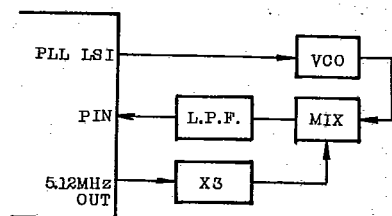
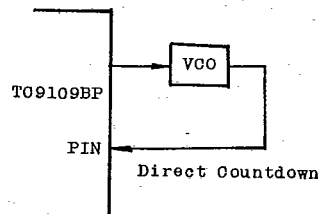


Fig. 2 TC9109BP DIRECT DIVISION METHOD



- In reception, the reference frequency is 5kHz and VCO frequency is 1627 ~ 1671 MHz (the frequency of second mixer injection). In transmission, the reference frequency is 25kHz and VCO frequency is 13.4825 ~ 13.7025MHz. (the half frequency of transmitting) The following Fig. 3 and Fig. 4 show the external circuit difference between present signal X-tal type and TC9109BP. TC9109BP can eliminate adjacent spurious problem and also has another advantage to simplify external circuit.

Fig. 3 PRESENT METHOD

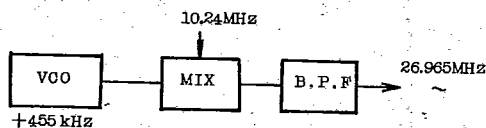
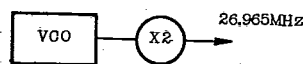


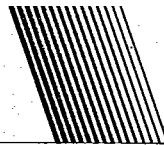
Fig. 4 TC9109BP



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- Can be programmed by 2 digit, 7 segment type LED drive code because of included code converter in internal channel selection program circuit. Therefore convenient to rotary switch/LEC channel indicator type, and also can use conventional rotary switch.
- Included a detector of misprogram.  
Detected wrong program and can be stopped PLL function at the moment.
- Included a detector of lockout.  
When switched transmitting/receiving or channel, can detect instant lockout state, and make transmitting power hold for a short time. This hold time may be determined by value of external capacitor. This function is effective as a audio muting against shock noise in channel change.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified  $V_{DD}=8V$ ,  $R_{IN}=10.24MHz$ ,  $T_a=25^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	$V_{DD}$			7.5	8.0	8.5	V
Operating Supply Current	$I_{DD}$		$V_{DD}=8V$ , $f_{IN}=16MHz$	-	18	25	mA

## PROGRAMMABLE COUNTER

Max. Operation Frequency	$f_{(Max)}$		$V_{DD}=7.5V$	20	-	-	MHz
Min. Operation Input Voltage	$V_{IN(Min)}$		$f_{IN}=20MHz$	2	-	-	Vp-p

## REFERENCE DIVIDER

Max. Operation Frequency	$f_{(Max)}$		$V_{DD}=7.5V$	12	-	-	MHz
Min. Operation Input Voltage	$V_{IN(Min)}$		$f_{IN}=12MHz$	1	-	-	Vp-p

## "H" LEVEL OUTPUT CURRENT

$D_0$ Output	$I_{OH D_0}$		$V_{OH}=7.0V$	-	0.3	-	mA
$A_0$ Output	$I_{OH A_0}$						
CL Output	$I_{OH CL}$						
LD Output	$I_{OH LD}$						

## "L" LEVEL OUTPUT CURRENT

$D_0$ Output	$I_{OL D_0}$		$V_{OL}=1V$	-	0.3	-	mA
$A_0$ Output	$I_{OL A_0}$		$V_{OL}=8V$	-	20	-	$\mu A$
CL Output	$I_{OL CL}$						
LD Output	$I_{OL LD}$		$V_{OL}=1V$	-	0.3	-	mA

 $D_0$  TRI-STATE LEAKAGE

Leakage Current	"H" Level	$I_{TLH D_0}$		-	0.1	-	nA
	"L" Level	$I_{TLL D_0}$					

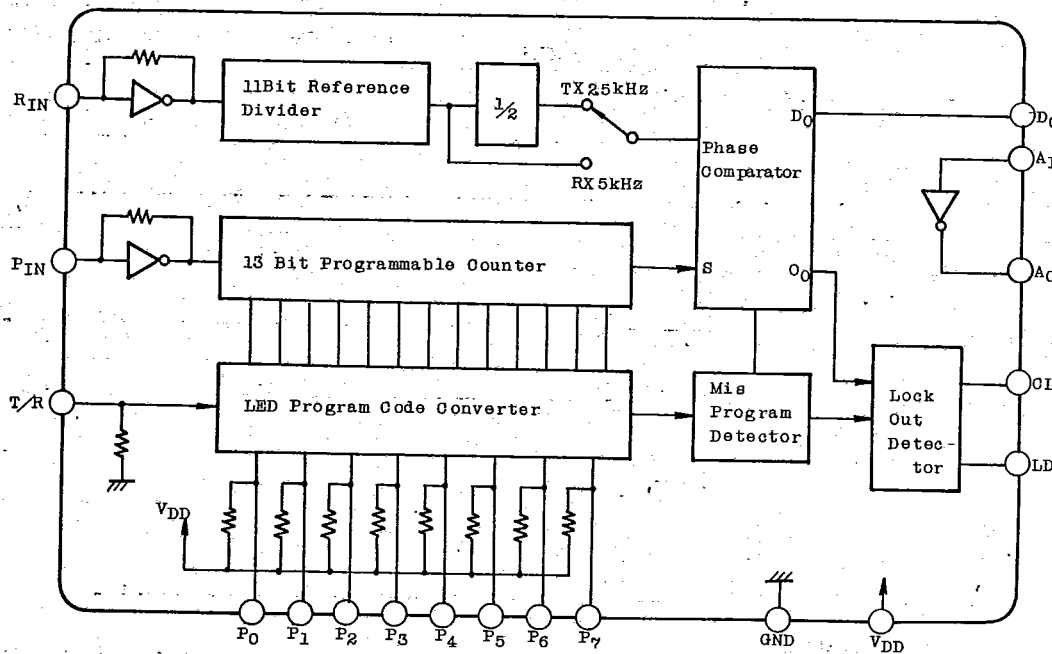
## AMPLIFIER

Voltage Gain			$f=5kHz$	-	25	-	dB
Input Leakage Current	"H" Level	$I_{IH A_I}$	$V_{IH}=8V$	-	0.1	-	nA
	"L" Level	$I_{IL A_I}$	$V_{IL}=0V$				

 $P_0 \sim P_7$ , T/R

Pull up/Down Resistance	$R_{IN}$			20	50	80	$k\Omega$
Input Voltage	"H" Level	$V_{IH}$		6.0	-	$V_{DD} + 0.3$	V
	"L" Level	$V_{IL}$		-0.3	-	2.0	V

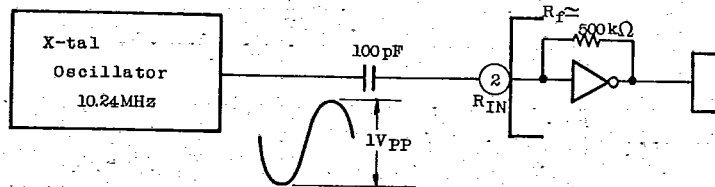
### BLOCK DIAGRAM



### BRIEF EXPLANATION OF EACH BLOCK PERFORMANCE

#### 1. REFERENCE FREQUENCY DIVIDER (11 BIT REFERENCE DIVIDER)

- Reference frequency divider generate reference frequency 50kHz/2.5kHz by 11-stage binary counter (supplied 10.24MHz signal from R<sub>IN</sub> terminal).
- R<sub>IN</sub> input circuit has self-biased amplifier, input signal through a coupling capacitor is enough about 1 V<sub>p-p</sub> sinoidal wave.



## TC9109BP

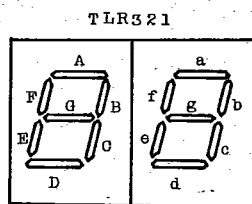
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## 2. PROGRAMMABLE COUNTER (13 BIT PROGRAMMABLE COUNTER)

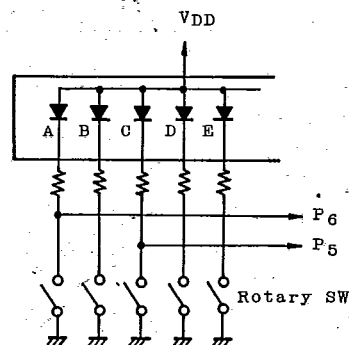
- Programmable counter is a 13 bit variable divider. Divided by indicated divide ratio from code converter binary code which is mentioned in following.
- TC9109BP has special high speed programmable counter, maximum operation frequency is higher than 20 MHz at  $V_{DD}=8V$ . Therefore can be divided directly by programmable counter without loop mixer.
- Divide range of programmable counter is 3345 ~ 3433 division (in transmitting) and 3254 ~ 3342 division (in receiving).
- Pin input has a self-biased amplifier as like as  $R_{IN}$  input circuit. Therefore low input signal like higher than 2 Vp-p (16 MHz) sinusoidal wave through a coupling capacitor is sufficient to operate it.

## 3. CODE CONVERTER

- $P_0 \sim P_7$  channel selection are programmed by 2 digit, 7 segment LED indication code. Code converter include read only memory (ROM) to convert  $P_0 \sim P_7$  input code to 13 bit binary code.
- This code converter include control terminal (T/R) to shift 2139 from the standard programmable counter division number in two ways. Obtained 10.695 MHz in case standard frequency is 5 kHz for example. When T/R is L or open, it is receive-state, when T/R is H, it is transmit-state.
- $P_0 \sim P_7$  input terminals include pull-up resistor respectively, read H level in case of open, lead connection between  $P_0 \sim P_7$  and LED is as follows.



$P_0$	f
$P_1$	a
$P_2$	g
$P_3$	e
$P_4$	d
$P_5$	C
$P_6$	A
$P_7$	F



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## 4. MISPROGRAM DETECTOR

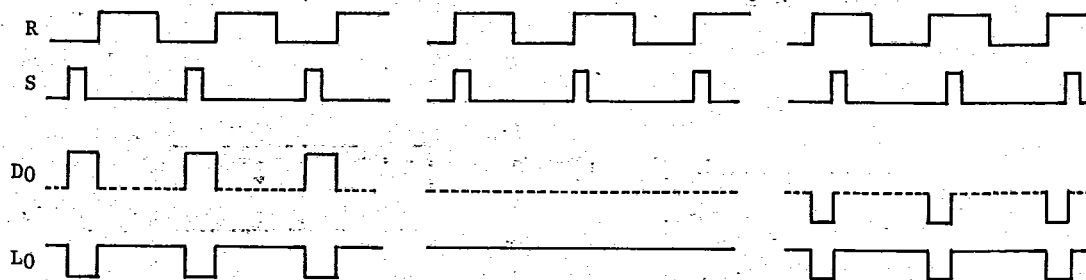
- Detect any wrong code except normal 1 ~ 40 channels from input.  
When wrong code is detected, controlled lockout detector. This circuit changes LD output level to be L-level and makes phase converter performance stop simultaneously.
- Protect perfectly performance against any external interference, for instance cause by rotary switch wrong contact.

## 5. PHASE COMPARATER

- Phase comparater generates proper VCO control voltage, compared frequency and phase between reference frequency, and output signal divided by programmable counter.
- S and R input signal rise-phases are compared. When S input signal phase advances D<sub>0</sub> output become to be H level, when delay D<sub>0</sub> output become L level. Otherwise D<sub>0</sub> output is held to be high impedance state.
- D<sub>0</sub> terminal output signal controls VCO by converting DC level through low pass filter which has proper time constant.

Performance waveforms in phase comparater are shown below.

Fig. 3 PHASE COMPARATER WAVEFORM



(Note) L<sub>0</sub> output is supplied to lock out detector.

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## 6. LOCKOUT DETECTOR

- Detects lockout state and supplies L level signal to LD terminal when abnormal phenomena occur in external circuit, for example PLL lockout caused at channel selection or on/off of press talk switch.
- LD terminal turns to L level in case that misprogram detector circuit operate like as lockout state.
- After lockout (L level), LD terminal is held for determined period, then returns H level. The constant time period can be chosen by capacitor value between CL terminal and ground.

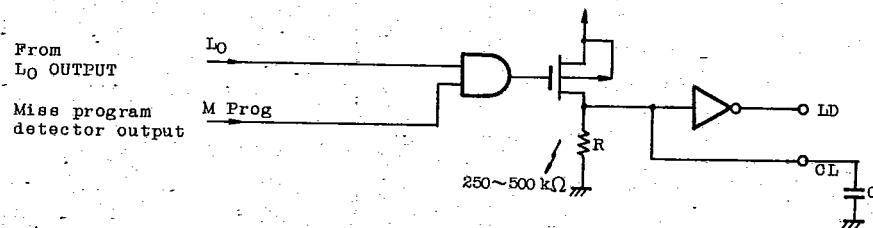


Fig. 4 LOGIC DIAGRAM

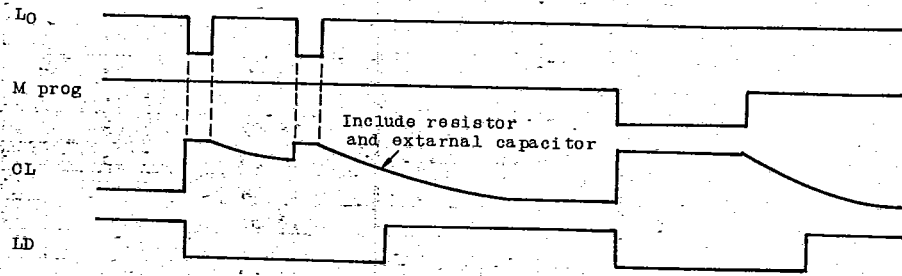


Fig. 5 OPERATION WAVEFORM



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PROGRAM CODE TABLE

(Note) O show "H" level

fVCO=N×0.005 (MHz)

CHANNEL NUMBER	PROGRAM CODE								R/T=L (RECEIVE)		R/T=H (TRANSMIT)	
	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>	N	fVCO	N	fVCO
1	○	○	○	○	○	○	○	○	3254	16.27	5393	13.4825
2	○					○	○	○	3256	16.28	5395	13.4875
3	○			○		○	○	○	3258	16.29	5397	13.4925
4		○		○	○	○	○	○	3262	16.31	5401	13.5025
5				○		○	○	○	3264	16.32	5403	13.5075
6		○				○	○	○	3266	16.33	5405	13.5125
7	○		○	○	○	○	○	○	3268	16.34	5407	13.5175
8						○	○	○	3272	16.36	5411	13.5275
9				○	○	○	○	○	3274	16.37	5413	13.5325
10			○				○	○	3276	16.38	5415	13.5375
11	○	○	○	○	○		○	○	3278	16.39	5417	13.5425
12	○						○	○	3282	16.41	5421	13.5525
13	○			○			○	○	3284	16.42	5423	13.5575
14		○		○	○		○	○	3286	16.43	5425	13.5625
15				○			○	○	3288	16.44	5427	13.5675
16		○					○	○	3292	16.46	5431	13.5775
17	○		○	○	○		○	○	3294	16.47	5433	13.5825
18							○	○	3296	16.48	5435	13.5875
19				○	○		○	○	3298	16.49	5437	13.5925
20			○				○	○	3302	16.51	5441	13.6025
21	○	○	○	○	○		○	○	3304	16.52	5443	13.6075
22	○						○	○	3306	16.53	5445	13.6125
23	○			○			○	○	3312	16.56	5451	13.6275
24		○		○	○		○	○	3308	16.54	5447	13.6175
25				○			○	○	3310	16.55	5449	13.6225
26		○					○	○	3314	16.57	5453	13.6325
27	○		○	○	○		○	○	3316	16.58	5455	13.6375
28							○	○	3318	16.59	5457	13.6425
29				○	○		○	○	3320	16.60	5459	13.6475
30			○				○	○	3322	16.61	5461	13.6525
31	○	○	○	○	○		○	○	3324	16.62	5463	13.6575
32	○						○	○	3326	16.63	5465	13.6625
33	○			○			○	○	3328	16.64	5467	13.6675
34		○		○	○		○	○	3330	16.65	5469	13.6725
35				○			○	○	3332	16.66	5471	13.6775
36		○					○	○	3334	16.67	5473	13.6825
37	○		○	○	○		○	○	3336	16.68	5475	13.6875
38							○	○	3338	16.69	5477	13.6925
39				○	○		○	○	3340	16.70	5479	13.6975
40			○				○	○	3342	16.71	5481	13.7025

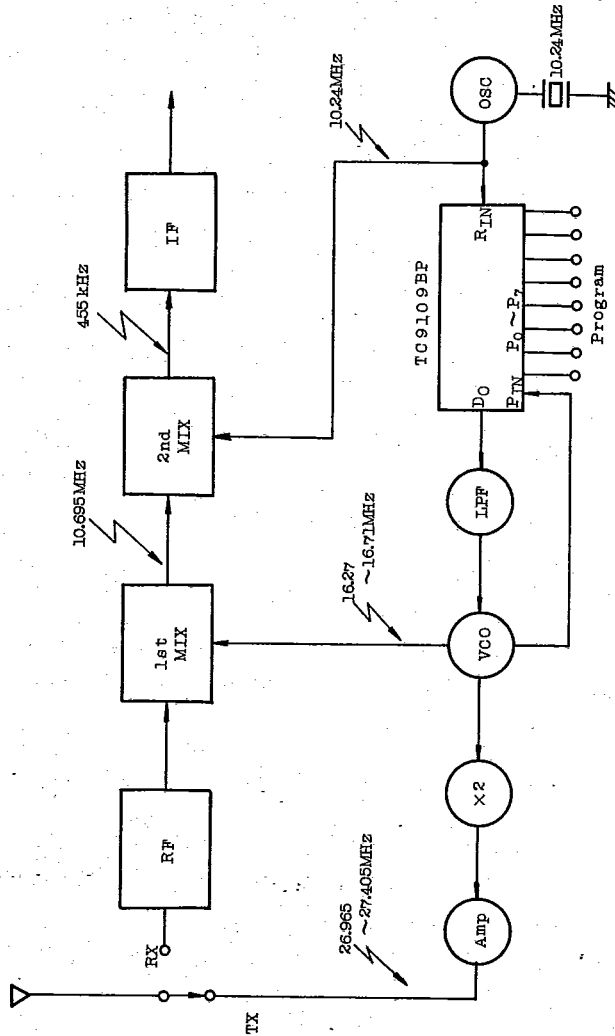
(Note) Rotary switch P<sub>0</sub> ~ P<sub>7</sub> : None-mark is "ON", 0-mark is "OPEN"

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APPLICATION BLOCK DIAGRAM



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## PERFORMANCE AGAINST WRONG-PROGRAM

- o TC9109BP include a program data code, ROM, respectively only 40 channel, regulated by FCC rules.  
Any external channel selection program can determine the data out of the programmable counter in the IC directly, and cannot generate the any other frequency except only formal 40 channel frequencies.
- o TC9109BP include eight program input terminals because of LED drive code. So these are 256 combinations due to eight inputs theoretically, however, this IC is designed to detect only formal 40 channel combinations. At the other combinations, this IC detects wrong code combinations or mis-programs, then make a phase comparator performance in the IC stop and transmitting output of two way radio is cut off by generated lockout signal at the moment.
- o As the above mentioned, TC9109BP is designed to prevent any abnormal performances and interferences perfectly due to channel selection failure, illegal modification, or any other malfunctions.

Following are an explanation on circuit performance.

When the 8 bit channel data is put into ROM-1, if the channel data is one of normal 1 ~ 40 channels, output of ROM-1 is sent to ROM-2 and the output of NOR gate is L-level

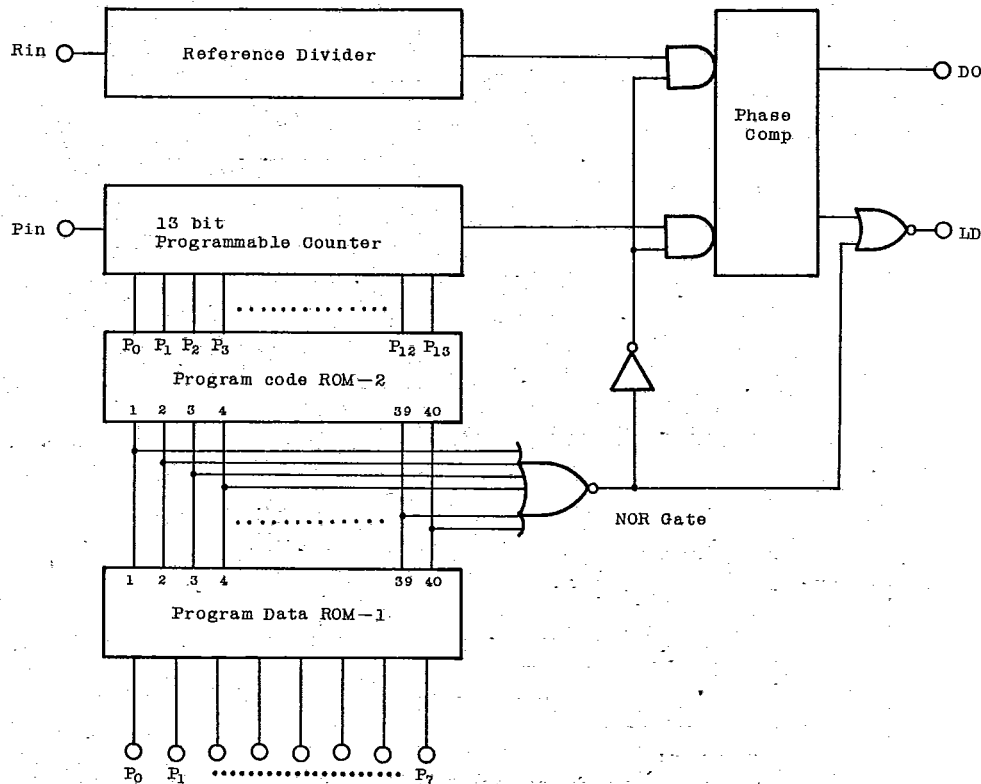
When the input channel data is the wrong except normal 1 ~ 40 channel, the NOR output changes H-level.

At the same time, this circuit changes LD output level to be L-level and make phase comparator performance stop.

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PROGRAM CODE DETECTOR BLOCK DIAGRAM



AUDIO DIGITAL IC

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APPLICATION CIRCUIT OF PLL SYNTHESIZER

